RZ5D BioAmp Processor

Hardware Reference

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RZ5D BioAmp Processor

RZ5D Overview

The RZ5D BioAmp Processor features up to four digital signal processors cards. Any card can be either a single standard processor card (RZDSP) or a quad core processor card (QZDSP). Standard single processor cards use a single Sharc DSP; quad-core processor cards use four Sharc DSPs cores with the potential to more than double the power of the RZ5D. All cards are networked on a multiprocessor architecture that features efficient onboard communication and memory access. The RZ5D is a versatile solution for real-time processing and simultaneous acquisition and stimulation.

The RZ5D acquires and processes up to 32 channels of neurophysiological signals in real-time. Data can be input from a PZ5 amplifier or digital headstage manifold at a sampling rate of up to ~50 kHz. The RZ5D also supports microstimulation applications. The RZ5D can be used with TDT's IZV Subject Interface (SI) for up to 128 channels of stimulation and switching headstages (ZC_SW) to comprise a complete microstimulation system.

Both single and quad-core processors cards may include an optical interface for connection to devices such as the RS4 Data Streamer or a second PZ Amplifier.

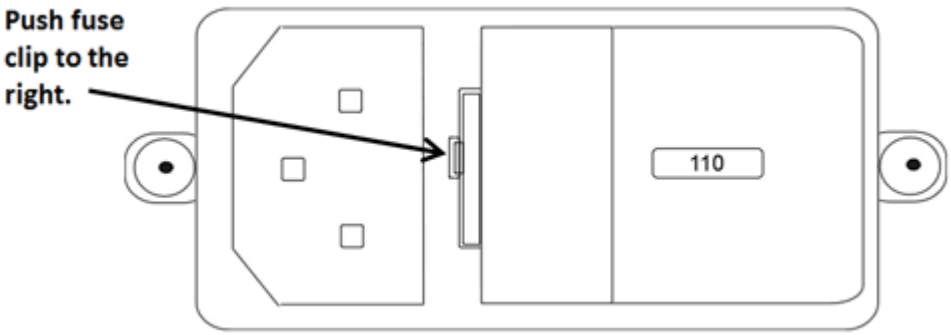
The RZ5D also features eight channels of analog I/O, 24 bits of digital I/O and an onboard monitor speaker with volume control.

Power and Communication

The RZ5D's Optibit optical interface connects to a PO5, PO5e, PO5c, or UZ3 computer interface card for fast and reliable data transfer from the RZ2 to the PC. Connectors on the back panel are color coded for correct wiring.

The RZ5D's integrated power supply is shipped from TDT configured for the end user's regional voltage setting (110 V or 220 V). If you need to change the voltage setting:

1. Turn off the RZ5D
2. Use a small flathead screwdriver to gently push the clip along the left side of the fuse plate to the right to remove it.



3. Remove the white AC voltage selector and rotate it until the desired voltage is displayed, then reinsert it and put the fuse plate back on.

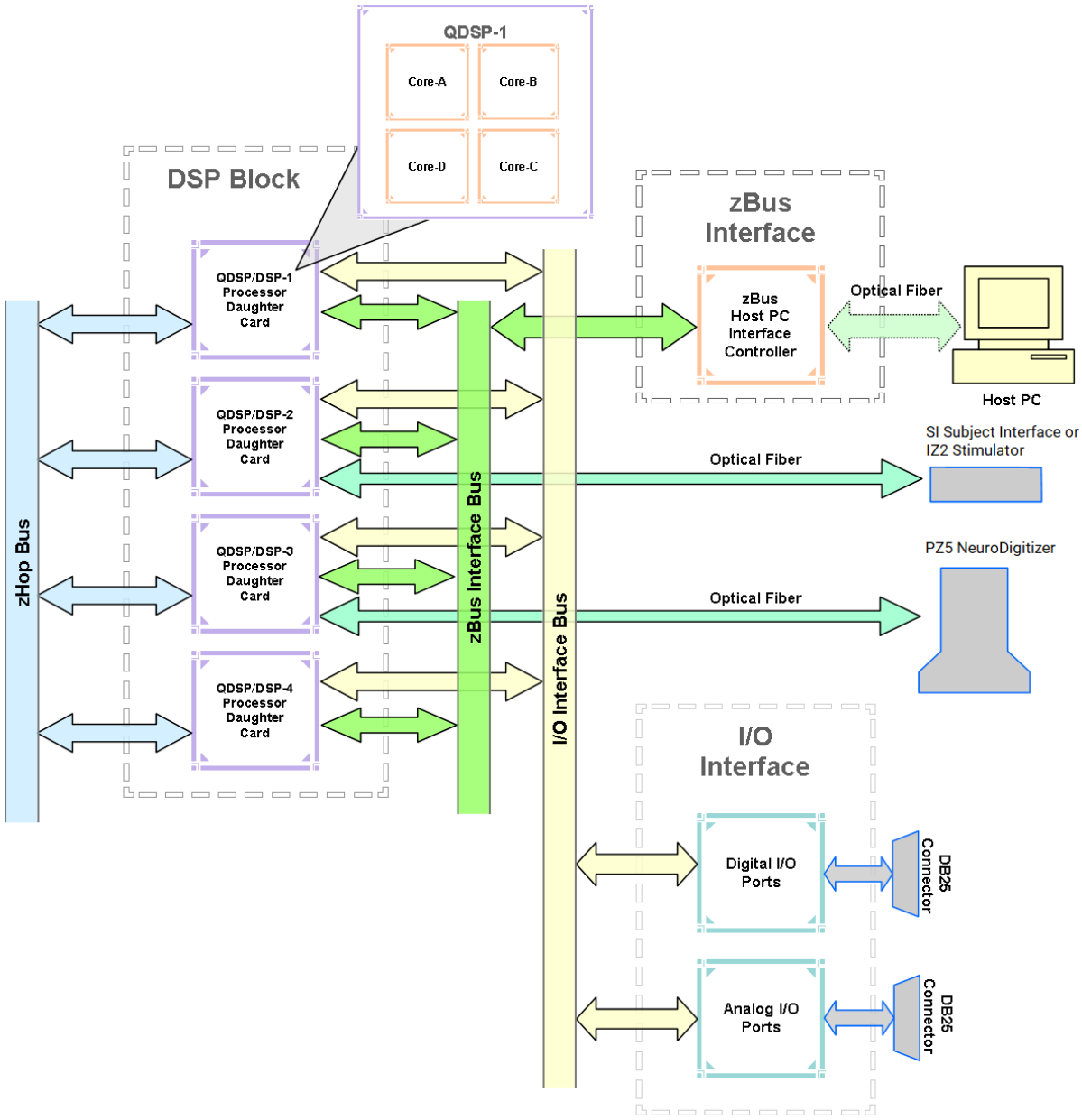
The RZ5D is UL compliant, see the RZ5 Operator's Manual for power and safety information.

Software Control

TDT's Synapse software controls the RZ5D and provides users a high level interface for device configuration.

RZ5D Architecture

The RZ5D processor uses a multi-bus architecture and offers three dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when designing experiments.



RZ5D Multi-DSP Architecture Functional Diagram

As shown in the diagram above, the RZ5D architecture consists of three functional blocks:

The DSPs	Each DSP in the DSP Block is connected to a local interface to the three data buses: two buses that connect each DSP to the other functional blocks and one that handles data transfer between the DSPs. Each standard DSP is connected to 64 MB SDRAM and each core in a QZDSP is connected to 256 MB DDR2. This architecture facilitates fast DSP-to-off-chip data handling. Because each DSP has its own associated memory, access is very fast and efficient. However, large and complex circuits should be designed to balance memory needs (such as data buffers and filter coefficients) across processors. The maximum number of circuit components for each RZ5D standard RZDSP is 768 and 1000 for each QZDSP core. DSP-2 and DSP-3 are special optical DSPs to connect directly to peripheral devices such as the SI, PZ, or iCon.
The zBus Interface	The zBus interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus interface bus, allowing for large high-speed data reads and writes without interfering with other system processing.
The I/O Interface	The I/O interface serves as a connection to outside signal sources or output devices. It is used to input data from the preamplifier inputs and digital and analog channels. The I/O interface bus provides a direct connection to each DSP.

Bus Related Delays

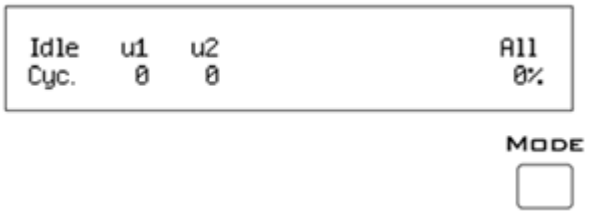
A standard two sample delay is associated with the zHop. However, these delays are managed for the user in Synapse software.

RZ5D Features

DSP Status Lights

These LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The corresponding LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second). For QZDSPs, the LED indicates levels for the core with the highest cycle usage.

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The top line reports the system mode, Run!, Idle, or Reset. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Reset).

> **Note**
>
> When burning new microcode or if the firmware on the RZ is blank, the display screen will report a cycle usage of 99% and the processor status lights will flash red.

Indicator	Description
Cyc	Cycle usage. For QZDSPs, the highest core cycle usage is shown
Bus%	Percentage of internal device's bus capacity used
I/O%	Percentage of data transfer capacity used

PZ Preamplifier Port

The RZ5D acquires digitized signals from a PZ5 preamplifier via a fiber optic cable through the port labeled 'PZ' on the front panel. This port can input up to 32 channels at a maximum sampling rate of ~50 kHz. The PZ port can be used with any of the PZ preamplifier and is configured in Synapse software.

SI Subject Interface Port

The output port labeled SI can be used with a Subject Interface, PZ5 amplifier, or iCon Behavioral Controller for up to 128 channels of electrical stimulation, neurophysiological recording, or behavior control.

> **Note**
>
> RZ5D with serial number <1215 had an IZ port for IZ2 Stimulator support.

Onboard Analog I/O

The RZ5D is equipped with four channels of 16-bit PCM D/A and four channels of 16-bit PCM A/D. All 8 channels can be accessed via front panel BNCs marked ADC and DAC or via a 25-pin analog I/O connector. See RZ5D Technical Specifications for the DB25 pinout.

The following table provides a quick overview of the analog I/O features and how they must be accessed during experiment design.

Analog I/O	Synapse Access	Notes
ADC Analog Inputs	ADC Tab	Accessed through ADC Input BNCs or Analog I/O labeled DB25
DAC Analog Outputs	DAC Tab	Accessed through DAC Output BNCs or Analog I/O labeled DB25

Monitor Speaker

The RZ5D is equipped with an onboard speaker. To use the speaker, feed the desired signal to the first DAC output channel. The speaker is provided primarily for audio monitoring of a single channel of electrophysiological potentials during recording.

Digital I/O

The digital I/O ports include 24 bits of programmable I/O. The digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ5D and bits 0 - 3 of byte C are available through BNC connectors on the front panel labeled Digital. See RZ5D Technical Specifications for the DB25 pinout.

The digital I/O is configured in the Synapse RZn Hal.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable

*Note: Byte C Bits 0 - 3 are available via front panel BNCs

The data direction for the Digital I/O is also configured in the Synapse RZn Hal.

The RZ digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table listing the different voltage outputs and thresholds for both types.

Digital I/O Type	Output High	Output Low	Input High	Input Low
Port A & Port B	5 V	0 V	>=2.5 V	0-2.45 V
Port C	3.3 V	0 V	>=1.5 V	0-1.4 V

LED Indicators

The RZ5D has 16 LED indicators for the analog and digital I/O located directly below the display screen and DSP status LEDs.

Digital I/O

These LEDs indicate the state of the 8 bit-addressable I/O of byte C.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog I/O

These LEDs indicate the state of the four ADC and four DAC channels.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than ±100 mV
Dim Green	Analog I/O channel signal voltage is less than ±5 V
Solid Green	Analog I/O channel signal voltage is between ±5 V to ±9 V
Solid Red	Analog I/O channel clip warning (voltage greater than ±9 V)

UDP Ethernet Interface

The RZ UDP Ethernet interface can transfer low bandwidth data directly to or from a PC. RZ devices equipped with a UDP interface have an additional Ethernet port and RS232 serial port located on the back panel. See RZ-UDP Communications Interface for more information.

Specialized DSP/Optical Interface Boards

The RZ standard DSP boards can be replaced with specialized DSP boards which include an optical interface for communication and control of RZ compatible devices, such as the Subject Interface and RS4 Data Streamer. RZ devices equipped with one or more specialized DSP boards include an optical port for each card. The ports are located on the front panel and labeled for easy identification.

DSP	Supported Peripheral
RZDSP-I	IZ2 Stimulators
RZDSP-M	Subject Interface, PZ5 amplifier, iCon Behavioral Controller
RZDSP-P	PZ amplifier. It can be used to expand the number of channels that can be acquired on any RZ processor.
RZDSP-S	RS4 Data Streamer, allowing the RZ device to stream data directly to the RS4's storage arrays.
RZDSP-U	PO8e interface card, allowing the RZ device to stream data directly to client software.
RZDSP-V	RV2 Video Tracking System
QZDSP_OPT	Supports all of the above devices.

RZ5D Technical Specifications

> **Note**
>
> Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

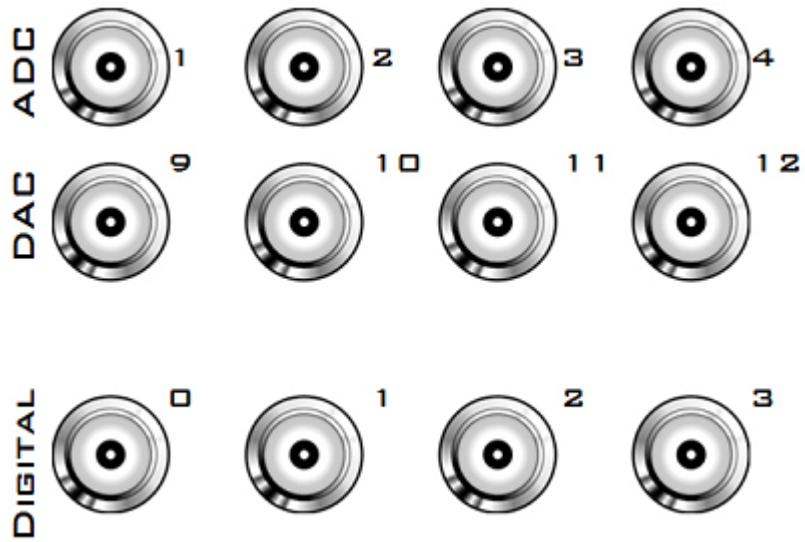
DSP	Up to four standard DSPs and/or quad-core (QZDSP) DSP: 400 MHz DSPs, 2.4 GFLOPS peak per DSP QZDSP: Four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per core, four cores per QZDSP
Digital I/O	8 programmable bits: 3.3 V (5.0 V max input), 25 mA max load 2 programmable bytes (16 bits): 5.0 V (6.0 V max input), 35 mA max load
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44 * Fs (Fs = sample rate)
Voltage Out	±10.0 V, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	10 Ohms
A/D	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	±10.0 V
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Ports	
M	Two connections for Subject Interface, PZ5, or iCon (serial >=1233)
SI	One connection for Subject Interface, PZ5, or iCon (serial 1215-1232)
IZ	One connection for IZ2 Stimulator (serial <1215)
PZ	One connection for PZ5 NeuroDigitizer (serial <1233)
Add-on (Optional)	Up to two, one per QZDSP_Opt or Optical DSP card upgrade.

Note

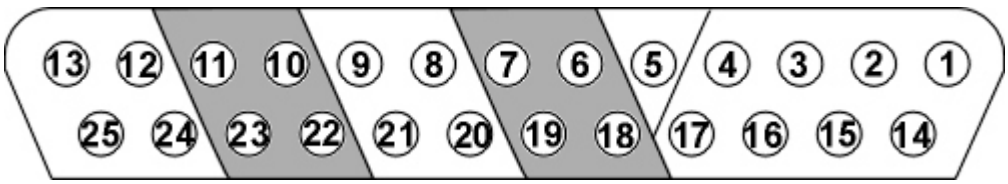
Technical specifications for preamplifier A/D converters and stimulator outputs are found in the specific preamplifier / stimulator document.

BNC Channel Mapping

Please note channel numbering begins at the top left block of BNCs for both analog and digital I/O and is printed on the face of the device to minimize miswiring.

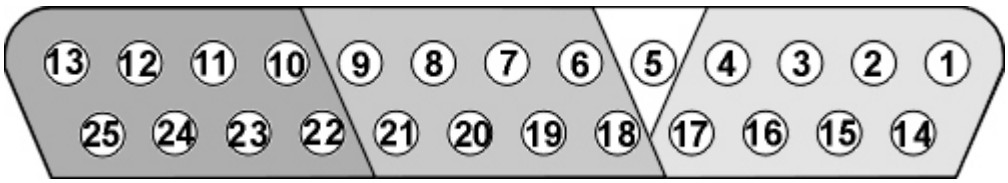


DB25 Analog I/O Pinout



Pin	Name	Description	Pin	Name	Description
1	NA	Not Used	14	NA	Not Used
2	NA		15	NA	
3	NA		16	NA	
4	NA		17	NA	
5	AGND	Analog Ground	18	A1	Analog Input
6	A2	Analog Input	19	A3	
7	A4		20	NA	Not Used
8	NA	Not Used	21	NA	
9	NA		22	A9	Analog Output
10	A10	Analog Output	23	A11	
11	A12		24	NA	Not Used
12	NA	Not Used	25	NA	
13	NA				

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Port C Bit Addressable		14	C1	Port C Bit Addressable
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Port A Word Addressable
6	A1	Port A Word Addressable		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Port B Word Addressable
10	B1	Port B Word Addressable		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

If using a PP24 Patch Panel, see PP24 to RZ5D Digital I/O.