

RP2.1 Real-Time Processor

Hardware Reference



Updated 2024-12-19

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Table of Contents

RP2.1 Real-Time Processor

RP2.1 Overview	4
Power and Communication	4
Software Control	4
Features	5
Memory	5
Digital Input/Output Bits	5
D/A and A/D	5
Hardware	5
RP2.1 Technical Specifications	7
DB25 Connector Pin Out	7

RP2.1 Real-Time Processor



RP2.1 Overview

The RP2.1 real-time processors consist of an Analog Devices Sharc floating point DSP with surrounding analog and digital interface circuits to yield a powerful programmable signal-processing device capable of handling a variety of tasks.

Power and Communication

The RP2.1 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using any of the zBus PC interfaces. The ZB1PS is UL compliant, see the [ZB1PS Operations Manual](#) for power and safety information.

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the [RPvdsEx Manual](#).

Features

Memory

The RP2.1 comes with 32 MB of memory for data storage and retrieval.

Digital Input/Output Bits

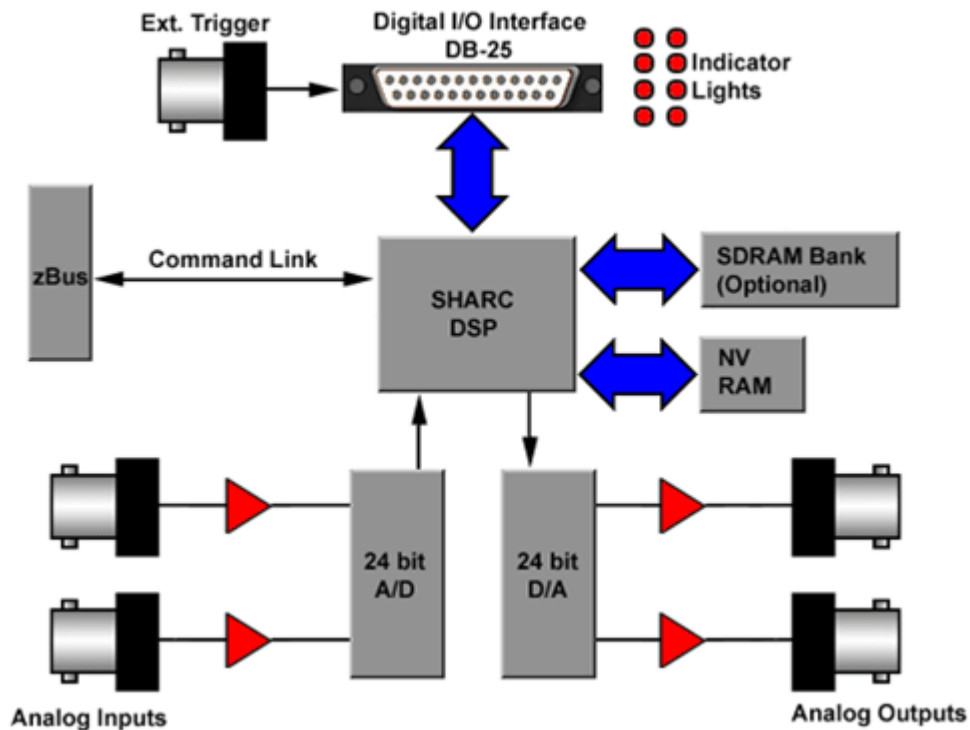
The digital I/O circuits include eight bits of digital input and eight bits of digital output that are accessed on the 25 pin connector on the front of the RP2.1. The bits of these ports can be programmed individually or as a 'digital word' and used in a variety of ways within the RP2.1 processing circuit, including implementing triggers, timing trigger responses, and lighting LEDs. The first four bits of the digital inputs and digital outputs as well as the Trigger/Enable input are mapped to LED indicators on the front panel of the RP2. There is an additional TRIG input BNC on the front panel.

D/A and A/D

The RP2.1 is equipped with two channels of 24-bit, 200 kHz sigma-delta D/A and two channels of 24-bit, 200 kHz sigma-delta A/D. Sigma-Delta converters provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. See [RP2.1 Technical Specifications](#) for the group delay of each device.

Hardware

The 32 MB of SDRAM are used for storage of long stimulus waveforms and acquired data. All of the RPvdsEx buffer components, used to build circuits for the RP2, utilize the SDRAM memory. The RP2.1 communicates with and is programmed through the zBus.



The RP2.1 is interfaced to the analog world via a two channel 24-bit analog to digital converter and a two channel 24-bit digital to analog converter. The RP2 system's I/O buffer handles ± 10 V signals with excellent signal to noise performance. The RP2 contains a 100 kHz (50 kHz BW) A/D and a 200 kHz (100 kHz BW) D/A, while the RP2-5 has a 50 kHz (25 kHz BW) A/D and D/A. Both devices allow for user programmable sampling rates from the specified maximum down to 6.25 kHz. A special calibration program is used to calibrate the RP2's analog I/O offering very small gain and DC offset errors.

RP2.1 Technical Specifications

DSP	50 MHz Sharc 21065, 150 MFLOPS
Memory	32 MB SDRAM
Digital I/O	8 input bits, 8 output bits, 1 TRIG input: 3.3 V (5.0 V max input), 25 mA max load
System Reset	Force input (see the section below on how to reset)

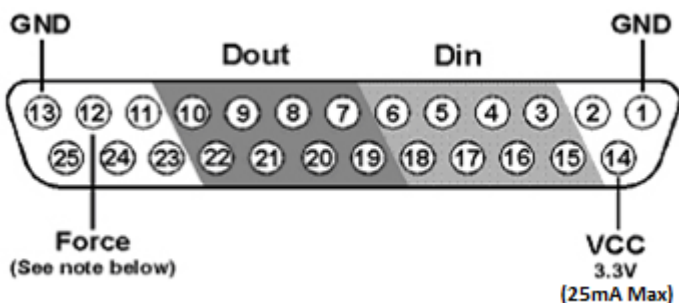
D/A 2 channels, 24-bit sigma-delta

Sample Rate	Up to 195.3125 kHz
Frequency Response	DC - $0.44 * F_s$ (F_s = sample rate)
Voltage Out	± 10.0 V, 175 mA max load
S/N (typical)	105 dB (20 Hz to 20 KHz), 95 dB (20 Hz to 50 KHz)
THD (typical)	-95 dB for 1 KHz output at 5 Vrms
Sample Delay	30 samples
Output Impedance	10 Ohms

A/D 2 channels, 24-bit sigma-delta

Sample Rate	Up to 195.3125 kHz
Frequency Response	DC - $0.44 * F_s$ (F_s = sample rate)
Voltage In	± 10.0 V
S/N (typical)	105 dB (20 Hz to 20 KHz), 95 dB (20 Hz to 50 KHz)
THD (typical)	-95 dB for 1 KHz input at 5 Vrms
Sample Delay	65 samples
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms

DB25 Connector Pin Out



Pin	Name	Description	Pin	Name	Description
1	GND	Ground	14	VCC	3.3 V (25 mA Max)
2	NA	Not Used	15	DI0	Digital Input Bits
3	DI1	Digital Input Bits	16	DI2	
4	DI3		17	DI4	
5	DI5		18	DI6	
6	DI7		19	DO0	Digital Output Bits
7	DO1	Digital Output Bits	20	DO2	
8	DO3		21	DO4	
9	DO5		22	DO6	
10	DO7		23	NA	Not Used
11	NA	Not Used	24	NA	
12	Force	Used to reset the RP2.1	25	NA	
13	GND	Ground			

Note

TDT recommends the PP16 Patch Panel for accessing digital I/O.

Important

Force is used to reset the RP2.1, including deleting the device's microcode. It has no function in data acquisition or manipulation.

To reset the device:

1. Connect a wire (or paper clip) from pin 12 to pin 13 on the Digital I/O port.
2. Use the desktop short cut to run zBusMon.
3. With pins 12 and 13 shorted, click the 'Reboot System!' button. The RP2.1 will appear as a 'G21' device.
4. Right-click on the G21 and select 'Program G21'.
5. In the System3 Device Programmer window, click the Browse button next to the uCode File field and select RP21.dxe.
6. Remove the short from pins 12 and 13, and click the 'Program Device!' button. Do not use your computer until the device reprogramming is complete (approximately four minutes).