

RZ5P Fiber Photometry Processor



RZ5P Overview

The RZ5P Processor is equipped with two 400 MHz Sharc digital signal processors networked on a multiprocessor architecture that features efficient onboard communication and memory access. The RZ5P is an optimized solution for fiber photometry and multi-channel neurophysiology.

The RZ5P features four channels of analog input and four channels of analog output. Its fiber optic input port can acquire up to 32 channels of neurophysiological signals to be processed in real-time. Data can be input from a PZ amplifier at a sampling rate of up to ~50 kHz. The RZ5P also features 24-bits of digital I/O and an onboard monitor speaker with volume control.

This manual provides hardware information for the RZ5P. For a full application guide specific to fiber photometry using the RZ5P, see the [Fiber Photometry User Guide for RZ5P](#).

Power and Communication

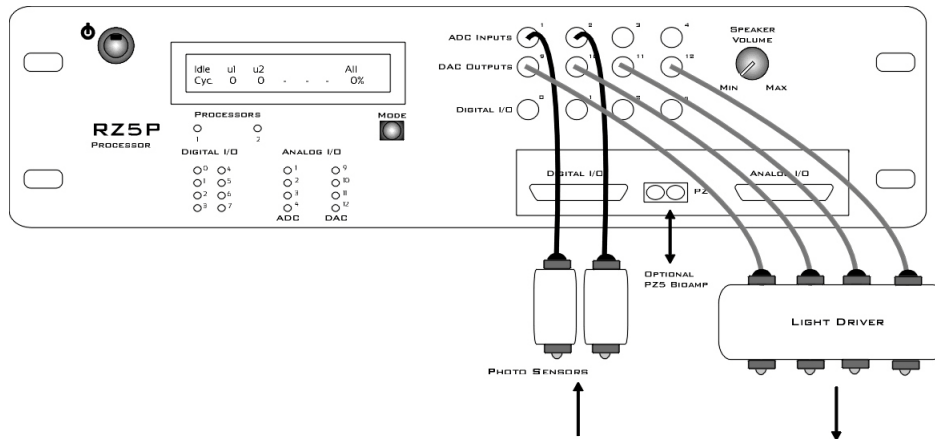
The RZ5P's integrated Optibit optical interface ensures fast and reliable data transfer from the RZ5P to the PC. Connectors are provided on the back panel and are color coded for correct wiring. The RZ5P's integrated power supply is shipped from the factory configured for the desired voltage setting (110 V or 220V). If you need to change the voltage setting, please contact TDT support at +1.386.462.9622 or email support@tdt.com.

Software Control

The RZ5P is intended for use with TDT's Synapse software. When custom control is required, see the RZ5D BioAmp Processor section in this manual for details on developing circuits in the System 3's RPvdsEx circuit design software. Note: PZ related macros should be moved to DSP-2 for the RZ5P.

Fiber Photometry Connections

On the front panel of the RZ5P, connect photo sensors to ADC BNCs 1 and 2 and connect light drivers to DAC BNCs 9 - 12.



Fiber Photometry System Connection Diagram

The Analog I/O DB25 connector can also be used for the connections. See “DB25 Analog I/O Pinout” on page 1-82.

RZ5P Features

DSP Status Displays

The RZ5P include status lights and a display screen to report the status of the individual processors.

Status Lights



Two LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The corresponding LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second).

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Reset).

Note: When burning new microcode or if the firmware on the RZ5P is blank, the display screen will report a cycle usage of 99% and the processor status lights will flash red.

Status Indicators	Description
Cyc:	processing cycle usage (note: limited to 2 digits; ex: 110 displayed as 10)
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
Opt:	Connection (sync) status of PZ amplifier

Important! The status lights flash when a DSP goes over its processor cycle usage limit, even if only for a particular cycle.

PZ Preamplifier Port

The RZ5P acquires digitized signals from a PZ preamplifier or digital headstage manifold over a fiber optic cable through the port labeled 'PZ' on the front panel. This port can input up to 32 channels at a maximum sampling rate of ~50 kHz. The PZ port can be used with any of the PZ preamplifiers including the PZ2, PZ3, and PZ5 or the PZ4 digital headstage manifold.

Onboard Analog I/O

The RZ5P is equipped with four channels of 16-bit PCM D/A and four channels of 16-bit PCM A/D. All 8 channels can be accessed via front panel BNCs marked ADC and DAC or via a 25-pin analog I/O connector. See the *Synapse Manual* for information on enabling analog I/O.

Monitor Speaker

The RZ5P is equipped with an onboard speaker tied to analog output channel 9. The speaker is provided primarily for audio monitoring of a single channel of input during recording.

Digital I/O

24 bits of programmable digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ5P and bits 0 - 3 of byte C are available through

BNC connectors on the front panel labeled Digital. See “RZ5P Technical Specifications” on page 1-81, for the DB25 pinout and BNC channel mapping.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable
*Note: Byte C Bits 0 - 3 are available via front panel BNCs				

See the *Synapse Manual* for information on enabling digital I/O and configuring data direction.

The RZ5P digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table depicting the different voltage outputs and thresholds for both type.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

LED Indicators

The RZ5P contains 16 LED indicators for the analog and digital I/O. These indicators are located directly below the display screen and DSP status LEDs. They display information relative to the various analog and digital I/O. The following tables illustrate the possible display options and their associated descriptions.

Digital I/O

These LEDs indicate the state of the 8 bit-addressable I/O of byte C.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog I/O

These LEDs indicate state of the ADC and DAC channels.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than +/-100 mV

Light Pattern	Description
Dim Green	Analog I/O channel signal voltage is less than +/-5 V
Solid Green	Analog I/O channel signal voltage is between +/-5 V to +/-9 V
Solid Red	Analog I/O channel clip warning (voltage greater than +/-9 V)

UDP Ethernet Interface (Optional)

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See “RZ-UDP Communications Interface” on page 1-51, for more information.

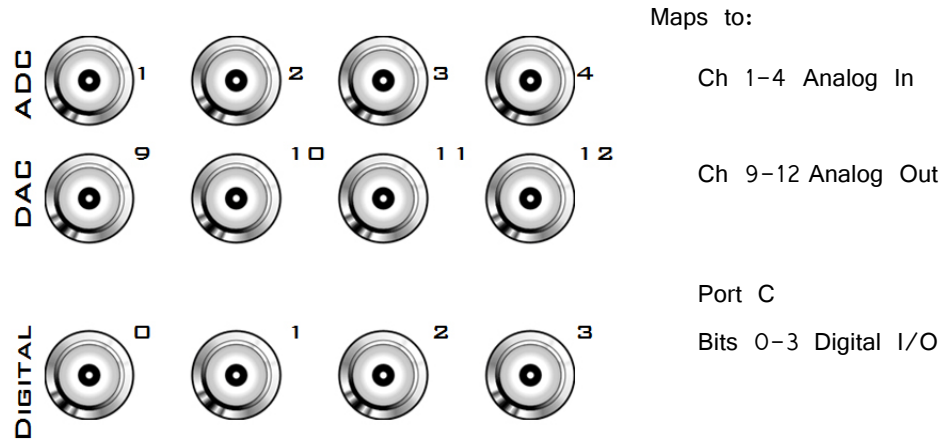
RZ5P Technical Specifications

Note: Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

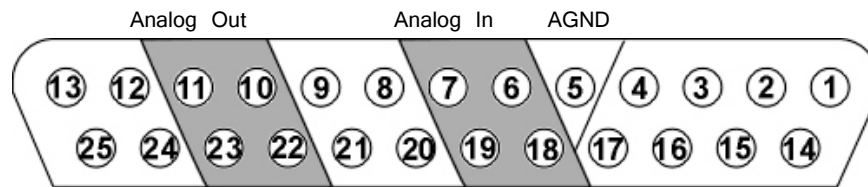
DSP	Two 400 MHz DSPs, 2.4 GFLOPS peak per DSP
Memory	64 MB SDRAM per DSP
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	10 Ohms
A/D	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Port	One input for PZ5, PZ2, PZ3 or PZ4, up to 32 channels
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes(16 bits): 5.0 V, 35 mA max load

BNC Channel Mapping

Please note channel numbering begins at the top left block of BNCs for both analog and digital I/O and is printed on the face of the device to minimize miswiring.

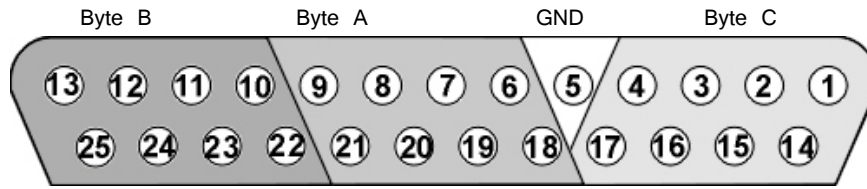


DB25 Analog I/O Pinout



Pin	Name	Description	Pin	Name	Description
1	NA	Not Used	14	NA	Not Used
2			15		
3			16		
4			17		
5	AGND	Analog Ground	18	A1	ADC
6	A2	ADC	19	A3	Analog Input Channels
7	A4	Analog Input Channels	20	NA	Not Used
8	NA	Not Used	21	NA	
9	NA		22	A9	DAC
10	A10	DAC	23	A11	Analog output Channels
11	A12	Analog Output Channels	24	NA	Not Used
12	NA	Not Used	25	NA	
13	NA				

DB25 Digital I/O Pinout



Pin	Name	Description	Pin	Name	Description
1	C0	Byte C	14	C1	Byte C
2	C2	Bit Addressable Digital I/O	15	C3	Bit Addressable Digital I/O
3	C4	Bits 0, 2, 4, and 6	16	C5	Bits 1, 3, 5, and 7
4	C6		17	C7	
5	GND	Digital I/O Ground	18	A0	Byte A
6	A1	Byte A	19	A2	Word Addressable Digital I/O Bits 0, 2, 4 and 6
7	A3	Word Addressable Digital I/O Bits 1, 3, 5 and 7	20	A4	
8	A5		21	A6	
9	A7		22	B0	Byte B
10	B1	Byte B	23	B2	Word Addressable Digital I/O Bits 0, 2, 4 and 6
11	B3	Word Addressable Digital I/O Bits 1, 3, 5 and 7	24	B4	
12	B5		25	B6	
13	B7				

