RZ5D BioAmp Processor

RZ5D Overview

The RZ5D BioAmp Processor is available with either three or four digital signal processors cards. Any card can be either a single standard processor card (RZDSP) or a quad core processor card (QZDSP). Standard single processor cards use a single Sharc DSP; quad-core processor cards use four Sharc DSPs cores with the potential to more than double the power of the RZ5D. All cards are networked on a multiprocessor architecture that features efficient onboard communication and memory access. The RZ5D is a versatile solution for real-time processing and simultaneous acquisition and stimulation.

The RZ5D acquires and processes up to 32 channels of neurophysiological signals in real-time. Data can be input from a PZ amplifier or digital headstage manifold at a sampling rate of up to ~50 kHz. The RZ5D also supports microstimulation applications. The RZ5D can be used with TDT's IZ2 stimulus isolator for up to 128 channels of stimulation and switching headstages (SH16-Z) to comprise a complete microstimulation system. For more information, see "IZ2/IZ2H Stimulator" on page 7-3.

Both single and quad-core processors cards may include an optical interface for connection to devices such as the RS4 Data Streamer or a second PZ Amplifier.

The RZ5D also features eight channels of analog I/O, 24 bits of digital I/O and an onboard monitor speaker with volume control.

Power and Communication

The RZ5D's integrated Optibit optical interface ensures fast and reliable data transfer from the RZ5D to the PC. Connectors are provided on the back panel and are color coded for correct wiring. The RZ5D's integrated power supply is shipped from the factory configured for the desired voltage setting (110 V or 220 V). If you need to change the voltage setting, please contact TDT support at +1.386.462.9622 or email support@tdt.com.

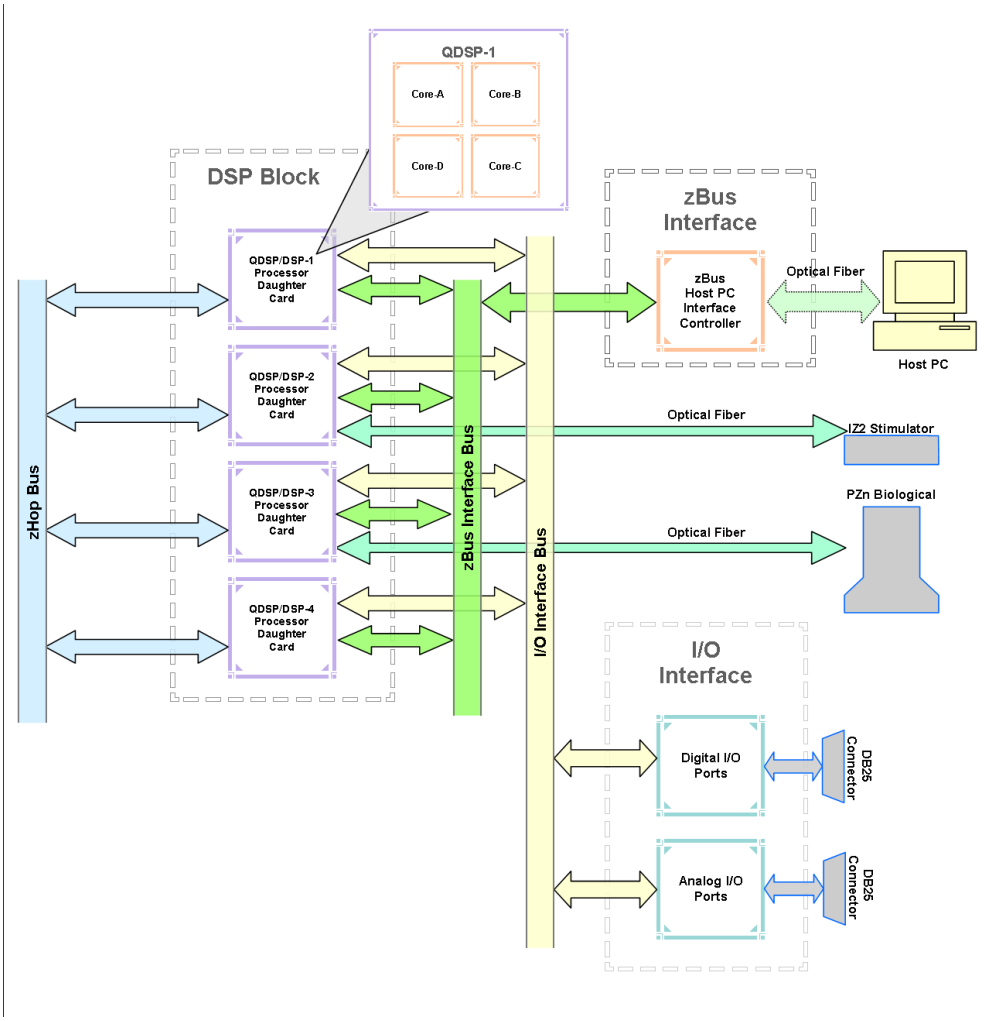
The RZ5D is UL compliant, see the *RZ5/RZ5D/RZ6 Operations Manual* for power and safety information.

Software Control

TDT Synapse software controls the RZ5D and provides users a high level interface for device configuration. Device programming is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed to design circuit. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RZ5D Architecture

The RZ5D processor utilizes a multi-bus architecture and offers four dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



RZ5D Multi-DSP Architecture Functional Diagram

As shown in the diagram above, the RZ5D architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP Block is connected to a local interface to the three data buses: two buses that connect each DSP to the other functional blocks and one that handles data transfer between the DSPs (as described further in "Distributing Data Across DSPs" below). Each standard DSP is connected to 64 MB SDRAM and each core in a QZDSP is connected to 256 MB DDR2. This architecture facilitates fast DSP-to-off-chip data handling.

Because each DSP has its own associated memory, access is very fast and efficient. However, large and complex circuits should be designed to balance memory needs (such as data buffers and filter coefficients) across processors.

When designing circuits also note that the maximum number of components for each RZ5D standard RZDSP is 768 and 1000 for each QZDSP.

DSP-2 and DSP-3 are special optical DSPs. These DSPs have a direct fiber optic connection to the IZ and PZ interface port, respectively.

The zBus Interface

The zBus interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus interface bus, allowing for large high-speed data reads and writes without interfering with other system processing.

The I/O Interface

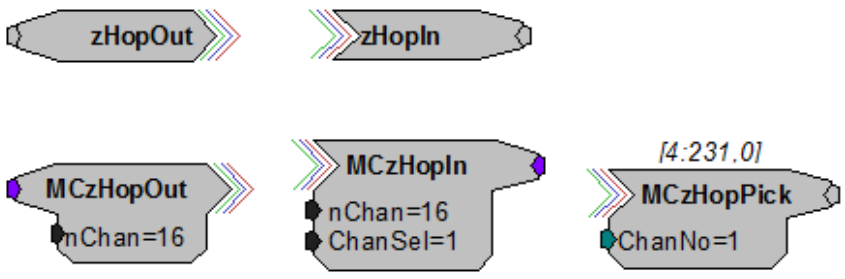
The I/O interface serves as a connection to outside signal sources or output devices. It is used to input data from the preamplifier inputs and digital and analog channels. The I/O interface bus provides a direct connection to each DSP.

Distributing Data Across DSPs

To reap the benefits of added power made possible by multi-DSP modules, processing tasks must be efficiently distributed across the available DSPs. That means transferring data across DSPs (or among cores of a quad-core DSP). The RZ5D architecture provides the zHop bus for inter-DSP data handling.

The zHop Bus

The zHop bus allows the transfer of single or multi-channel signals between each DSP in the RZ5D.



In RPvdsEx data is transferred across the zHop bus using paired zHop components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

The zHop bus introduces a two sample delay However, this delay is taken care of for the user in Synapse and in OpenEx (when Timing and Data Saving macros are used).

RZ5D Features

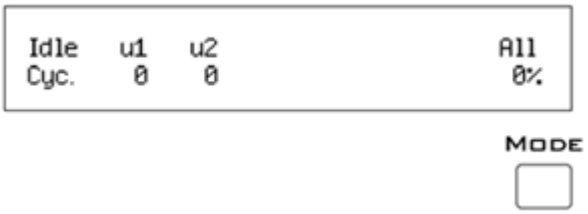
DSP Status Displays

The RZ5D include status lights and a VFD (Vacuum Fluorescent Display) screen to report the status of the individual processors.

Status Lights

Two LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The corresponding LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second). For QZDSPs, the LED indicates levels for the core with the highest cycle usage.

Front Panel VFD Screen



The front panel VFD screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The VFD screen may also report system status such as booting status (Reset).

Note: When burning new microcode or if the firmware on the RZ5D is blank, the VFD screen will report a cycle usage of 99% and the processor status lights will flash red.

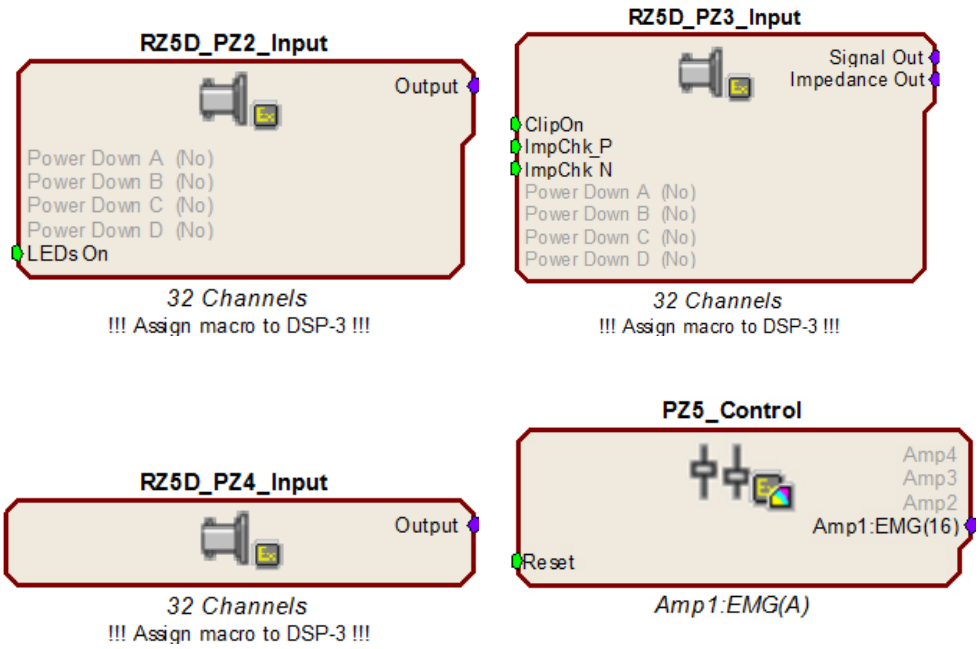
Status Indicators	Description
Cyc:	cycle usage (note: limited to 2 digits; ex: 110 displayed as 10) for QZDSPs, the highest core cycle usage is shown
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
Opt:	connection (sync) status of amplifiers A and B

Important! The status lights flash when a DSP goes over the cycle usage limit, even if only for a particular cycle. This helps identify periodic overages caused by components in time slices.

PZ Preamplifier Port

The RZ5D acquires digitized signals from a PZ preamplifier or digital headstage manifold over a fiber optic cable through the port labeled 'PZ' on the front panel. This port can input up to 32 channels at a maximum sampling rate of ~50 kHz. The PZ port can be used with any of the PZ preamplifiers including the PZ2, PZ3, and PZ5 or the PZ4 digital headstage manifold. The PZ5_Control and RZ5D_PZn_Input macros are used to access neurophysiological data in the processing chain.

Important! The macro must be placed on DSP-3 in the RPvdsEx circuit. Further, when using the RZ5D, set the *Use Direct Input* option on the PZ5_Control Setup tab to *Yes*. See the internal macro help for more details.



IZ Stimulator Port

The output port labeled IZ can be used to transfer microstimulation waveforms to the IZ2 Stimulator and/or to control an attached SH16-Z switching headstage. This port can output up to 128 channels of stimulation at a maximum sampling rate of ~50 kHz.

The IZ2_Control macro is used to send stimulation waveforms, control an optional SH16-Z, and receive monitor information from the IZ2.

Important! The IZ2_Control macro must be placed on DSP-2 in the RPvdsEx circuit. See the internal macro help for more details.

Voltage Stim Mode (32 ch)

Onboard Analog I/O

The RZ5D is equipped with four channels of 16-bit PCM D/A and four channels of 16-bit PCM A/D. All 8 channels can be accessed via front panel BNCs marked A and DAC or via a 25-pin analog I/O connector. See "RZ5D Technical Specifications" on page 1-24 for the DB25 pinout.

The following table provides a quick overview of the analog I/O features and how they must be accessed during circuit design. See the *RPvdsEx Manual* for more information on circuit design.

Analog I/O	Description	Components	Chan.	Notes
ADC Inputs	Analog Input	ADCIn	1 - 4	Accessed through A Input BNCs or Analog I/O labeled DB25
DAC Outputs	Analog Output	DacOut	9 - 12	Accessed through DAC Output BNCs or Analog I/O labeled DB25

Monitor Speaker

The RZ5 is equipped with an onboard speaker. To use the speaker, feed the desired signal to output channel 9 using a DacOut component. The speaker is provided primarily for audio monitoring of a single channel of electrophysiological potentials during recording.

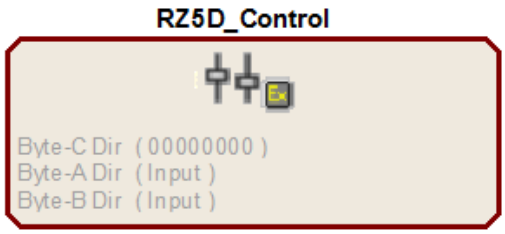
Digital I/O

24 bits of programmable digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ5D and bits 0 - 3 of byte C are available through BNC connectors on the front panel labeled Digital. See "RZ5D Technical Specifications" on page 1-24, for the DB25 pinout and BNC channel mapping.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable
*Note: Byte C Bits 0 - 3 are available via front panel BNCs				

By default, all digital I/O are configured as inputs. The data direction for the Digital I/O is configured using the RZ5D_Control macro in RPvdsEx. Double-click the macro to access the settings on the Digital I/O tab. The RZ5_Control macro also offers a Direction Control Mode parameter that enables the macro inputs and allows the user to control data direction dynamically. For more information on using the RZ5D_Control macro see the help provided in the macro's properties dialog box. For more information on addressing and Digital I/O see the *RPvdsEx Manual*.



The RZ digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table listing the different voltage outputs and thresholds for both types.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

LED Indicators

The RZ5D contains 16 LED indicators for the analog and digital I/O. These indicators are located directly below the VFD and DSP status LEDs. They display information relative to the various analog and digital I/O. The following tables list the possible display options and their associated descriptions.

Digital I/O

These LEDs indicate the state of the 8 bit-addressable I/O of byte C.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog I/O

These LEDs indicate the state of the four ADC and four DAC channels.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than +/-100 mV
Dim Green	Analog I/O channel signal voltage is less than +/-5 V
Solid Green	Analog I/O channel signal voltage is between +/-5 V to +/-9 V
Solid Red	Analog I/O channel clip warning (voltage greater than +/-9 V)

UDP Ethernet Interface (Optional)

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP Communications Interface" on page 1-51, for more information.

RZ5D Technical Specifications

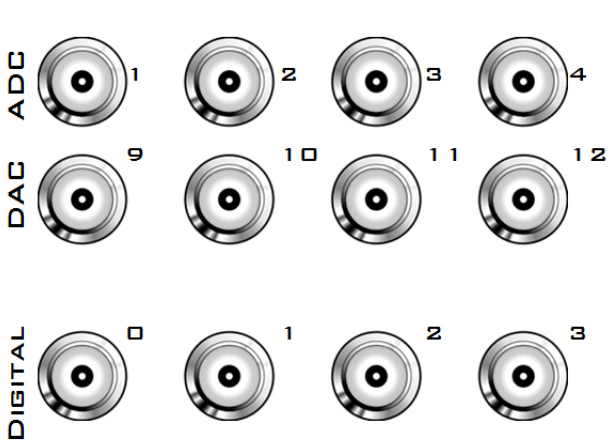
Note: Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

DSP	Three or four standard DSPs and/or quad-core (QZDSP) DSP: 400 MHz DSPs, 2.4 GFLOPS peak per DSP QZDSP: four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per QZDSP core
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)

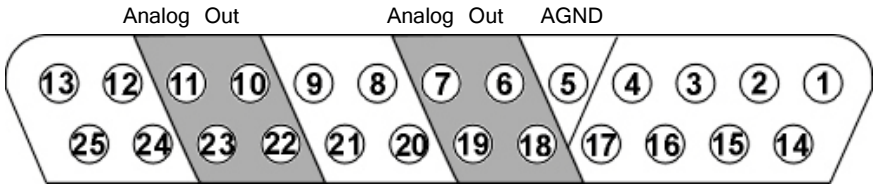
Output Impedance	10 Ohms
A/D	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Ports	
Stimulator (IZ2)	One output for IZ2, up to 128 channels
Preamplifier (PZ)	One input for PZ5, PZ2, PZ3 or PZ4
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes (16 bits): 5.0 V, 35 mA max load

BNC Channel Mapping

Please note channel numbering begins at the top left block of BNCs for both analog and digital I/O and is printed on the face of the device to minimize miswiring.

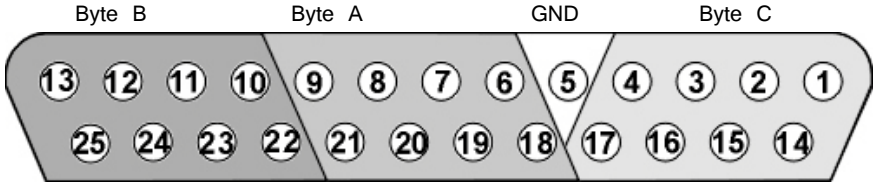


DB25 Analog I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	AGND	Analog Ground		18	A1	ADC Analog Input Channels
6	A2	ADC Analog Input Channels		19	A3	
7	A4			20	NA	Not Used
8	NA	Not Used		21	NA	
9	NA			22	A9	DAC Analog Output Channels
10	A10	DAC Analog Output Channels		23	A11	
11	A12			24	NA	Not Used
12	NA	Not Used		25	NA	
13	NA					

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable Digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Byte A Word Addressable Digital I/O Bits 1, 3, 5 and 7		19	A2	
7	A3			20	A4	
8	A5			21	A4	
9	A7			22	B0	Byte B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Byte B Word Addressable Digital I/O Bits 1, 3, 5 and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					