System 3 Manual

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Warranty
TDT System 3 hardware* carries a five-year warranty on parts and labor. Contact TDT to obtain an RMA (return merchandise authorization) number before returning any hardware.

* Custom hardware carries a one-year warranty on parts and labor. All headstages, the ES1 and the EC1 carry a two year warranty.

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RZ2 BioAmp Processor

RZ2 Overview

The RZ2 BioAmp Processor has been designed for high channel count neurophysiology recording and signal processing. The RZ2 features two (RZ2-2), four (RZ2-4), or eight (RZ2-8) digital signal processors cards. Any card can be either a single standard processor card (RZDSP) or a quad-core processor card (QZDSP). Standard single processor cards use a single Sharc DSP; quad-core processor cards use four Sharc DSPs Cores with the potential to more than double the power of the RZ2. All cards are networked on a multiprocessor architecture that features efficient onboard communication and memory access. The highly optimized multi-bus architecture uses four dedicated data buses to eliminate data flow bottlenecks—all transparent to the user. This architecture yields an extremely powerful system capable of sophisticated real-time processing and simultaneous acquisition on all channels.

The RZ2 is typically used with a Z-Series Amplifier (such as the PZ5). High bandwidth data is streamed from the amplifier to the RZ2 over a lossless, fast, fiber optic connection. Both single and quad-core processors cards may include an optical interface for connection to devices such as the RS4 Data Streamer, an IZ2 Stimulator or a secondary PZ Amplifier. Each onboard optical connection can support 256 channels at sampling rates up to ~25 kHz and 128 channels at sampling rates up to ~50 kHz. The RZ2 also features 16 channels of analog I/O, 24 bits of digital I/O, two Legacy optical inputs for Medusa PreAmps, and an onboard LCD for system status display.

Power and Communication

The RZ2's Optibit optical interface ensures fast and reliable data transfer from the RZ2 to the PC and is integrated into the device. Connectors are provided on the back panel and are color coded for correct wiring. The RZ2's power supply is also integrated into the device and is shipped from the factory configured for the desired voltage setting (110 V or 220 V). If you need to change the voltage setting, please contact TDT support at +1.386.462.9622 or email support@tdt.com.

The RZ2 is UL compliant, see the *RZ2 Operations Manual* for power and safety information.

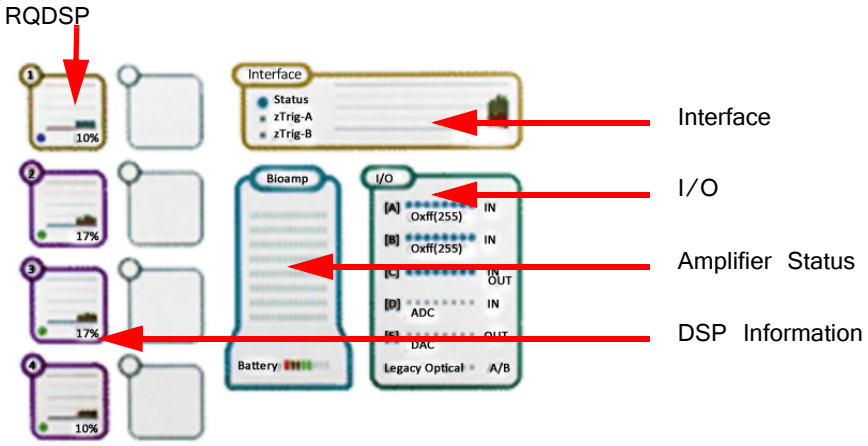
Software Control

TDT *Synapse* software controls the RZ2 and provides users a high level interface for device configuration.

Device programming is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed for designing circuits. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RZ2 TouchScreen

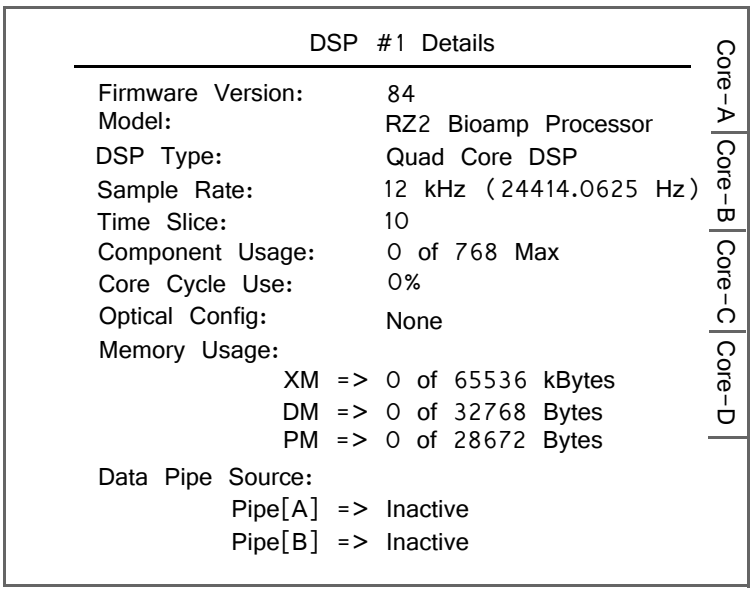
The touchscreen shows information about each DSP, the optical PC interface, a connected PZ preamplifier, and system I/O.



Touch a section of the screen to display more detailed information.

Screen Element	Information Displayed
DSPs	A stacked histogram shows cycle usage for each DSP with the bottom section (blue) showing the cycle usage taken up by circuit operation and the top section (pink) showing the cycle usage required for data transfer. If the cycle usage surpasses 100%, a bar is drawn above the 100% line in the cycle use histogram and will persist until the RZ2 is rebooted. For quad-core DSPs, the core with the highest cycle usage is displayed.

Touch to Display:



Optical Config is the peripheral device supported by the DSP, if any.

Data memory (DM) is the amount of DM used for filter delay line and short delays.

External Memory (XM) is the amount of XM used for long delays and buffers.

Program Memory (PM) is the amount of PM used to hold filter coefficients.

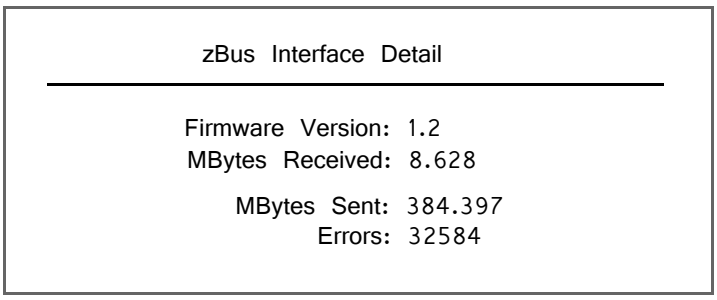
Tabs are enabled for quad-core DSPs, with one Core per tab.

Interface

Virtual Status lights display status of the interface (Status), zTrig-A, and zTrig-B. A stacked histogram shows data transfer rate in mb/s.

Touch to Display:

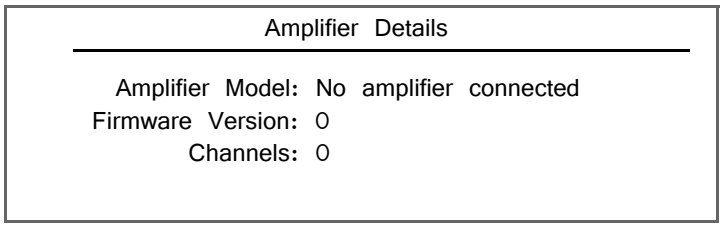
Firmware version, MB data received/sent and transfer errors.



Amp

Touch to Display:

Amp model, number of channels and firmware version of connected PZ series amplifier.



I/O Virtual indicator lights.

[A], [B], and [C]: Digital I/O

LED will light for an input bit or it will show the logic level for an output bit.

[D] and [E]: Analog I/O

16 lights indicate the signal level, green when a signal is present and red to warn that the signal is approaching the maximum voltage (at which point clipping would occur).

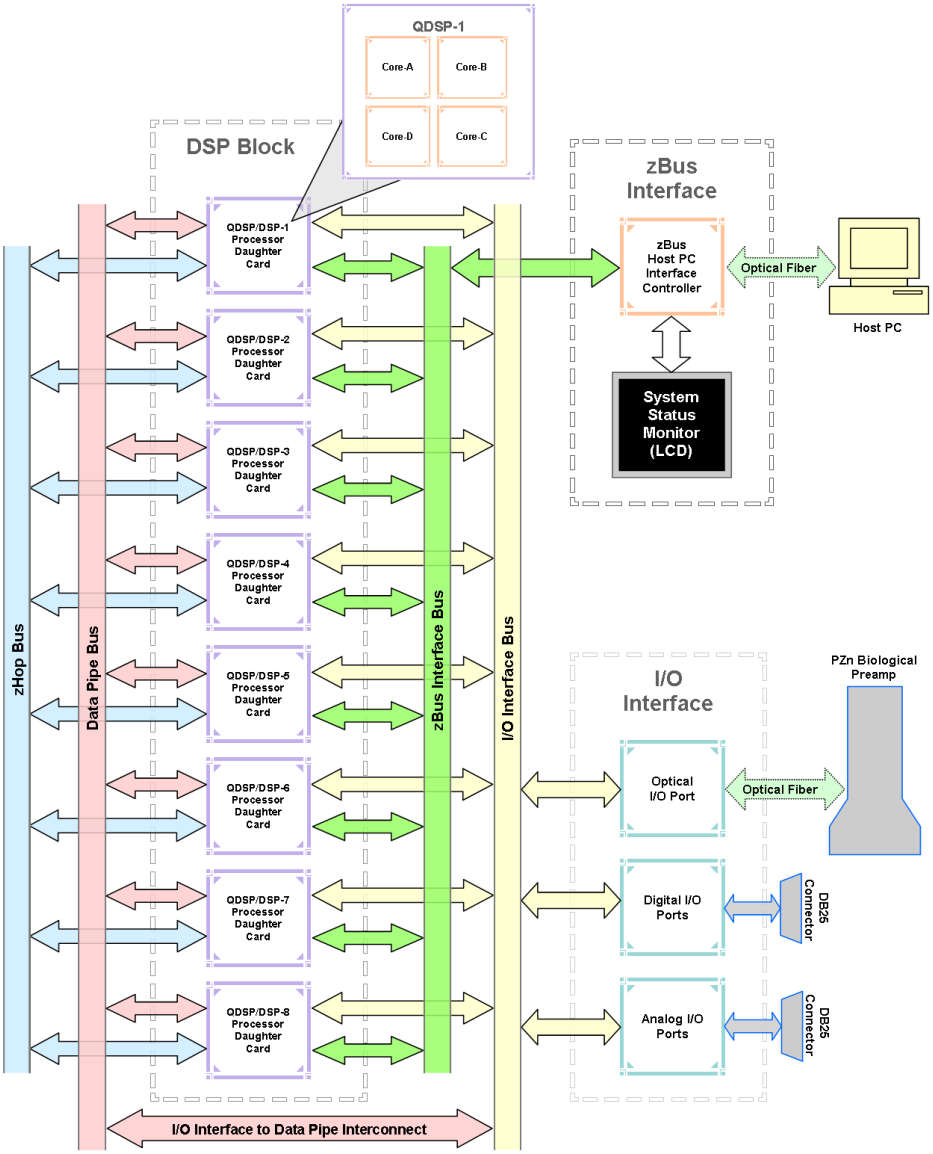
Legacy Optical: Amp Light For The Legacy Preamplifier Sync

Flashes yellow when no amp is connected and will be light green when the amplifier is correctly connected.

Note: Older versions of the RZ2 have a selection knob that allows the user to highlight a section of the screen. To display more detailed information, rotate the knob to select a system component and then push the knob to show the information view.

RZ2 Architecture

The RZ2 processor utilizes a highly optimized multi-bus architecture and offers four dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



RZ2 Multi-DSP Architecture Functional Diagram

As shown in the diagram above, the RZ2 architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP Block is connected to a local interface to the four data buses: two buses that connect each DSP to the other functional blocks and two that handle data transfer between the DSPs (as described further in Distributing Data Across DSPs below). Each standard DSP is connected to 64 MB SDRAM and each core in a QZDSP is connected to 256 MB DDR2. This architecture facilitates fast DSP-to-off-chip data handling.

Because each DSP has its own associated memory, access is very fast and efficient. However, large and complex circuits should be designed to balance memory needs (such

as data buffers and filter coefficients) across processors. Memory use can be monitored on the RZ2 front panel display.

When designing circuits also note that the maximum number of components for each RZ2 standard RZDSP is 768 and 1000 for each QZDSP.

The zBus Interface

The zBus interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus Interface Bus, allowing for large high-speed data reads and writes without interfering with other system processing.

The I/O Interface

The I/O interface serves as a connection to outside signal sources or output devices. It is used primarily to input data from a PZ amplifier via the high speed optical port, but also serves the Legacy amplifier inputs and digital and analog channels. The I/O Interface Bus provides a direct connection to each DSP and the Data Pipe Bus.

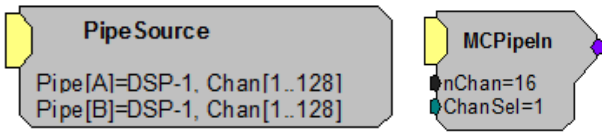
Distributing Data Across DSPs

For the best performance, processing tasks must be efficiently distributed across the available DSPs. That means transferring data across DSPs. The RZ2 architecture provides three data buses for this type of data handling.

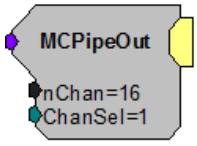
The Data Pipe Bus

The Data Pipe bus is optimized for handling high count multi-channel data streams and efficiently transfers up to 256 channels of data between DSPs. The Data Pipe bus also interconnects to the I/O Interface bus allowing direct access to data from the PZ amplifiers.

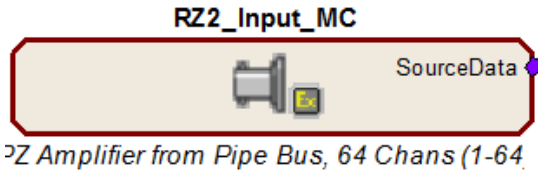
In RPvdsEx data can be transferred across the Data Pipe bus using Data Pipe components.



PipeSource and MCPipeIn components are used to select a data source (another DSP or the PZ amplifier) and feed data to a DSP circuit.



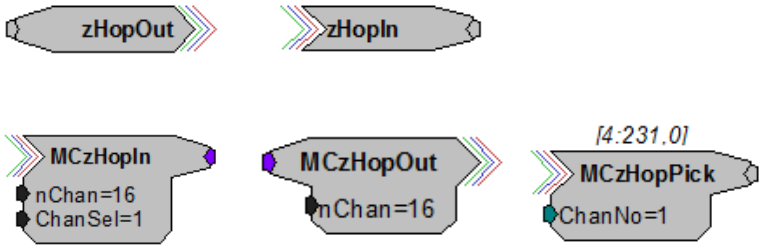
MCPipeOut feeds data off the DSP to the Data Pipe Bus.



The RZ2_Input_MC macro also transfers inputs from the I/O interface to the Data Pipe bus and DSPs.

The zHop Bus

The zHop bus is useful for transferring single or low channel count signals, such as timing and control signals.



In RPvdsEx data is transferred across the zHop Bus using paired zHop components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. These components can be used on any DSP or DSP-core. Up to 126 pairs can be used in a single RPvdsEx circuit.

The zHopBus is less efficient than the Data Pipe bus, so it is not recommended for multi-channel signals.

Bus Related Delays

A standard two sample delay is associated with the zHop, and Data Pipe. However, these delays are taken care of for the user in Synapse and when Timing and Data Saving macros are used in OpenEx.

50 kHz Sampling Rate Acquisition with the PZ Amplifier

The RZ2 and PZ amplifier support sample rates from ~6 kHz to ~50 kHz.

When sampling at a rate of ~50 kHz, there are several important considerations:

- Only the first 128 PZ amplifier channels will be available.
- All Data Pipes will have a max of 128 channels instead of 256.
- Both halves (A and B) of the PipeSource component must be selecting the desired source. For example, when acquiring data from a PZ amplifier, Pipe[A] and Pipe[B] both need to be set to Amp. Chan[1...128].

Data Transfer Rate

As with other devices, your expected sustained RZ-to-Host PC data rate should not exceed 1/2 to 2/3 of the rated data transfer speed. For the RZ2 device this is 160 Mbits/second (Mbps) so your designs should have a sustained data rate of no

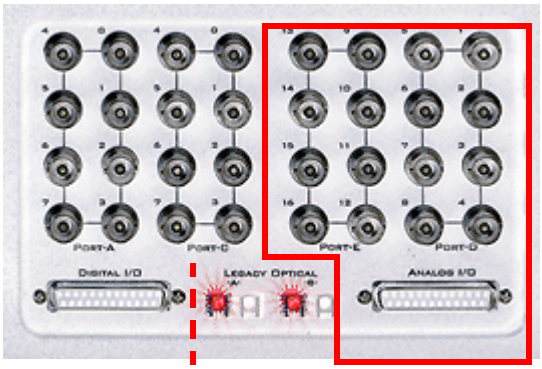
more than ~100 Mbps. When the RZ2 is processing, the current data transfer rate (Mbps) is displayed in the top right corner of the LCD Screen. This maximum rate may be further limited by your PC's ability to store the data to disk.

This equates to streaming a maximum of 160 channels at a sampling rate of ~25 kHz or 90 channels at a sampling rate of ~50 kHz. See "Calculating Data Transfer Rates" in the *OpenEx Manual* for more information.

RZ2 Features

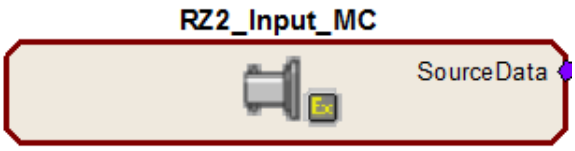
Amplifier and Onboard Analog I/O

The RZ2 is equipped with both optical port amplifier input and onboard analog I/O capabilities. The high speed fiber optic ports (located on the RZ2 back panel) and Legacy fiber optic ports allow a direct connection to Z-Series or Medusa preamplifiers. Physiological signals are digitized on the preamplifier and transferred across noiseless fiber optics.



Legacy PreAmp Input Analog I/O

The RZ2 also includes onboard D/A for stimulus generation and experiment control, and A/D for input of signals from a variety of other analog sources.



Data Pipe, 16 Chans (1-16)

The RZ2_Input_MC macro provides a universal solution for analog input via the RZ2, automatically selecting the correct components, applying any scale factors or channel offsets, and performing data type conversion needed based on information the user provides about the input source.

The table below provides a quick overview of these I/O features and how they must be accessed during circuit design. When the RZ2_Input_MC macro is not used, reference the table and be sure to use the appropriate component, channel offset,

scale factor and so forth. Further detail can be found below the table. Also, see the *RPvdsEx Manual* for more information.

Analog I/O	Description	Components	Chan.	Notes
Port D	Analog Input	AdcIn	1-8	Standard Configuration (may vary) Accessed through Port D BNCs or Analog I/O labeled DB25
Port E	Analog Output	DacOut	9-16	Standard Configuration (may vary) Accessed through Port E BNCs or Analog I/O labeled DB25
High Speed Fiber Optic Port	Z-Series BioAmp Input (located on RZ back panel)	MCPipeIn PipeIn recommended	1-256	When the RZ2_Input_MC is NOT USED, use MCInt2Float or Int2Float with a scale factor of 1e-9
		MCAdcIn	1-256	No scale required
Legacy Amp-A	Medusa PreAmp Input	AdcIn	17-32	When the RZ2_Input_MC is NOT USED, apply a scale factor of .000833
Legacy Amp-B	Medusa PreAmp Input	AdcIn	33-48	When the RZ2_Input_MC is NOT USED, apply a scale factor of .000833

Onboard Analog I/O

The RZ2 is equipped with eight channels of 16-bit PCM D/A and eight channels of 16-bit PCM A/D. All 16 channels can be accessed via front panel BNCs marked Port D and Port E or via a 25-pin analog I/O connector. See "RZ2 Technical Specifications" on page 1-14, for the DB25 pinout.

PZ Amplifier Fiber Optic Port

The RZ2's primary amplifier input, a high-speed fiber optic port is located on the back panel. The connectors on the fiber optic pair used for PZ amplifier communication are color coded for correct wiring. When designing circuits in RPvdsEx, the PZ amplifier input channels are accessed using the Pipe components. When the Data Pipe is used to feed signals from the amplifier an MCInt2Float or Int2Float must be used with a scale factor of 1e-9.

The amplifier inputs can also be accessed using the RPvdsEx MCAIn component starting at channel 1; however, this access method is less efficient and not recommended for high channel count applications. Unlike the Legacy Port, this high speed port can input up to 256 channels at a maximum sampling rate of 25 kHz or 128 channels at a maximum sampling rate of 50 kHz.

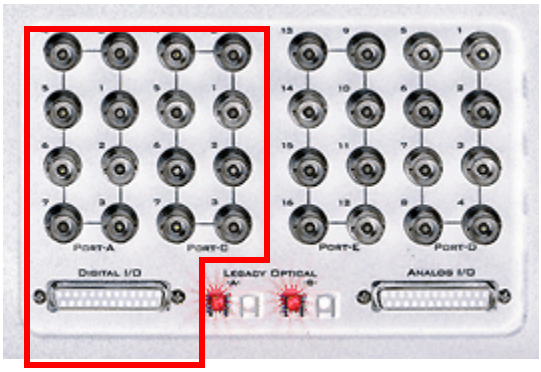
Legacy Fiber Optic Ports

The base station can also acquire digitized signals from the Medusa preamplifier, RA8GA, or other legacy enabled device over a fiber optic cable using the Legacy ports. Two Legacy fiber optic ports labeled -A- and -B- are provided to support simultaneous acquisition from up to two Medusa preamplifiers. Each port can input up

to 16 channels at a maximum sampling rate of 25 kHz. The Legacy fiber optic ports can be used with any of the Medusa preamplifiers including, the RA16PA, the RA4PA, or the RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Digital I/O

The digital I/O ports include 24 bits of programmable I/O. The digital I/O is divided into three ports (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ2 and ports A and C are available through BNC connectors on the front panel.



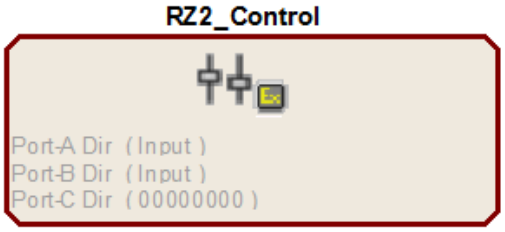
Digital I/O

See "RZ2 Technical Specifications" on page 1-14, for the DB25 pinout and BNC channel mapping.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

Digital I/O	Description	DB25	BNCs	Notes
Port A	bits 0 - 7	Yes	Yes	byte addressable
Port B	bits 0 - 7	Yes	No	byte addressable
Port C	bits 0 - 7	Yes	Yes	bit addressable

The data direction for the Digital I/O is configured using the RZ2_Control macro in RPvdsEx.



Double-click the macro to access the settings on the Digital I/O tab. The RZ2_Control macro also offers a Direction Control Mode parameter that enables the macro inputs and allows the user to control data direction dynamically. For more information on using the RZ2_Control macro see the help provided in the macro's properties dialog box.

Note: For more information on addressing and Digital I/O see the *RPvdsEx Manual*.

The RZ digital I/O ports have different voltage outputs and logic thresholds depending on the type. The table below depicts the different voltage outputs and thresholds for both types.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

UDP Ethernet Interface

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP Communications Interface" on page 1-51, for more information.

Note: If the RZ2 has 4 optical DSP cards (see below) installed, the UDP Serial port is not available.

Specialized DSP/Optical Interface Boards (Optional)

The RZ standard DSP boards can be replaced with specialized DSP boards which include an optical interface for communication and control of RZ compatible devices, such as the IZ2 Stimulator and RS4 Data Streamer. RZ devices equipped with one or more specialized DSP boards include an optical port for each card. The ports are located on the back panel and labeled for easy identification.

RZDSP-I This board supports the IZ2 Stimulator, allowing the RZ device to function as a controller or base station. See "Software Control" on page 8-11, for more information on using and designing circuits for the stimulator.

RZDSP-M This board supports the SI Subject Interface, for reading analog and digital amplifier signals, and controlling analog stimulation. See "RS4 Data Streamer" on page 2-3, for more information on using the Subject Interface.

RZDSP-P This board supports PZ amplifier input, providing an alternate method for acquiring data from a PZ amplifier. It can be used to expand the number of channels that can be acquired on any RZ processor. Access to this input can be enabled in the PZ control macro.

RZDSP-S This board supports the RS4 Data Streamer, allowing the RZ device to stream data directly to the RS4's storage arrays. See "RS4 Data Streamer" on page 2-3, for more information on using and designing circuits for the streamer.

RZDSP-U This board supports the PO8e interface card, allowing the RZ device to stream data directly to storage arrays on a PC or other device. See "PO8e Streaming Interface for the RZ" on page 2-27, for more information.

RZDSP-V This board supports the RV2 Video Tracking System, allowing the RZ device to function as a controller or base station. See “RV2 Video Processor” on page 9-3, for more information on using and designing circuits for the RV2.

QZDSP_OPT This version of the QZDSP quad-core processor includes an optical interface that can be programmed for use with any of the RZ compatible devices, such as a secondary PZ Amp, the IZ2 Stimulator, and RS4 Data Streamer. Core-A is always used for control of the peripheral device.

RZ2 Technical Specifications

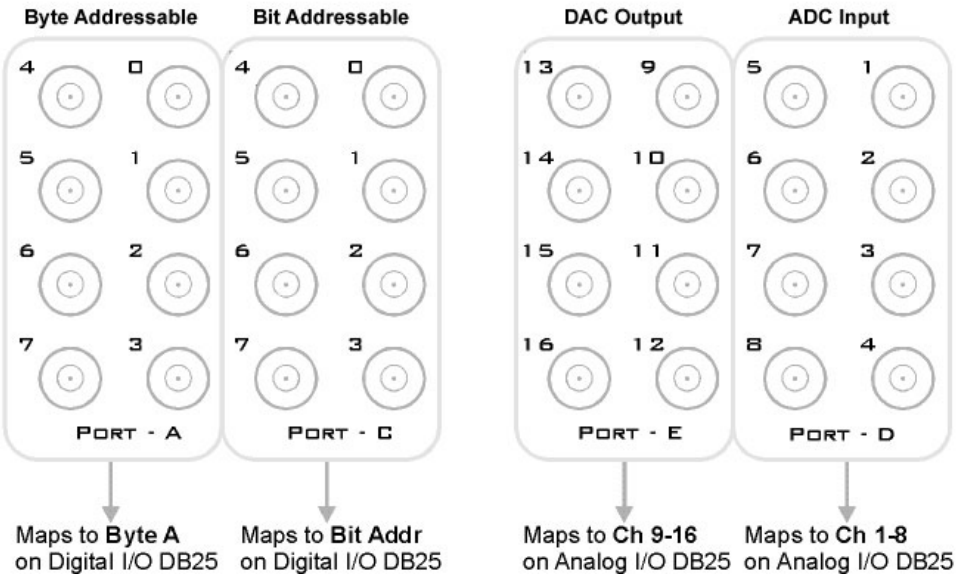
Note: Technical specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

DSP	Up to eight standard DSPs and/or quad-core (QZDSP) DSP: 400 MHz DSPs, 2.4 GFLOPS peak per DSP QZDSP: Four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per core, four cores per QZDSP
D/A	8 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	10 Ohms
A/D	8 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Ports	

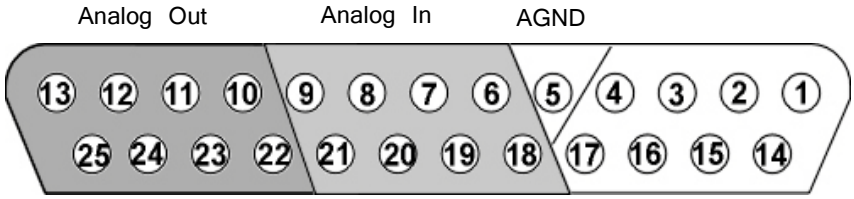
Z-Series	One 256-channel input The maximum sample rate is 48828.125 Hz when recording up to 128 channels or 24414.0625 Hz when recording 129 - 256 channels).
Legacy (Medusa)	Two 16-channel inputs
Add-on Specialty (Optional)	Up to four, one per QZDSP_Opt or Specialty DSP card upgrade.
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes (16 bits): 5.0 V, 35 mA max load

BNC Channel Mapping

Please note channel numbering begins at the top right block of BNCs for each port and is printed on the face of the device to minimize miswiring. The figure below represents the standard configuration and may vary depending on customer request.

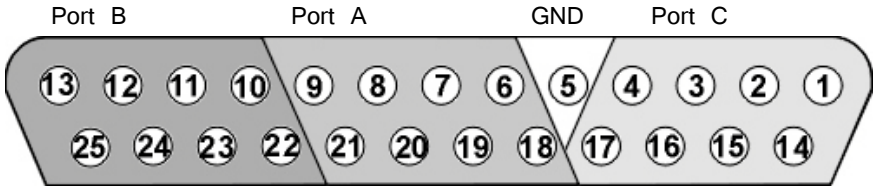


DB25 Analog I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	AGND	Analog Ground		18	A1	A Analog Input Channels (Port D)
6	A2	A Analog Input Channels (Port D)		19	A3	
7	A4			20	A5	
8	A6			21	A7	
9	A8			22	A9	DAC Analog Output Channels (Port E)
10	A10	DAC Analog Output Channels (Port E)		23	A11	
11	A12			24	A13	
12	A14			25	A15	
13	A16					

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Port C Bit Addressable Digital I/O Bits 0, 2, 4, and 6		14	C1	Port C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Port A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Port A Word Addressable Digital I/O Bits 1, 3, 5 and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Port B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Port B Word Addressable Digital I/O Bits 1, 3, 5 and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

RZ5D BioAmp Processor

RZ5D Overview

The RZ5D BioAmp Processor is available with either three or four digital signal processors cards. Any card can be either a single standard processor card (RZDSP) or a quad core processor card (QZDSP). Standard single processor cards use a single Sharc DSP; quad-core processor cards use four Sharc DSPs cores with the potential to more than double the power of the RZ5D. All cards are networked on a multiprocessor architecture that features efficient onboard communication and memory access. The RZ5D is a versatile solution for real-time processing and simultaneous acquisition and stimulation.

The RZ5D acquires and processes up to 32 channels of neurophysiological signals in real-time. Data can be input from a PZ amplifier or digital headstage manifold at a sampling rate of up to ~50 kHz. The RZ5D also supports microstimulation applications. The RZ5D can be used with TDT's IZ2 stimulus isolator for up to 128 channels of stimulation and switching headstages (SH16-Z) to comprise a complete microstimulation system. For more information, see "IZ2/IZ2H Stimulator" on page 8-3.

Both single and quad-core processors cards may include an optical interface for connection to devices such as the RS4 Data Streamer or a second PZ Amplifier.

The RZ5D also features eight channels of analog I/O, 24 bits of digital I/O and an onboard monitor speaker with volume control.

Power and Communication

The RZ5D's integrated Optibit optical interface ensures fast and reliable data transfer from the RZ5D to the PC. Connectors are provided on the back panel and are color coded for correct wiring. The RZ5D's integrated power supply is shipped from the factory configured for the desired voltage setting (110 V or 220 V). If you need to change the voltage setting, please contact TDT support at +1.386.462.9622 or email support@tdt.com.

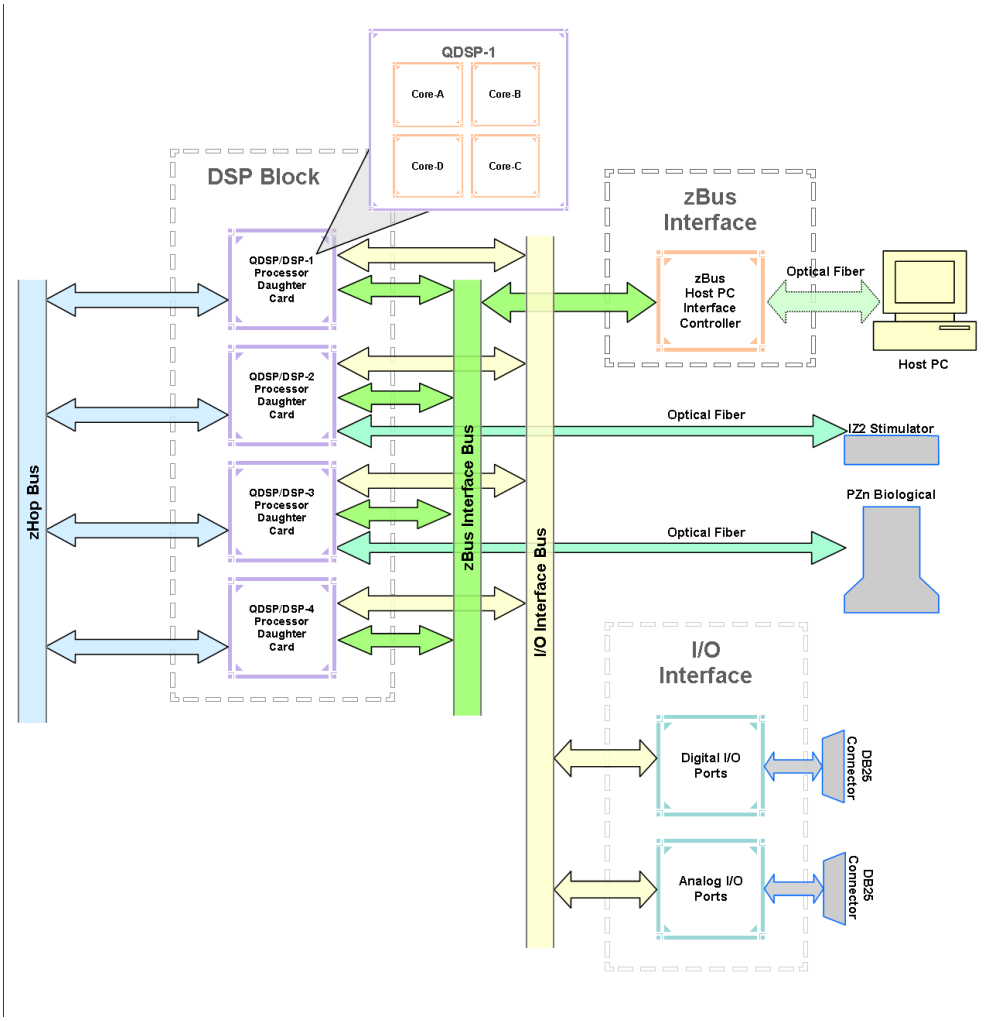
The RZ5D is UL compliant, see the *RZ5/RZ5D/RZ6 Operations Manual* for power and safety information.

Software Control

TDT Synapse software controls the RZ5D and provides users a high level interface for device configuration. Device programming is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed to design circuit. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RZ5D Architecture

The RZ5D processor utilizes a multi-bus architecture and offers four dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



RZ5D Multi-DSP Architecture Functional Diagram

As shown in the diagram above, the RZ5D architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP Block is connected to a local interface to the three data buses: two buses that connect each DSP to the other functional blocks and one that handles data transfer between the DSPs (as described further in "Distributing Data Across DSPs" below). Each standard DSP is connected to 64 MB SDRAM and each core in a QZDSP is connected to 256 MB DDR2. This architecture facilitates fast DSP-to-off-chip data handling.

Because each DSP has its own associated memory, access is very fast and efficient. However, large and complex circuits should be designed to balance memory needs (such as data buffers and filter coefficients) across processors.

When designing circuits also note that the maximum number of components for each RZ5D standard RZDSP is 768 and 1000 for each QZDSP.

DSP-2 and DSP-3 are special optical DSPs. These DSPs have a direct fiber optic connection to the IZ and PZ interface port, respectively.

The zBus Interface

The zBus interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus interface bus, allowing for large high-speed data reads and writes without interfering with other system processing.

The I/O Interface

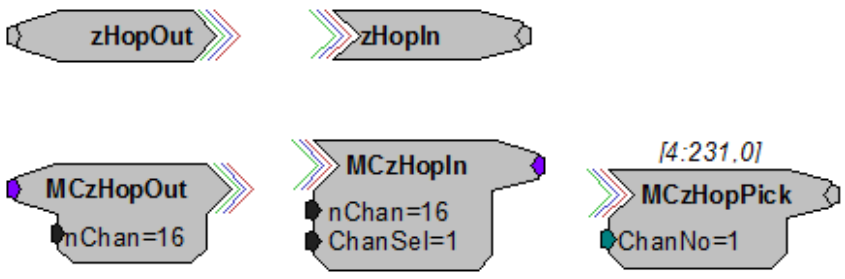
The I/O interface serves as a connection to outside signal sources or output devices. It is used to input data from the preamplifier inputs and digital and analog channels. The I/O interface bus provides a direct connection to each DSP.

Distributing Data Across DSPs

To reap the benefits of added power made possible by multi-DSP modules, processing tasks must be efficiently distributed across the available DSPs. That means transferring data across DSPs (or among cores of a quad-core DSP). The RZ5D architecture provides the zHop bus for inter-DSP data handling.

The zHop Bus

The zHop bus allows the transfer of single or multi-channel signals between each DSP in the RZ5D.



In RPvdsEx data is transferred across the zHop bus using paired zHop components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

The zHop bus introduces a two sample delay However, this delay is taken care of for the user in Synapse and in OpenEx (when Timing and Data Saving macros are used).

RZ5D Features

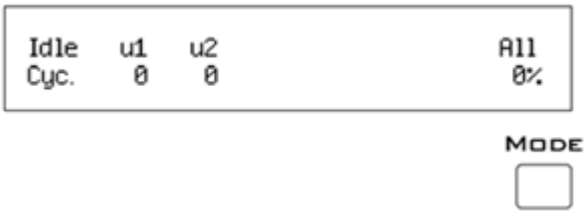
DSP Status Displays

The RZ5D include status lights and a display screen to report the status of the individual processors.

Status Lights

Two LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The corresponding LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second). For QZDSPs, the LED indicates levels for the core with the highest cycle usage.

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Reset).

Note: When burning new microcode or if the firmware on the RZ5D is blank, the display screen will report a cycle usage of 99% and the processor status lights will flash red.

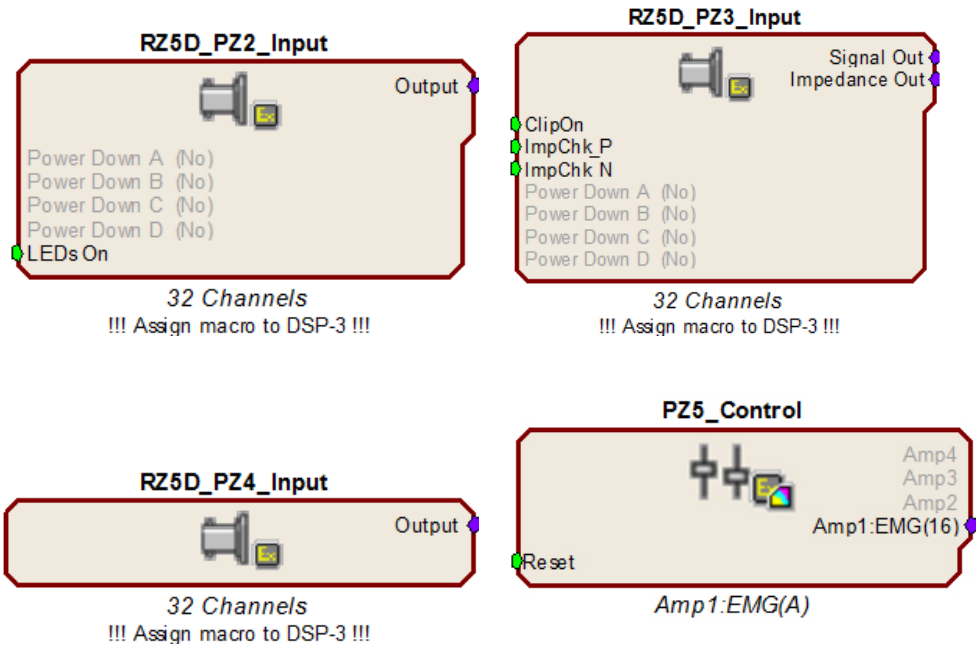
Status Indicators	Description
Cyc:	cycle usage (note: limited to 2 digits; ex: 110 displayed as 10) for QZDSPs, the highest core cycle usage is shown
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
Opt:	connection (sync) status of amplifiers A and B

Important! The status lights flash when a DSP goes over the cycle usage limit, even if only for a particular cycle. This helps identify periodic overages caused by components in time slices.

PZ Preamplifier Port

The RZ5D acquires digitized signals from a PZ preamplifier or digital headstage manifold over a fiber optic cable through the port labeled 'PZ' on the front panel. This port can input up to 32 channels at a maximum sampling rate of ~50 kHz. The PZ port can be used with any of the PZ preamplifiers including the PZ2, PZ3, and PZ5 or the PZ4 digital headstage manifold. The PZ5_Control and RZ5D_PZn_Input macros are used to access neurophysiological data in the processing chain.

Important! The macro must be placed on DSP-3 in the RPvdsEx circuit. Further, when using the RZ5D, set the *Use Direct Input* option on the PZ5_Control Setup tab to *Yes*. See the internal macro help for more details.



IZ Stimulator Port

The output port labeled IZ can be used to transfer microstimulation waveforms to the IZ2 Stimulator and/or to control an attached SH16-Z switching headstage. This port can output up to 128 channels of stimulation at a maximum sampling rate of ~50 kHz.

The IZ2_Control macro is used to send stimulation waveforms, control an optional SH16-Z, and receive monitor information from the IZ2.

Important! The IZ2_Control macro must be placed on DSP-2 in the RPvdsEx circuit. See the internal macro help for more details.

Voltage Stim Mode (32 ch)

Onboard Analog I/O

The RZ5D is equipped with four channels of 16-bit PCM D/A and four channels of 16-bit PCM A/D. All 8 channels can be accessed via front panel BNCs marked ADC and DAC or via a 25-pin analog I/O connector. See "RZ5D Technical Specifications" on page 1-24 for the DB25 pinout.

The following table provides a quick overview of the analog I/O features and how they must be accessed during circuit design. See the *RPvdsEx Manual* for more information on circuit design.

Analog I/O	Description	Components	Chan.	Notes
ADC Inputs	Analog Input	ADCIn	1 - 4	Accessed through ADC Input BNCs or Analog I/O labeled DB25
DAC Outputs	Analog Output	DacOut	9 - 12	Accessed through DAC Output BNCs or Analog I/O labeled DB25

Monitor Speaker

The RZ5 is equipped with an onboard speaker. To use the speaker, feed the desired signal to output channel 9 using a DacOut component. The speaker is provided primarily for audio monitoring of a single channel of electrophysiological potentials during recording.

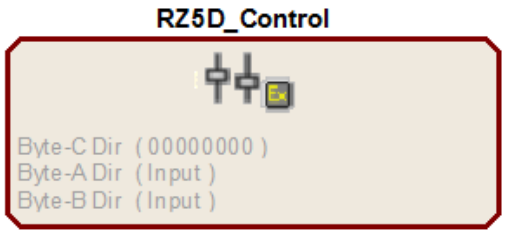
Digital I/O

24 bits of programmable digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ5D and bits 0 - 3 of byte C are available through BNC connectors on the front panel labeled Digital. See "RZ5D Technical Specifications" on page 1-24, for the DB25 pinout and BNC channel mapping.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable
*Note: Byte C Bits 0 - 3 are available via front panel BNCs				

By default, all digital I/O are configured as inputs. The data direction for the Digital I/O is configured using the RZ5D_Control macro in RPvdsEx. Double-click the macro to access the settings on the Digital I/O tab. The RZ5_Control macro also offers a Direction Control Mode parameter that enables the macro inputs and allows the user to control data direction dynamically. For more information on using the RZ5D_Control macro see the help provided in the macro's properties dialog box. For more information on addressing and Digital I/O see the *RPvdsEx Manual*.



The RZ digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table listing the different voltage outputs and thresholds for both types.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

LED Indicators

The RZ5D contains 16 LED indicators for the analog and digital I/O. These indicators are located directly below the display screen and DSP status LEDs. They display information relative to the various analog and digital I/O. The following tables list the possible display options and their associated descriptions.

Digital I/O

These LEDs indicate the state of the 8 bit-addressable I/O of byte C.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog I/O

These LEDs indicate the state of the four ADC and four DAC channels.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than +/-100 mV
Dim Green	Analog I/O channel signal voltage is less than +/-5 V
Solid Green	Analog I/O channel signal voltage is between +/-5 V to +/-9 V
Solid Red	Analog I/O channel clip warning (voltage greater than +/-9 V)

UDP Ethernet Interface (Optional)

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP Communications Interface" on page 1-51, for more information.

RZ5D Technical Specifications

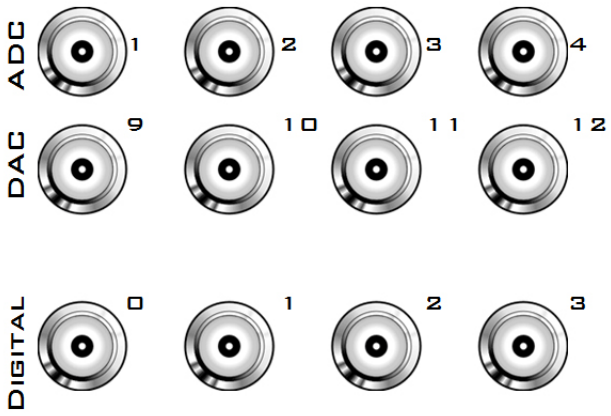
Note: Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

DSP	Three or four standard DSPs and/or quad-core (QZDSP) DSP: 400 MHz DSPs, 2.4 GFLOPS peak per DSP QZDSP: four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per QZDSP core
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)

Output Impedance	10 Ohms
A/D	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Ports	
Stimulator (IZ2)	One output for IZ2, up to 128 channels
Preamplifier (PZ)	One input for PZ5, PZ2, PZ3 or PZ4
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes (16 bits): 5.0 V, 35 mA max load

BNC Channel Mapping

Please note channel numbering begins at the top left block of BNCs for both analog and digital I/O and is printed on the face of the device to minimize miswiring.



Maps to:

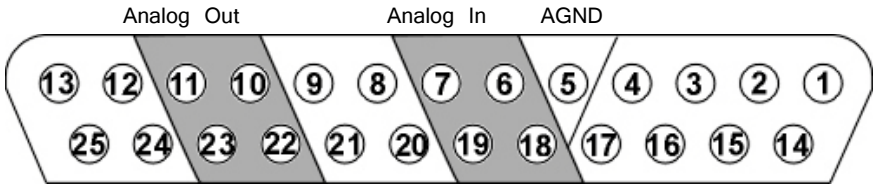
Ch 1-4 Analog In

Ch 9-12 Analog Out

Port C

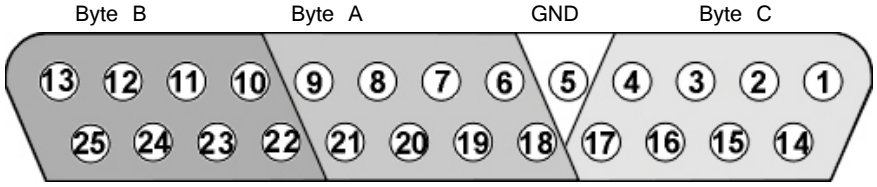
Bits 0-3 Digital I/O

DB25 Analog I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	AGND	Analog Ground		18	A1	ADC Analog Input Channels
6	A2	ADC Analog Input Channels		19	A3	
7	A4			20	NA	Not Used
8	NA	Not Used		21	NA	
9	NA			22	A9	DAC Analog Output Channels
10	A10	DAC Analog Output Channels		23	A11	
11	A12			24	NA	Not Used
12	NA	Not Used		25	NA	
13	NA					

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable Digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Byte A Word Addressable Digital I/O Bits 1, 3, 5 and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Byte B Word Addressable Digital I/O Bits 1, 3, 5 and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

RZ10 Lux Integrated Processor

RZ10 Overview

The RZ10 platform includes light driving/sensing capabilities for lock-in amplification fiber photometry setups. The RZ10x model has twice as many light driving/sensing ports for running multiple subjects or to add optogenetic stimulation, and includes fiber optic connections for integrated multi-channel neurophysiology.

The RZ10 Lux Integrated Processor has a single 400 MHz Sharc digital signal processor (DSP). It includes one bank of integrated Lux light drivers and photosensors. The RZ10x model (shown above) has three DSPs and two Lux banks standard. Both models are expandable to up to four DSPs.

Each Lux bank has 3 output drivers and 2 inputs. Each output port can have either a Lux LED, an M8 connector to drive an external LED, or a BNC connector to control a voltage signal. Each input port can have either a Lux PS1 photosensor, Lux PM1 power meter, or BNC connector to measure a voltage input. The components are interchangeable by the user.

The RZ10 includes one additional analog input channel. The RZ10x includes two additional analog input channels. The RZ10x fiber optic input port can acquire up to 32 channels of neurophysiological signals from a PZ amplifier at up to ~50kHz for real-time processing synchronized to your fiber photometry data and/or optogenetic stimulation.

The RZ10 and RZ10x both feature 24-bits of digital I/O (four bits are accessible on the front panel BNC connectors) and a legacy fiber optic port to acquire neurophysiological signals from a Medusa4Z, RA8GA, or RA16PA preamplifier.

This manual provides hardware information for the RZ10. For a full application guide specific to fiber photometry using the RZ10, see the Fiber Photometry User Guide.

Power and Communication

The RZ10's integrated Optibit optical interface connects to a PO5e card in the host PC. The connectors on the back panel are color coded for correct wiring. The RZ10's integrated power supply is shipped from the factory configured for the desired voltage setting (110 V or 220V). If you need to change the voltage setting, please contact TDT support at +1.386.462.9622 or email support@tdt.com.

Software Control

The RZ10/RZ10x is intended for use with TDT's Synapse software only.

RZ10 Features

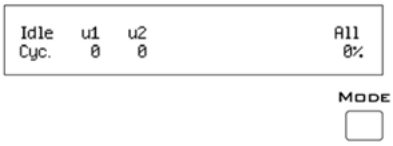
DSP Status Displays

The RZ10 include status lights and a display screen to report the status of the individual processors.

Status Lights

Four LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. If the cycle usage on a DSP exceed 99% of its capacity, the corresponding LED will flash red (~1 Hz).

Front Panel Display Screen



The front panel display screen shows two lines of information about the system status. The top line reports the system mode, Run!, Idle, or Reset. Run! means a circuit is loaded and running. Reset means the system is booting up. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value, selected with the Mode pushbutton. Press and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options.

Note: When burning new microcode after a TDT driver update, or if the firmware on the RZ10 is blank, the display screen will report a cycle usage of 99% and the processor status lights will flash red.

Status Indicators	Description
Cyc:	processing cycle usage
Bus%:	percentage of internal device's data bus capacity used
I/O%:	percentage of data transfer capacity used

PZ Preamplifier Port

The RZ10x acquires digitized signals from any PZ preamplifier (PZ2-PZ5) over a fiber optic cable through the port labeled 'PZ Amp' on the front panel. This port can input up to 32 channels at a maximum sampling rate of ~50 kHz.

Onboard Analog Inputs

The RZ10 has an extra channel of 16-bit PCM A/D input, accessible through the BNC marked 'ADC4'. The RZ10x has an additional channel marked 'ADC8'. See the *Synapse Manual* for information on enabling analog inputs.

Fiber Optic Preamplifier Port

The RZ10 acquires digitized neurophysiological signals from a Medusa preamplifier over a fiber optic cable. It samples up to 16 channels at a maximum sampling rate of ~25 kHz.

The fiber optic ports can be used with any of the Medusa preamplifiers including the Medusa4Z, RA16PA, RA4PA, or RA8GA. The port is limited to ~25 kHz, however if the processor is running ~50 kHz sampling rate the Medusa data is oversampled to 2x or ~50 kHz.

Digital I/O

24 bits of programmable digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ10 and bits 0 - 3 of byte C are available through BNC connectors on the front panel labeled C0-C3. See "RZ10 Technical Specifications" on page 1-33, for the DB25 pinout and BNC channel mapping.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable
*Note: Byte C Bits 0 - 3 are available via front panel BNCs				

See the *Synapse Manual* for information on enabling digital I/O and configuring data direction.

The RZ10 digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table depicting the different voltage outputs and thresholds for both type.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

LED Indicators

The RZ10 has 16 LED indicators for the analog and digital I/O. These indicators are located directly below the display screen and DSP status LEDs. The following tables describe the meaning of the status LEDs.

Digital I/O

These LEDs indicate the state of the 8 bit-addressable I/O of byte C.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1) default

Analog I/O

These LEDs indicate state of the first bank of Lux I/O only.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than +/- 100 mV
Dim Green	Analog I/O channel signal voltage is less than +/- 5 V
Solid Green	Analog I/O channel signal voltage is between +/- 5 V to +/- 9 V
Solid Red	Analog I/O channel clip warning (voltage greater than +/- 9 V)

Note: ADC channel 3 and DAC channel 4 are used internally while the RZ10 is actively running, so the ADC3 and DAC4 LEDs will flash ~1Hz during normal operation.

UDP Ethernet Interface (Optional)

The RZ UDP Ethernet interface can transfer data to or from a networked computer for fast integration with external software. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP Communications Interface" on page 1-51, for more information.

Onboard Lux I/O

The RZ10 has one bank of integrated Lux components. Each Lux bank has three built-in current driver outputs for driving integrated LEDs directly, or external LEDs connected to an M8 cable. Each Lux bank also has two input slots for photosensors and/or power meters.

The RZ10x includes a second full bank for Lux components.

The Lux components are held in place with two nylon screws. They are interchangeable, so you can swap LED colors at any time, upgrade from an external photosensor to a PS1 integrated sensor, or interface with an external device with a BNC connector. In the case of lost Lux screws, do not replace them with metal screws. Please contact TDT support for replacement screw options.

Important!: Make sure the RZ10 is powered off before changing the Lux components.

Each Lux LED pod is colored with the closest visible color to the wavelength of light it emits. The Lux LEDs can occupy the left three slots of each Lux bank. The 465nm Lux LED is shown at left.

The PS1 photosensor measures the fluorescence response from the subject. It can occupy the right two slots of each Lux bank.

The PM1 Power Meter measures the LED power received by the subject. It has built-in fluorescing material so it can also mimic a subject response for full end-to-end system testing. The PM1 can only occupy the slot on the far right of each Lux bank.

The M8 connector is the default placeholder for the left three slots if LEDs aren't installed. It is used to drive an external LED. This can be a Lux LED in an external heat sink, or a third-party LED.

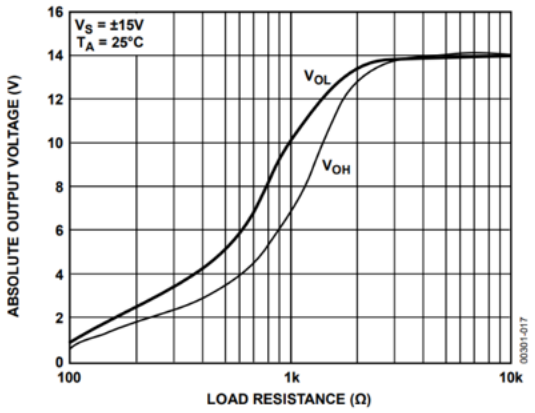
The BNC connector can be swapped into any location on the Lux bank to connect to third party devices. It is the default placeholder for the right two slots if PS1/PM1s aren't installed.

The Lux LEDs, PS1, and PM1 have an FC connector with a small key that must be aligned to the fiber optic cable. This key is in the 10 o'clock position on all TDT optical Lux components.

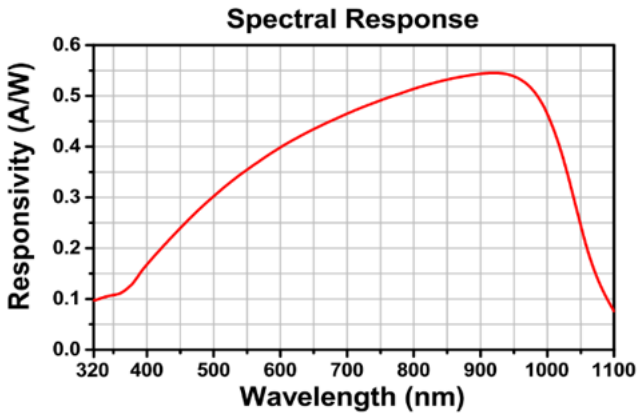
See the *Synapse Manual* for information on controlling the Lux drivers and reading the sensors.

Lux Technical Specifications

LEDs	
Available Wavelengths	385 nm, 405 nm, 415 nm, 450 nm, 465 nm, 500 nm, 530 nm, 560 nm, 590 nm, 615 nm, 635 nm, 850 nm, 940 nm, 5K
Current Range	2 mA - 1000 mA
PS1	
Bandwidth	DC - 700 Hz
Wavelength Range	320 nm - 1100 nm
Gain	10^{10}
PM1	
Bandwidth	DC - 3000 Hz
Wavelength Range	320 nm - 1100 nm
Gain	6.5×10^{4}
BNC Output Pod	RZ10: up to 3 channels, 16-bit PCM RZ10x: up to 6 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 6 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	See below
BNC Input Pod	RZ10: up to 2 channels, 16-bit PCM RZ10x: up to 4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms (impedance of input connection will appear to be ~400 Ohm higher)



Lux BNC Pod Output Impedance



PS1 and PM1 Responsivity

RZ10 Technical Specifications

Note: Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

DSP	Up to four standard DSPs and/or quad-core (QZDSP) DSP: 400 MHz DSPs, 2.4 GFLOPS peak per DSP QZDSP: four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per QZDSP core
A/D	RZ10: 1 channel, 16-bit PCM RZ10x: 2 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms

Fiber Optic Ports	
PZ Amp	RZ10x: One input for PZ5, PZ2, PZ3 or PZ4, up to 32 channels
Legacy Amp	16-channel input, up to 24414.0625 Hz
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes (16 bits): 5.0 V, 35 mA max load

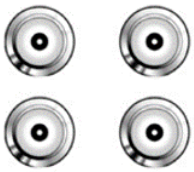
BNC Channel Mapping

Please note channel numbering is printed on the face of the device to minimize mis-wiring.

Maps To:

Ch 4 Analog In

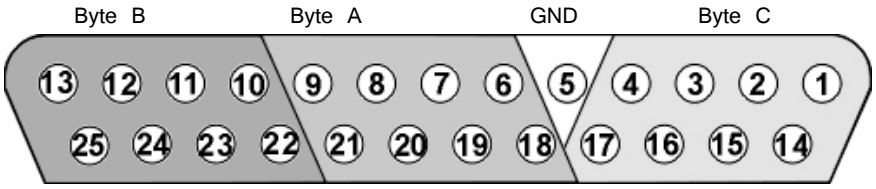
Ch 8 Analog In (RZ10x only)



Maps To:

Port C Bits 0-3 Digital I/O

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable Digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Byte A Word Addressable Digital I/O Bits 1, 3, 5 and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Byte B Word Addressable Digital I/O Bits 1, 3, 5 and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

RZ6 Multi I/O Processor

RZ6 Overview

The RZ6 Multi I/O Processor is a high sample rate processor with flexible input/output capabilities. The RZ6 features up to four digital signal processors cards; any card can be either a single standard processor card (RZDSP) or a quad-core processor card (QZDSP). Standard single processor cards use a single Sharc DSP, quad-core processor cards use four Sharc DSPs cores with the potential to more than double the power of the RZ6. All cards are networked in an optimized multiprocessor architecture that features efficient onboard communication and memory access. Two channels each of sigma-delta D/A and A/D converters provide a dynamic range of up to 115 dB and sampling rates up to ~200 kHz.

The single device form factor incorporates two channels of onboard programmable and manual attenuation and can drive headphones and standard, magnetic, or electrostatic speakers. It includes an onboard monitor speaker, two channels of amplification for analog inputs, and 24 channels of digital I/O. XLR, audio jack, and BNC connections are supported. Optionally, the RZ6 can be equipped with a fiber optic input, allowing it to support a four channel Medusa preamplifier.

The RZ6-A base version starts with a single DSP and makes an excellent all-in-one psychoacoustics system or can be added to any system to add audio stimulus generation to experiments.

The RZ6-A-P1 comes equipped with three DSPs for more processing power and includes the optional fiber optic input port, allowing it to serve as a BioAmp base station for ABR and OAE studies.

Both configurations can be upgraded with additional single or quad-core DSP cards (up to a maximum of four DSP cards) for complex filtering and high frequency applications.

Power and Communication

The RZ6's Optibit optical interface ensures fast and reliable data transfer from the RZ6 to the PC and is integrated into the device. Connectors are provided on the

back panel and are color coded for correct wiring. The RZ6's power supply is also integrated into the device and is shipped from the factory configured for the desired voltage setting (110 V or 220 V). If you need to change the voltage setting, please contact TDT support at 386.462.9622 or email support@tdt.com.

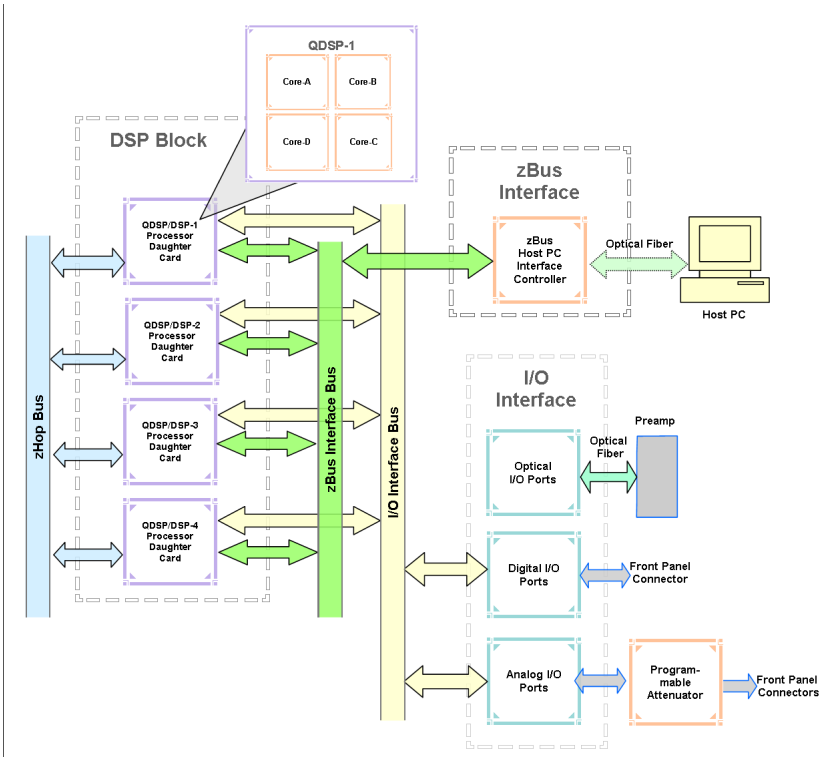
The RZ6 is UL compliant, see the *RZ5/RZ5D/RZ6 Operations Manual* for power and safety information.

Software Control

TDT Synapse or BioSigRZ software controls the RZ6 and provides users a high level interface for device configuration. Device programming is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. Several RZ6 macros are provided and are required to handle all programmable features related to the RZ6. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RZ6 Multi-Bus Architecture

The RZ6 processor utilizes a multi-bus architecture and offers four dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



RZ6 Architecture Diagram

As shown in the diagram above, the RZ6 architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP block is connected to three data buses: two buses that connect each DSP to the other functional blocks and one that handles data transfer between the DSPs (the zHop Bus). This architecture facilitates fast DSP-to-off-chip data handling.

Each standard DSP is connected to 64 MB SDRAM and each core in a QZDSP is connected to 256 MB DDR2. Large and complex circuits should be designed to balance memory needs (such as data buffers and filter coefficients) across processors.

When designing circuits also note that the maximum number of components for each RZ6 standard RZDSP is 768 and 1000 for each QZDSP.

The zBus Interface

The zBus interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus Interface Bus.

The I/O Interface

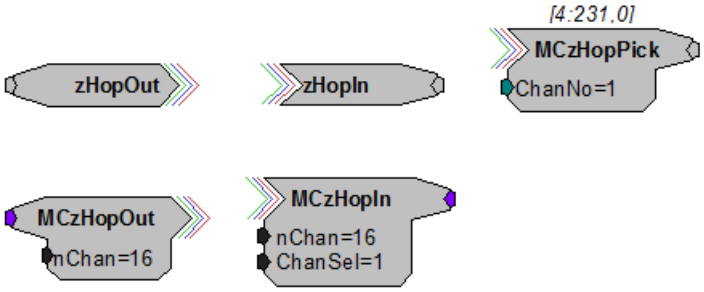
The I/O interface serves as a connection to outside signal sources or output devices. It is used to input data from the optional preamplifier input and digital and analog channels. The I/O interface bus provides a direct connection to each DSP.

Distributing Data Across DSPs

To take advantage of multi-DSP modules, processing tasks must be efficiently distributed across the available DSPs (or among cores of a quad-core DSP). The RZ6 architecture provides the zHop bus for transferring data across DSPs.

The zHop Bus

The zHop bus allows the transfer of single or multi-channel signals between each DSP in the RZ6.



In RPvdsEx, data is transferred across the zHop bus using paired zHop components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. Up to 126 pairs can be used in a single RPvdsEx circuit.

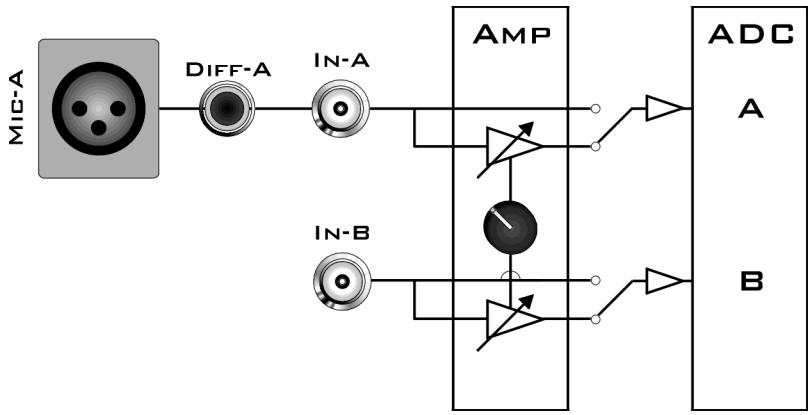
Bus Related Delays

The zHop Bus introduces a two sample delay. This delay is taken care of for the user in Synapse, BiosigRZ, and in OpenEx (when Timing and Data Saving macros are used).

Functional Signal Flow Diagrams

The following diagrams illustrate how analog signals for channels A and B flow through the RZ6 and its modules. For more information on analog input and output see "Onboard Analog I/O and Optional Amplifier Input" on page 1-41.

The diagram to the below depicts the analog input flow for the RZ6.

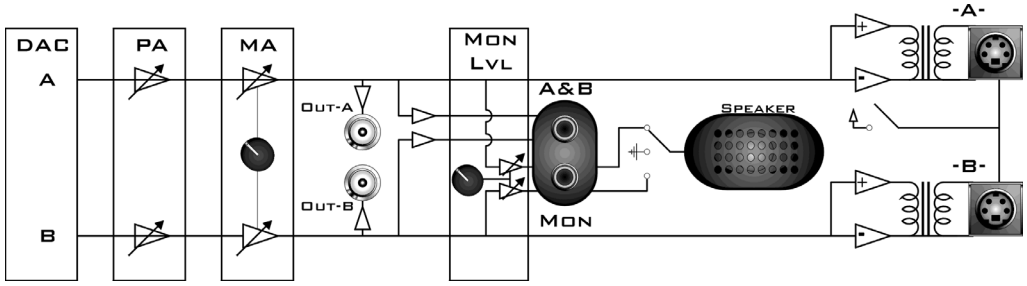


RZ6 Analog Input Flow Diagram

Input signals for channel A are input either through the XLR input (Mic-A), the audio jack input (Diff-A), or BNC (In-A). Input signals for channel B are input through the BNC (In-B).

A switch located to the left of the gain control knob allows a single gain setting for both channels to be applied or bypassed completely.

The diagram below depicts analog output flow through the RZ6.



RZ6 Analog Output Flow Diagram

Signals A and B flow out of the DAC and pass through the programmable and manual attenuation modules prior to being output on the front panel BNC connectors (Out-A and Out-B).

The signals for channels A and B are also passed to two stereo headphone output ports labeled A&B and Mon. Individual stereo power amplifiers are used for the BNC and stereo headphone outputs.

A single channel monitor speaker is connected either to signal A, signal B, or disabled based on the monitor control switch setting. The monitor level knob controls the sound level of both the stereo headphone jack labeled Mon and the monitor speaker.

Finally, if the electrostatic speaker driver is enabled via its switch, located on the front panel, signals A and B are output from the mini-DIN ports located on the RZ6 front panel.

RZ6 Features

Onboard Analog I/O and Optional Amplifier Input

The RZ6 is equipped with onboard analog I/O and may also include a fiber optic port for Medusa preamplifier input.

The following table provides a quick overview of the analog I/O and amplifier input features and how they must be accessed during circuit design. The RZ6 relies exclusively on macros for configuring analog and digital I/O and its fiber optic input port. See the *RPvdsEx Manual* for more information on circuit design.

Analog I/O	Description	Channels	Required Macro
ADC Inputs	Analog Input	A and B	RZ6_AudioIn
DAC Outputs	Analog Output	A and B	RZ6_AudioOut
Optical Amp	Medusa PreAmp Input	1-4	RZ6_AmpIn

Onboard Analog Inputs

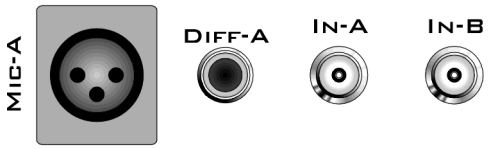
The RZ6 is equipped with two channels of 24-bit sigma-delta A/D converters. See "RZ6 Multi I/O Technical Specifications" on page 1-47, for more information.

Analog signals can be input through several connectors on the RZ6 front panel.

Channel A has three possible sources:

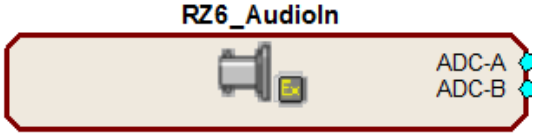
- MIC-A (XLR microphone input)
- DIFF-A (1/4" TRS microphone input)
- BNC labeled In-A

Channel B uses only the BNC labeled In-B:



Important! Use only one input for channel A at a time. Attempting to input signals from multiple sources will produce an erroneous signal.

Analog input is accessed in RPvdsEx through the RZ6_AudioIn macro.



A and B Microphone Amplifier

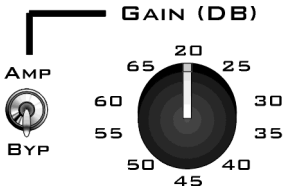
An onboard two channel amplifier provides gain for the onboard analog input signals (MIC-A, DIFF-A, In-A, and In-B). The switch located to the left of the gain control knob allows the current gain setting to be applied (if set to Amp) or bypassed completely (if set to Byp).

Important! When the gain is enabled, analog input signals MIC-A and DIFF-A are differential. Since the differential signals are summed a signal gain of 6 dB will be inherently applied. If the amplifier is bypassed, common mode rejection is disabled.

Note: To prevent clipping caused by a DC offset, the amplifier is AC coupled when the gain amplification is in use.

Gain

The front panel gain control knob can be used to the control overall signal level of both channels from 20 to 65 dB in 5 dB steps.



Fiber Optic Port - Optional

The RZ6-A-P1 acquires digitized signals from a Medusa preamplifier over a fiber optic cable. The port can be used with the RA4PA to input up to 4 channels.

Input from the preamplifier fiber optic port is accessed using the RZ6_AmpIn macro.

The fiber optic port (devices with serial number 1007 and greater) can also support the HTI3 Head Tracker Interface.

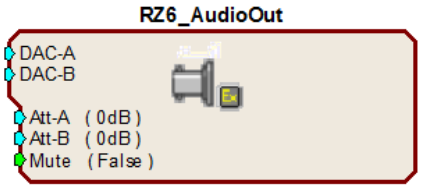
Fiber Oversampling (acquisition only)

Signals are digitized on the Medusa preamplifier at a maximum sampling rate of ~25 kHz, however, the fiber optic port on the RZ6 can oversample the digitized signals up to 8X or ~200 kHz. This will allow the RZ6 to run a DSP chain at ~200 kHz and still sample data acquired through an optically connected preamplifier.

Oversampling is performed on the RZ6. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

Onboard Analog Outputs

The RZ6 is equipped with two channels of 24-bit sigma-delta D/A converters (see "RZ6 Multi I/O Technical Specifications" on page 47). Analog signals are output through a variety of connectors on the RZ6 front panel. Analog output is configured in RPvdsEx through the RZ6_AudioOut macro.



Programmable Attenuation

The RZ6_AudioOut macro provides access to two channels of programmable attenuation for precision control of analog output signal levels over a wide dynamic range.

Programmable attenuation in the RZ6 is achieved using both analog and digital attenuation methods. The device supports analog attenuation values of 0, 20, 40, and 60 dB. Attenuation values which lie in-between or exceed 60 dB are handled using digital attenuation.

For example, if you set an attenuation value of 66 dB in the RZ6_AudioOut macro, the analog attenuator will be set to 60 dB and the remaining 6 dB of attenuation will be applied by scaling the digital signal through RPvdsEx.

Note: For the best results, you should utilize the maximum D/A voltage range and use the RZ6_AudioOut macro to configure the desired attenuation setting for channels A and B.

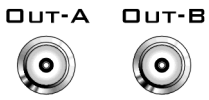
Manual Attenuator

The RZ6 includes another level of analog attenuation that can be controlled manually via the attenuator control knob from 0 to 27 dB in increments of 3 dB.

Manual attenuation is applied to both channels before the signals are output on any of the front panel connectors and is therefore applied in addition to any programmable attenuation set in RPvdsEx through the RZ6_AudioOut macro.

Analog Output via BNCs

DAC channels A and B are output to BNCs labeled Out-A and Out-B after attenuation has been applied. These outputs use a stereo power amplifier to drive TDT's MF1 multi-function speakers.



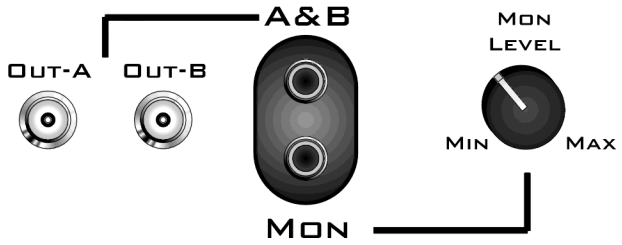
Note: A single signal generated or input from any of the RZ6 analog inputs can be ganged to reduce the spectral variation in power of the transducer across all frequencies. To do this, configure your signal to output from both DAC channels as shown in the following diagram.

Ganged Output Connection Diagram

Configure your RPvdsEx circuit to output the same signal to DAC channels A and B then connect the transducer as shown in the diagram above.

Stereo Headphone Output

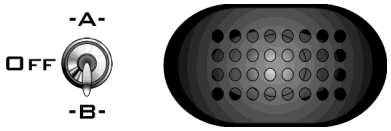
DAC channels A and B are also available as a stereo headphone output through two 1/8" audio jack connector ports (channel A is the left stereo output and channel B is the right stereo output). The port labeled A&B (top) provides a stereo headphone output suitable for experimental paradigms while the port labeled Mon (bottom) can be controlled by the Mon Level knob located directly to the right, making it more suitable for monitoring the experiment.



Audio Outputs

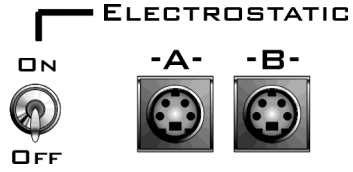
Note: All outputs use stereo power amplifiers

Monitor Speaker



The RZ6 is equipped with an onboard monitor speaker, provided for audio monitoring of a single channel. A switch located directly to the left of the monitor speaker is used to select between DAC channels A and B or to disable the monitor speaker. The monitor speaker output level is controlled by the Mon Level knob located directly to the right of the monitor stereo output.

Electrostatic Speaker Output



An onboard two channel broadband electrostatic speaker driver is provided, allowing direct connection of TDT's ES series electrostatic speakers. The driver produces flat frequency responses reaching far into the ultrasonic range, can drive two ES series speakers, and is powered using the onboard power supply. A switch located directly to the left of the two 4-pin, mini-DIN connectors is used to enable or disable output of DAC channels A and B.

Note: The electrostatic speaker driver is designed to work exclusively with TDT's electrostatic series speakers. Do NOT attempt to use any other speaker.

Important! If the electrostatic speaker driver is not being used, make sure that the ON/OFF switch is in the OFF position to reduce noise on the RZ6.

Digital I/O

Current RZ6 models are equipped with 24 bits of programmable digital I/O divided into three bytes (A, B, and C) as described in the chart below. Earlier versions

(serial number < 2000) were limited to 8 bits. By default, all lines are configured as inputs.

Data direction is configured using the RZ6_Control macro in RPvdsEx and may be controlled dynamically through the macro input port. For more information on using the RZ6_Control macro see the help provided in the macro's properties dialog box.

Digital I/O	Description	Notes
Byte A	bits 0 - 7	byte addressable
Byte B	bits 0 - 7	byte addressable
Byte C	bits 0 – 7	bit addressable

The Digital I/O connector can be found on the front of the RZ6. See "RZ6 Multi I/O Technical Specifications" on page 1-47, for pinout.

Voltage outputs and logic thresholds vary by type as shown in the table below.

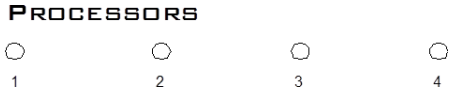
Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

See "Working with BitIn - BitOut" in the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming and addressing Byte C of the digital I/O. See "Working with WordIn -WordOut" in the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming and addressing Bytes A and B of the digital I/O.

DSP Status Displays

The RZ6 includes status lights and a screen to report the status of the individual processors.

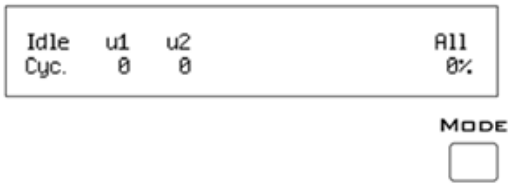
Status Lights



LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second). For QZDSPs, the LED represents the highest core cycle usage.

Important! The status lights flash when a DSP goes over the cycle usage limit, even if only for a cycle. This helps identify periodic overages caused by components in time slices.

Front Panel Screen



The front panel screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The screen may also report system status such as booting status (Reset).

Note: When burning new microcode or if the firmware on the RZ6 is blank, the screen will report a cycle usage of 99% and the processor status lights flashes red.

Status Indicators

Cyc:	cycle usage; for QZDSPs, the highest core cycle usage is shown **Note:** limited to 2 digits; ex: 110 displayed as 10.
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
DAC:	Displays the current analog attenuator setting. Also displays bars according to the RMS level of DAC A and B using a logarithmic scale. **Note:** Eight solid bars denote that the signal on DAC A or B is clipping.
ADC:	Displays bars according to the RMS Level on ADC A and B using a logarithmic scale. **Note:** Eight solid bars denote that the signal on ADC A or B is clipping.

Analog Input – ADC LED Indicators

The ADC LED indicators are labeled and located at the top right of the RZ6 front panel. The LEDs indicate the level of the signals on ADC channels A and B. This provides a useful indicator for adjusting the gain and to detect and prevent clipping. The following table describes the LED indicators' operation.

Light Pattern	LEDs Lit	Description
	4	Input is ≤ -6 dB down from max input voltage
	3	Input is between -6 dB and -12 dB down from max input voltage
	2	Input is between -12 dB and -25 dB down from max input voltage
	1	Input is between -25 dB and -50 dB down from max input voltage

Digital I/O LED Indicators

The digital I/O LED indicators are located directly below the screen and DSP status LEDs and display information relative to the digital I/O contained on the RZ6. There are 8 LEDs one for each bit addressable digital I/O channel (Byte C). Each LED may display one of four states. The following table illustrates the possible display options and their associated descriptions.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog Input - Fiber Optic Port LED Indicator

A single green LED indicator is provided for the fiber optic input port on the RZ6-A-P1. When lit the LED signifies a Medusa preamplifier is correctly synced with the RZ6.

RZ6 Multi I/O Technical Specifications

Note: The RZ6 can be equipped with a fiber optic input port and used with a four channel Medusa preamplifier. See the preamplifier's technical specifications for A/D converters.

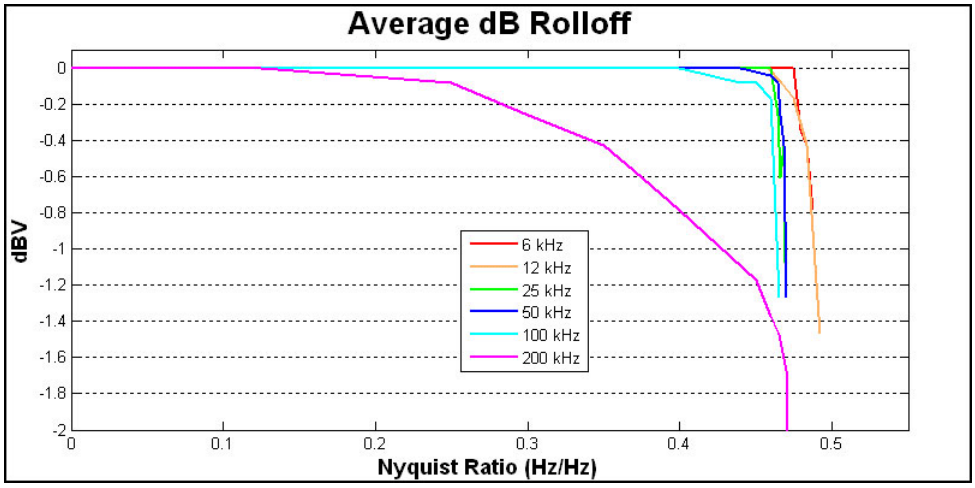
DSP	Up to four standard DSPs and/or quad-core (QZDSP) DSP: 400 MHz DSPs, 2.4 GFLOPS peak per DSP QZDSP: four 400 MHz DSPs, 2.4 GFLOPS per core
Memory	64 MB SDRAM per standard DSP 256 MB DDR2 RAM per QZDSP core
D/A	2 channels, 24-bit sigma-delta
Sample Rate	Up to 195312.50 Hz
Frequency Response	DC - 0.44*Fs (Fs=sample rate)

Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	115 dB (20 Hz - 80 kHz at 5 Vrms)
THD (typical)	-90 dB (1 kHz output at 5 Vrms)
Sample Delay	31 (Serial numbers > 2000) 47 (Serial numbers < 2000)
A/D	2 channels, 24-bit sigma-delta
Sample Rate	Up to 195312.50 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage In	+/- 10.0 Volts
S/N (typical)	115 dB (20 Hz - 80 kHz at 5 Vrms)
THD (typical)	-90 dB (1 kHz output at 5 Vrms)
Sample Delay	66 samples
Fiber Optic Ports	**Optional Input Available on RZ6-A-P1 only** Supports 4-channel Medusa preamplifier or HTI3 Head Tracker Interface (serial number 1007 and greater)
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes (16 bits): 5.0 V, 35 mA max load
A and B Microphone Amplifier	Single setting for both channels (AC coupled when enabled)
High Pass Corner Frequency	3.6 Hz (Active only if the Amplifier is enabled)
Gain Settings	20 to 65 dB
Gain Step Size	5 dB
Programmable Attenuation	2 channels
Switching Time	1 sample
Settling Time	3 µsec
Transient Voltage	~370 mV
Hardware Attenuation Settings	0, 20, 40, 60 dB
Manual Attenuation	Single setting for both channels
Attenuation Settings	0 to 27 dB
Attenuation Step Size	3 dB
Amplification	2 channels
Spectral Variation	< 0.1 dB from 50 Hz to 200 kHz

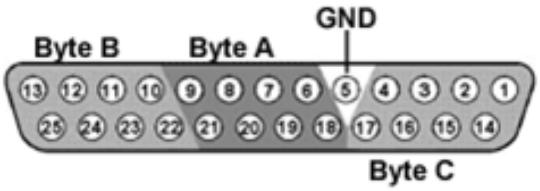
Signal Noise	115 dB (20 Hz to 80 kHz)
THD	< 0.02% at 1 Watt from 50 Hz to 100 kHz
Noise Floor	20 µV rms
Input Impedance	10 kOhm
Output Impedance	1 Ohm
Power Output	0.75 W/channel into 5.5 ohms
Headphone Output	2 channels
Output Impedance	1 Ohm
Power Output	0.75 W/channel into 5.5 ohms
Electrostatic Speaker Output	2 channels Note: For further information on speaker specifications, "EC1 Technical Specifications" on page 17-12.

D/A dB Rolloff Diagram

This graph shows the dB rolloff for the RZ6 with varying sampling frequencies for the D/A. The sample delay remains constant for varying frequencies.

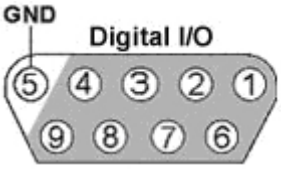


DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word addressable digital I/O Bits 0, 2, 4, and 6
6	A1	Byte A Word addressable digital I/O Bits 1, 3, 5, and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word addressable digital I/O Bits 0, 2, 4, and 6
10	B1	Byte B Word addressable digital I/O Bits 1, 3, 5, and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

Digital I/O – DB9 Connector Pinout



Note: Serial numbers < 2000 only.

Pins	Name	Description		Pin	Name	Description
1	D0	Digital I/O 0, 2, 4, 6		5	GND	Ground
2	D2			6	D1	Digital I/O bits 1, 2, 3, 5, 7
3	D4			7	D3	
4	D6			8	D5	
5	GND	Ground		9	D7	

RZ-UDP Communications Interface

RZ2 Processor Back side with RZ-UDP Installed

RZ-UDP Overview

The RZ Communications Interface (RZ-UDP-20) is an optional interface for RZ processor devices that includes a UDP Ethernet connection and a serial port connection.

The serial port can support baud rates up to 115200. The port is a standard 9-pin RS232 connection located on the back of the RZ. The RS232 port can be directly connected to any device that communicates via serial port, such as head trackers, eye trackers, or a PC. Note: If installed in an RZ with 4 optical DSP cards, the serial port is not available.

The UDP interface is designed to transfer up to 200 data values at low rates to or from a PC. The PC may be directly connected through a dedicated Ethernet card located elsewhere on the user's network, or even in a remote location connected via the Internet. The RZ UDP interface is located on the back panel of the RZ processor and accepts a standard Ethernet cable.

Like all network devices the RZ UDP interface utilizes several network parameters such as a unique network address, appropriate network mask, and optionally a gateway (if operating across networks). The RZ UDP Ethernet interface supports the DHCP (Dynamic Host Configuration) protocol for automatic configuration of these network parameters, but these parameters may also be set manually, as described in "Network Settings" on page 1-60 The type and structure of data for the serial port must be manually configured through the same network interface.

Note: The RZ-UDP-20 is an updated version of the RZ-UDP-10 which had only an Ethernet interface. Configuration of the Ethernet interface is the same for both versions.

RZ-UDP Basics

Installation

Synapse has built-in objects for the Processing Tree to send and receive data from the UDP interface. These must be added to your Hardware Rig in Synapse and then simply connect the desired signal stream to the UDP object. See the Synapse manual for more information.

The TDT drivers installation provides the UDP test application here:

C:\TDT\RPvdsEx\Examples\RZ UDP\

For RPvdsEx circuit design, two macros designed for the UDP Ethernet interface and two macros for the serial interface are installed here:

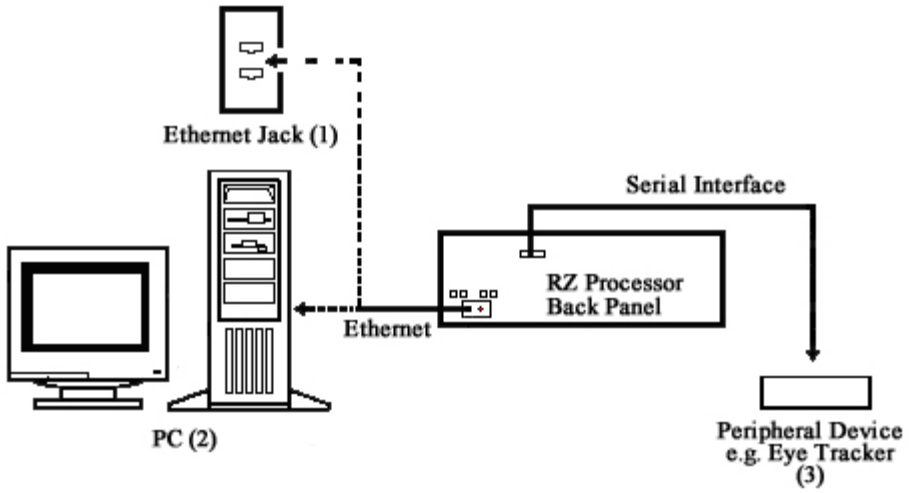
C:\TDT\RPvdsEx\Macros\Device\UDP Ethernet\

Hardware Requirements

Basic requirements include an Ethernet cable and an RZ processor equipped with the UDP interface. A PC equipped with an Ethernet port or an Ethernet jack connected to a local area network is required to send or receive data from an RZ processor. Optionally, a 9-pin RS232 cable is required to connect the serial port to an external device or a PC.

Setting-Up Your Hardware

To setup the UDP Ethernet interface, connect your Ethernet cable directly to a PC Ethernet port or standard Ethernet wall jack. For more information on setting up or configuring the RZ processor see the System 3 Installation Guide.



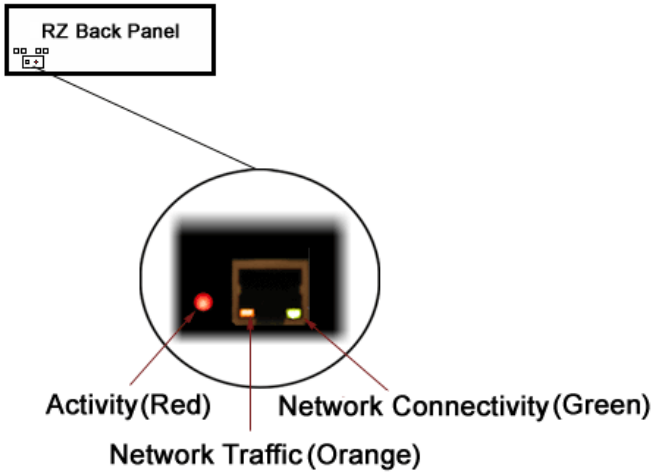
The diagram above illustrates the possible connections from the RZ processor to an active network (1) or PC (2), and an optional serial connection to a peripheral device (3).

Note: If you are only using the serial interface, you will still need a UDP Ethernet connection to configure the serial interface through the web interface. See "Configuring the UDP through the Web Interface" on page 1-58, for more

information.

Status LEDs

The UDP Ethernet interface provides several status indicators which are located on the back of the RZ processor. These status indicators are used to denote a proper connection to a network, activity or network traffic, or UDP activity such as sending or receiving packets.



The following table lists the possible status indicators for the UDP Ethernet interface.

Status	LED Color		
	Green	Orange	Red
Off	No network connectivity	No network traffic detected	Remote address set, no activity
Blinking slowly (once / sec)		Light network traffic is present	Power connected, waiting for remote address to be set
Blinking rapidly or solid glow (several times / sec)	Link connected	Heavy network traffic present	Packet activity present (send or receive)

Network Structure

In order to understand how the UDP interface works, a basic understanding of Internet Protocol (IP) networking is required. As mentioned above, all network devices require a unique network address, appropriate network mask, and if communicating between networks, a gateway. Data in IP networks is organized into discrete packets for transmission or reception. For our purposes, the packet size is equivalent to the number of channels being transmitted or received.

Network Address

All network devices utilize a network address commonly referred to as the "IP address". The IP address is a unique address given to any networked device and consists of four hexadecimal values that are used to locate a device from within a network. Multiple devices that are located within a common network use similar IP addresses.

For example:

Several office computers are connected to a network within an office.

IP address Computer 1:192.86.100.10

IP address Computer 2:192.86.100.11

IP address Computer 14:192.86.100.23

As shown above, IP addresses share a common prefix when located on a common network.

Subnet Mask

Just as the IP address is important for each device contained within a network, the subnet mask is used to classify the size of the network as well as determine the broadcasting address for a device. When an IP address is given to a device, the inverse of the subnet mask is ORed to the IP address to obtain the broadcast address.

For example:

To obtain the broadcast for an IP address with a subnet mask of 255.255.255.0 the IP address and inverse of the subnet mask value are ORed.

IP Address:

192.86.100.10 = 1100 0000 | 0101 0110 | 0110 0100 | 0000 1010

Subnet Mask^{-1}:

0.0.0.255 = 0000 0000 | 0000 0000 | 0000 0000 | 1111 1111

Broadcast:

192.86.100.255 = 1100 0000 | 0101 0110 | 0110 0100 | 1111 1111

Several types of network protocols and services use broadcasts in different ways. Dynamic Host Configuration Protocol (DHCP), for instance, requires that broadcasts be used to dynamically assign a unique IP address to computers on a network.

Types of Networks

Several different classifications of networks exist and are organized by the number of possible network addresses (IP addresses) available. The previous example used a Class C network subnet mask.

The following table illustrates the bit ranges and classifications of common networks.

Class	Start	End	Default Subnet Mask
Class A	0.0.0.0	127.255.255.255	255.0.0.0
Class B	128.0.0.0	191.255.255.255	255.255.0.0

Class	Start	End	Default Subnet Mask
Class C	192.0.0.0	223.255.255.255	255.255.255.0

Class A defined networks contain a broad range of possible values since the subnet mask allows for 24 bits or 16,777,214 addresses per network. A Class C network contains 8 bits of IP addresses per network and so, allows up to 256 possibilities.

Gateway

Along with an IP address and subnet mask, networks may optionally use a gateway which is required to send or receive data from outside the network. You can think of a gateway as a node that serves as an access point to another network.

MAC Address

A device's MAC address or "Media Access Control" address is a unique number that acts like a name for a particular network adapter. On a shared medium such as Ethernet, this address is generally assigned to the hardware when it is constructed, but may be manually modified in the UDP Interface.

For example:

The network cards in two different computers will have different MAC addresses, as would an Ethernet adapter and a wireless adapter in the same computer.

The DHCP Protocol

DHCP or "Dynamic Host Configuration Protocol" is a protocol used by networked devices (clients) to obtain various parameters necessary for the clients to operate in an Internet Protocol (IP) network. By using this protocol, system administration workload greatly decreases, and devices can be added to the network with minimal or no manual configuration.

DHCP automates the assignment of IP addresses, subnet masks, default gateway, and other IP parameters. Three modes for allocating IP addresses exist: dynamic, reserved, and manual. The UDP interface relies primarily on dynamic mode for its IP configuration.

Dynamic

In dynamic mode a client is provided with a temporary IP address for a given length of time. This length of time is dependent on the server configuration and may range from a long time (months) to several hours.

The current IP address can be renewed at any time by the DHCP client. This renewal is used by properly functioning clients to maintain the same IP address throughout their connection to a network.

Reserved

In reserved mode, the IP address is permanently assigned to a client via DHCP server-side reservations. Please check the documentation for your DHCP server for more information.

Manual

In manual mode the IP address is selected by the client (manually by the user or any other means) and the DHCP protocol messages are used to inform the server that the address has been allocated.

The UDP Protocol

UDP or "User Datagram Protocol" is a core protocol of the Internet Protocol suite or more commonly known as the TCP/IP protocol suite. UDP allows programs and networked computers to send datagrams or data organized in a specific structure (commonly referred to as a packet).

Note: The UDP protocol is considered "connectionless" since devices send data to a defined IP address and are not actively connected to the destination device or PC. As such, the UDP Ethernet interface will send or receive data from the last IP address it is configured to communicate with.

When information from a data protocol (UDP or TCP) is sent, the information may get lost or delayed along the way. UDP protocol allows time critical data to be transmitted with very low latency since UDP protocol does not implement data tracking. Conversely, when TCP detects that information has been lost or received out of order, it resends the suspect information. This is insufficient for time dependent data found in most neuroscience applications.

Note: The UDP protocol does not account for data received out of order.

Process Layers

The UDP Ethernet interface operates on a structure of layers. These layers interact with each other as segments to produce the end result; to send data from one source and receive it intact on another source. Five layers of this structure are shown below.

Layer - Name	Entity or Protocol	Segment Task
1 – Physical	UDP Ethernet Interface	Encodes the data into packets.
2 – Data Link	Ethernet	Provides a means to move data packets.
3 – Network	IP	Provides a link between one or more data sources.
4 – Transmission	UDP	Manages the transfer of data packets to or from sources.
5 – Presentation	Application	Used to manipulate or analyze the data packets.

Each process begins with encoding in which the data is organized into packets before it is sent through the data link to a network. Once the device is recognized on the network (through an IP address) data transmission can occur. In order for the destination to be selected and the device to be recognized, the NetBIOS protocol translates any present NetBIOS names to IP addresses and the target source's application may receive the data packet for further processing. Once resolved, the

NetBIOS to IP address conversion is cached for future transmissions. All other processes repeat for each data packet sent.

UDP Configuration

Given this basic understanding of a Network (IP) address, subnet mask, gateway, MAC address, and the various protocols, we can now look at the default configuration of the UDP Ethernet interface.

Initialization

Upon initializing, the UDP interface will attempt to locate a DHCP server to dynamically assign an IP address to the device. If a DHCP server is available, a dynamically allocated IP address is assigned to the interface and NetBIOS is used to associate the interface IP address with a unique name, the NetBIOS name.

If no DHCP server responds, the device falls back on the following static IP configuration which is also associated with the NetBIOS name:

IP Address: 10.1.0.100

IP Mask: 255.0.0.0

Gateway: 10.1.0.1

NetBIOS Name

The default NetBIOS name associated with the IP address is set by TDT. All RZ processor devices equipped with the UDP Ethernet interface will use this standard NetBIOS Name structure:

TDT_UDP_MD_XXXX

M = the model of the device, e.g. '2' for an RZ2, '5' for an RZ5, '6' for an RZ6, 'D' for an RZ5D

D = the number of RZ processor DSPs

XXXX = last 4 digits the RZ processor device serial number

For Example:

An RZ2-4 (4 DSP) with a serial number of 1234 uses a NetBIOS name of:

TDT_UDP_24_1234

An RZ5D with a serial number of 1011 uses a NetBIOS name of:

TDT_UDP_D3_1011

Note: Devices equipped with a UDP interface that have a serial number less than 2012 use a different NetBIOS name format.

Although a default NetBIOS name is assigned. The name can be changed using the UDP Web Interface, see “Configuring the UDP through the Web Interface” on page 58 for more information.

Note: When connecting the RZ, be sure the network mask is set to a Class C or smaller network. A Class A network mask (255.0.0.0) will disable NetBIOS naming on the PC Ethernet interface. In such cases, the IP address of the UDP Ethernet interface must be specified instead.

Configuring the UDP through the Web Interface

Every RZ UDP interface contains a minimal web server which is used to configure the UDP and serial interfaces. Configuration options can be set here if no DHCP server is available. If a DHCP server exists, the NetBIOS name associated with the dynamically assigned IP address can be configured here.

Note: The web interface is only enabled for one minute after powering up the RZ, unless it is in use, in which case it remains enabled until the RZ is turned off. Loading pages through the web interface while collecting data is discouraged and may cause packet loss.

To connect to the UDP Ethernet interface server:

1. Make sure there is an active connection from the PC to the UDP Ethernet port on the back of the RZ then open an Internet browser such as Internet Explorer or Mozilla FireFox.
2. Enter the device's IP address (if known) as the web address (e.g. http://10.1.0.100) and click **Enter**.

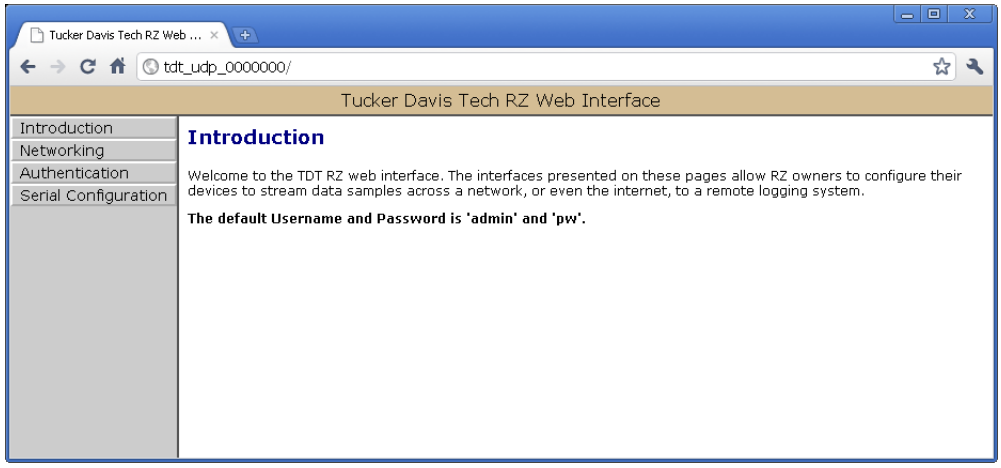
   or

   Enter the NetBIOS name as the web address (e.g. TDT_UDP_0000000) and click **Enter**.

Once properly connected, navigation to the UDP web interface loads the Introduction page. Clicking the links to the left of the web interface loads the corresponding page.

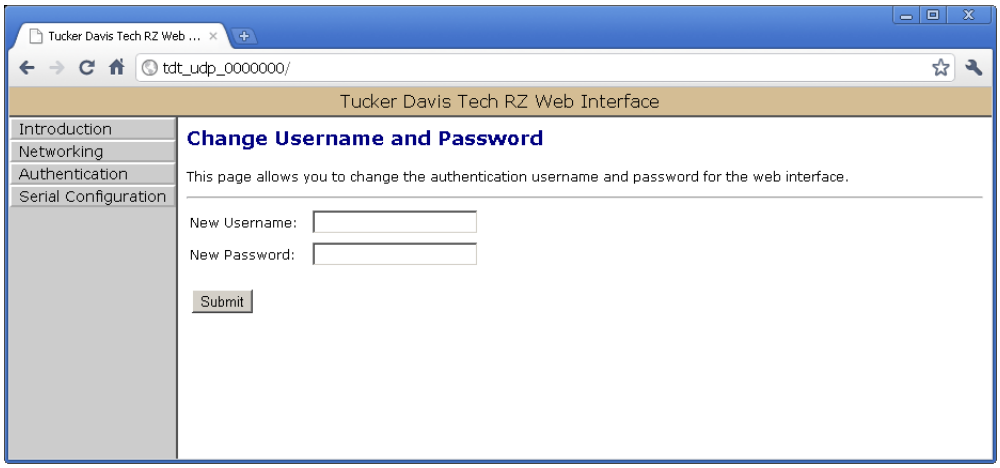
Introduction Page

The Introduction page provides basic information, including the default username and password. The login information can be changed on the Authentication page.



Authentication Page

The Authentication page allows users to change their username and password provided they enter the currently set username and password.



Note: Any server pages that modify the device configuration require a username and password.

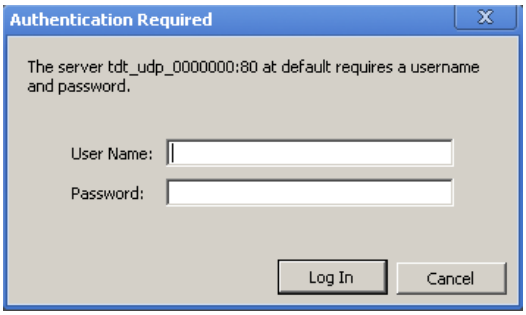
Default Username: **admin**

Default Password: **pw**

To change the Username and Password:

1. Click the **Authentication** link on the left side of the UDP server web page.

   You will be prompted to enter the current username and password.



2. Enter the current **username** and **password**.
3. Click **OK**.
4. Enter the desired new username and password.
5. Click the **Submit** button.

Note: Once changed, you may need to re-enter the new username and password to access the network configurations or Authentication pages.

Network Configurations Page

This page contains settings for configuring the UDP interface.

To change the network configuration:

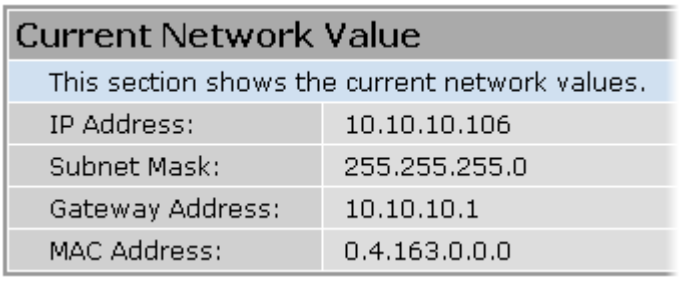
1. Click the **Networking** link on the left side of the UDP server web page.

   If you have not already entered the username and password, the authentication dialog box will prompt.

2. Enter the username and password to access the Networking page.

Current Network Value

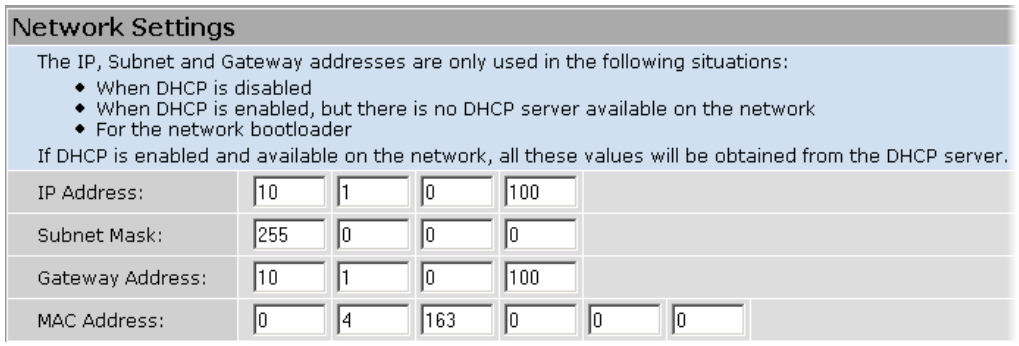
Current IP settings are displayed in this area.



Settings for configuring the static IP address, subnet mask, gateway address, and MAC address are located in the "Network Settings" area.

Network Settings

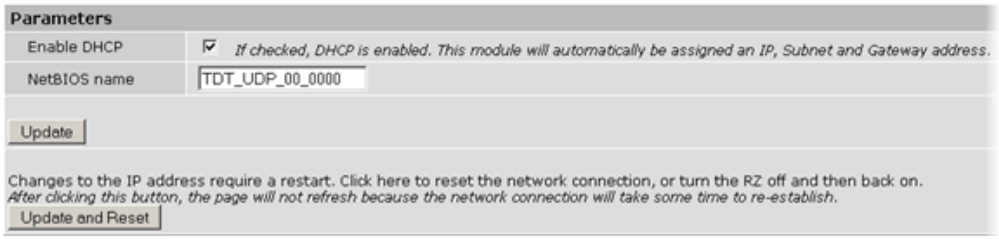
This area contains settings for configuring the UDP interface in the event that no DHCP server is detected. If the Enable DHCP check box is checked (see following Parameters diagram), the "IP Address", "Subnet Mask", and "Gateway Address" values are overridden and automatically configured by the DHCP server if available.



Note: These settings are reserved for connections that cannot locate a DHCP server. If no DHCP server can be detected contact your network administrator for applicable settings.

Parameters

This area contains settings for enabling DHCP or renaming the NetBIOS name.



To Change the NetBIOS name:

- Type the desired NetBIOS name in the **NetBIOS name** textbox and click the **Update** button.

  or

- Type the desired NetBIOS name in the **NetBIOS name** textbox and click the **Update and Reset** button.

The Update and Reset button saves the current configuration settings and performs a soft reset of the UDP interface to load the current settings.

Note: The NetBIOS name can be no greater than 15 characters long and cannot contain spaces or the following characters: \ / : * ? " ; | -

Note: A reset circuit is provided with the TDT driver installation and can be found in:

C:/TDT/RPvdsEx/Support/

Running this circuit on the device with the UDP interface will reset the NetBIOS name to the factory default setting described on "NetBIOS Name" on page 1-57.

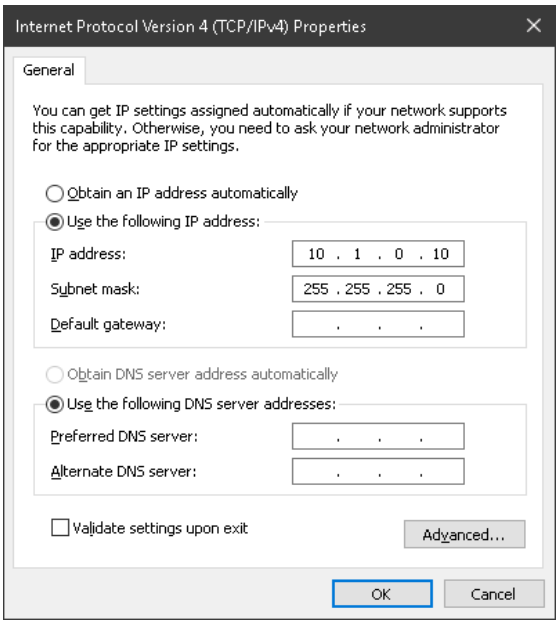
Direct Connection to a PC

The UDP interface can be connected directly to a PC or laptop. Once connected, several steps are required in order for the PC to recognize to the UDP interface connection. This method may be performed on any operating system which supports TCP/IP.

To initialize the PC for a direct connection in Windows 7:

1. Physically connect the UDP interface and the PC via an Ethernet cable.
2. Open **Control Panel** then double-click **Network and Sharing Center**.
3. Click the desired connection link (this is usually a Local Area Connection).
4. In the status dialog, click the **Properties** button.
5. In the item list, select Internet Protocol (TCP/IP) or if there are multiples, select Internet Protocol (TCP/IPv4).
6. Click the **Properties** button.
7. Select **Use the following IP address** and enter these values:

   IP address: 10.1.0.x, where x can be any value, 1 to 254, except 100
   Subnet mask: 255.255.255.0
   Default gateway: Leave empty



8. Click **OK**.

The UDP interface connection should now be recognized by the PC. Cycle power on the RZ device, the IP address of the RZ will be 10.1.0.100.

Serial Configuration

The Serial Configuration page on the web interface contains settings for configuring the serial interface.

Note: If installed in an RZ with 4 optical DSP cards, the serial port is not available.

To change the serial configuration:

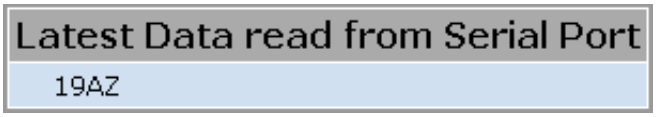
1. Click the **Serial Configuration** link on the left side of the UDP server web page.

   If you have not already entered the username and password, the authentication dialog box will prompt.

2. Enter the username and password to access the Serial Configurations page.

Latest Data Read from Serial Port

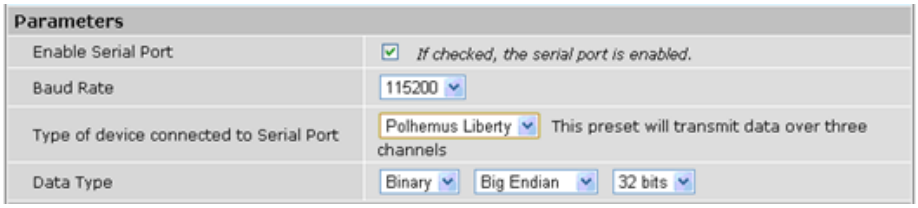
If any data has been sent to the RZ serial port, the latest value will be displayed in this area. ASCII characters represent each byte.



Settings for enabling the serial port, setting baud rate, setting data type and command formats are located in the Serial Port Settings area.

Parameters

The user can enable/disable the serial port, specify the baud rate, and select from a list of preset values.



Data Type

Big vs Little Endian

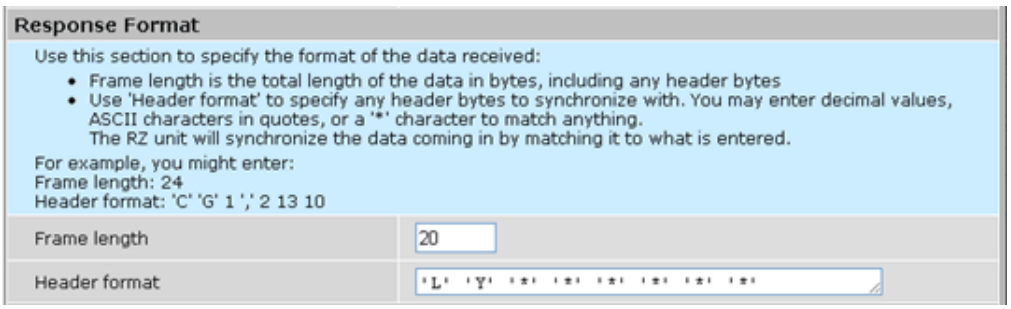
If the device attached to the RS232 connection sends the lower byte before the upper byte, set this to Little Endian. Otherwise, use Big Endian.

8 vs 16 vs 24 vs 32 bit words

This field specifies the length of the data words that the device attached to the RS232 connection is sending. If the data being received is less than 32 bits in length, it is 0 padded out to 32 bits.

Response Format

This area contains configuration settings for the data received from the peripheral device. As data is received over the RS232 connection, it is matched against a user-specified sequence of header bytes at user specified intervals. For example, the user could set the connection to match two specific header bytes, process the next four bytes as data and then start the process over again.



Frame Length

Enter the total length of a 'frame' of data, including any header bytes. In the example shown in the image above, three channels of 32 bit data are being sent, for a total of 12 data bytes (32 bits = 4 bytes). In addition, there are 8 'header' bytes that the user wants to synchronize with, bringing the total frame byte count to 20. The Frame Length, the word size, and the size of the header bytes are used to determine the number of channels being sent and which channel each data byte belongs to.

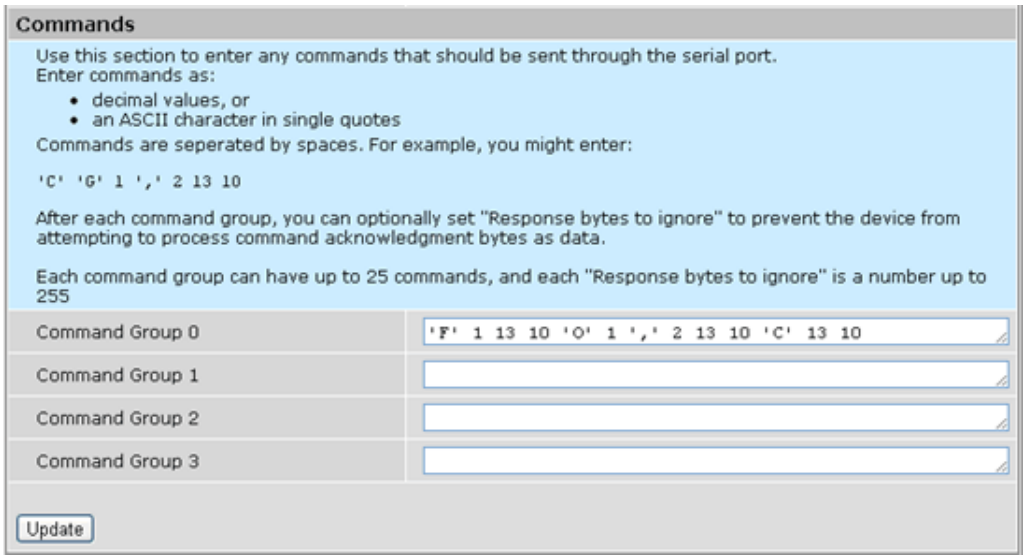
Header Format

If this field is empty, no synchronization will occur, and everything sent over the RS232 connection will be processed. Otherwise, the RZ will look for the specified sequence of bytes at the beginning of each frame. The user can enter a decimal value or any ASCII character in single quotes (e.g. 'A'). The '*' character is reserved as a wilard character that will match anything.

Note: If the received data/headers do not match the expected format, they are discarded and all synchronization information is reset. The RZ will then wait until 10 consecutive successful synchronizations before processing any further data bytes.

Commands

This area is used to configure any commands that the RZ needs to send over the serial port. Use this section if the peripheral device connected to the RS232 accepts special requests, such as an initialization command, start/stop command, or reset command.



Command Groups

The format of this section is similar to the header format. The user can enter a decimal value or any ASCII character in single quotes, but the '*' no longer takes on any special meaning here. Each of the command groups is tied to a trigger in the RZ_Serial_Rec or RZ_Serial_Send macros. When triggered, the specified sequence of bytes/characters will be sent over the RS232 connection.

The UDP Packet Structure

All data sent or received by the UDP Ethernet interface is in the form of a packet. Every packet has a standard structure which includes a 4 byte header followed by n x 4 bytes of data, where n is the total number of channels.

Note: The term packet refers to a header and number of single sample values sent. Each channel sends a single sample. The packet size is therefore equivalent to the number of channels and is measured in 32-bit words.

For Example:

Sending 16 channels (a packet size of 16, 32-bit words) will produce a packet of 68 bytes.

4 byte header + (16 channels x 4 bytes) = 68 bytes.

Header Format

The packet header precedes a new packet and stores information about the packet and its intended command for the UDP interface. The structure for the packet header is shown below.

4 Byte Packet Header (32 bits)

0x55	0xAA	Cmd	Num

The upper two bytes, "55AA" are reserved and required by hardware. The lower two bytes are used for specifying a UDP command (Cmd) and the number of 4 byte

data packets (Num) that are to be expected following the header. For all data samples, "Cmd" must be set to 0.

For Example:

The previous example which sent a packet size of 16 channels would use the 32-bit header:

55 | AA | 0x00 | 0x10

Where the "Num" value 0x10 = 16 (the number of channels).

UDP Interface Commands

There are 4 commands that can be specified for the header byte labeled "Cmd".

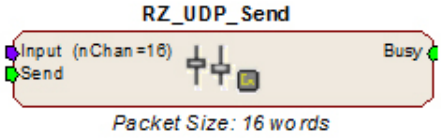
Name	Hex Code	Description
DATA_SEND	0x00	Data is being sent, the byte labeled "Num" contains the number of data packets following the current header.
GET_VERSION	0x01	Retrieve the protocol version supported by the UDP interface.
SET_REMOTE_IP	0x02	Sets the target for receiving packets from the RZ. The IP and port of the machine sending this packet will be used as the new target.
FORGET_REMOTE_IP	0x03	Clears the target IP and port, thereby stopping the flow of packets.

UDP Circuit Design

Access to the UDP interface is provided through two RPvdsEx macros: RZ_UDP_Send and RZ_UDP_Rec. Both macros operate on multi-channel data and can be configured to specify the number of channels. The channel count corresponds to the size of the underlying UDP packets.

RZ_UDP_Send Macro

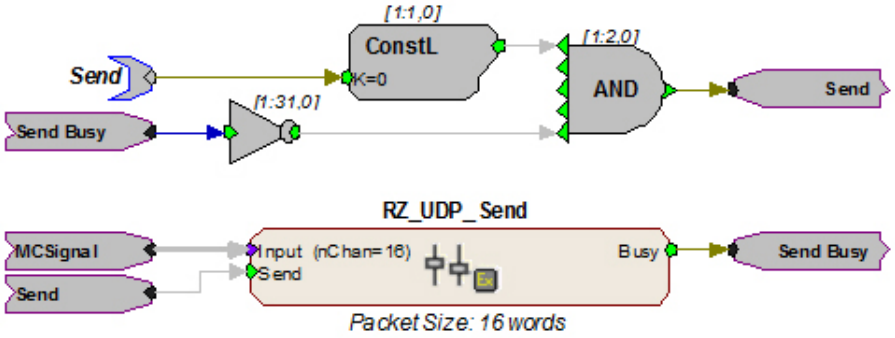
The RZ_UDP_Send macro is used to send data from the RZ across a network. All data is organized into packets according to the number of words (specified by the packet size) set in the macro setup properties dialog. The macro accepts a multi-channel data stream as well as a logic input that tells the macro to send out a packet. An output labeled "Busy" indicates if the macro is currently in the process of sending out a packet.



Sending Data Construct

Data is sent on the rising edge of the "Send" input. The duration of the busy signal is then dependent on the number of channels to send (packet size). It takes N+1samples to send a packet, where N is the packet size.

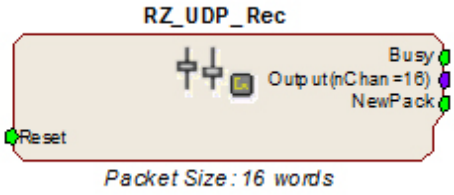
Note: Since the data packets are sent serially, multi-channel data is not sent at the same time. This means that there will be a time shift of multiple samples in multi-channel data.



In this construct, the parameter tag "Send" is used to enable data transmission. The Send input on the RZ_UDP_Send macro is only pulsed when the Send parameter tag is high (1) and the macro is not already sending a packet (Busy = low (0)). Data is input from the HopIn component labeled MCSignal.

RZ_UDP_Rec Macro

The RZ_UDP_Rec macro is used to receive data packets from across a network to the RZ. All data is organized into packets according to the number of words (specified by the packet size) set in the macro setup properties dialog. The macro outputs a latched multi-channel data stream and status lines. An output labeled "Busy" is used to determine if the macro is currently in the process of receiving a packet. Another output labeled "NewPack" is used to denote that a new packet header has been received. The "Reset" input can be used to reset the macro or halt any data transfer.

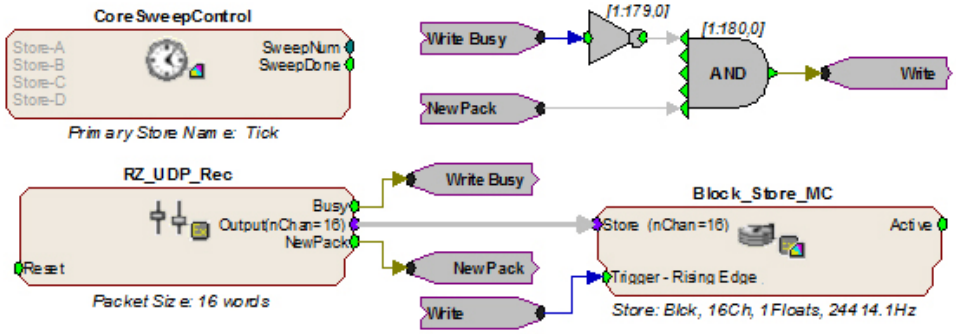


Receiving Scalar Data Construct

When data is received, the NewPack signal will output a logic high (1) for one sample denoting that a packet header has been found. As data is being received, the Busy signal will output logic high (1). The Busy signal will then remain high until the entire packet has been received. The duration of the busy signal is dependent on the number of channels (packet size).

If reset goes high (1) at any time, receiving data is halted and the macro will wait until a new header is found. Any data that was received will still be available on the multi-channel output.

Note: Since the channels are received serially, all channels are not received at the same time. Data received in later channels occurred several samples before it is available on the Output.



In this example, whenever a packet header is detected the Block_Store_MC macro saves the specified packet size as a single block. The Block_Store_MC macro is configured for 16 channels of 32-bit floats.

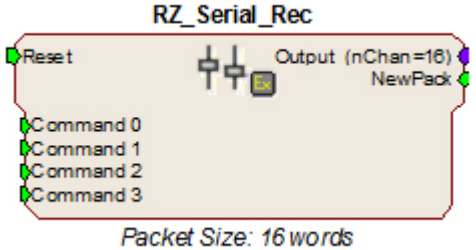
Note: To modify the number of channels received, edit the Packet Size parameter found in the RZ_UDP_Rec macro setup properties. Remember to also edit the number of channels in the Block_Store_MC macro.

Serial Circuit Design

Access to the Serial interface is provided through two RPvdsEx macros: RZ_Serial_Send and RZ_Serial_Rec. Both macros operate on multi-channel data and can be configured to specify the number of channels. This channel count corresponds to the size of the underlying serial stream.

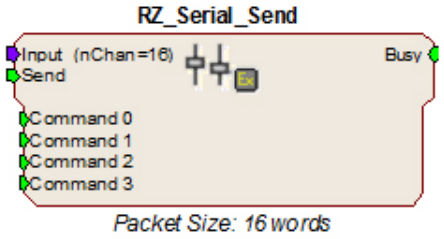
RZ_Serial_Rec Macro

The RZ_Serial_Rec macro is used to receive serial data from the RS232 connection and can also be triggered to send preset commands over the RS232 connection. The number of channels received by the hardware is set in the web configuration. Make sure the packet size set in the macro is at least as large as the value set in the web configuration, otherwise some channels will have missing or incorrect data. If packet size is larger than the number of channels being sent, any excess channels will simply read 0.



RZ_Serial_Send Macro

Use the RZ_Serial_Send macro to send more than just the preconfigured commands over RS232. If using both the RZ_Serial_Rec and RZ_Serial_Send in the same circuit you must disable the Commands in the RZ_Serial_Rec macro options.



Sending Data Construct

Data is sent whenever the "Send" input receives a rising trigger (logic high (1)). The duration of the busy signal is then dependent on the number of channels to send (packet size). Each logic high pulse sent to the send input results in one send packet request. This means that each packet sent results in one sample sent per channel.

Note: Since the data packets are sent serially, multi-channel, non-scalar data is not sent at the same time. Each time a packet is sent, the macro sends a single sample from each channel serially. This means that there will be a time shift present in multi-channel, non-scalar data consisting of multiple samples.

In this construct, the parameter tag "Send" is used to enable data transmission. The Send input on the RZ_UDP_Send macro is only pulsed when the Send parameter tag is high (1) and the macro is not already sending a packet (Busy = low (0)). Data is input from the HopIn component labeled MCSignal.

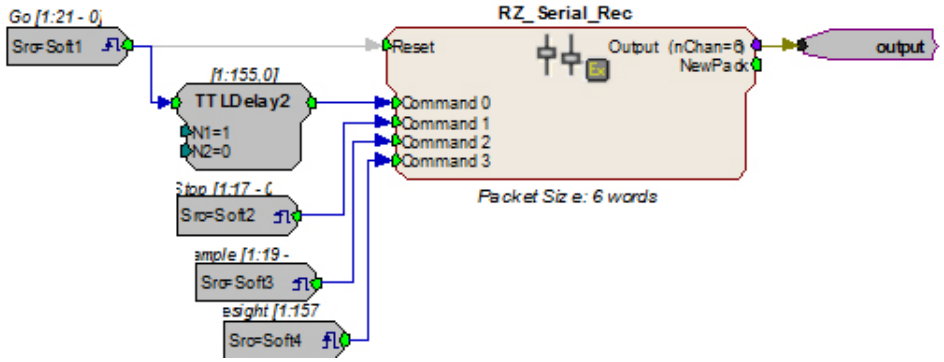
Note: To modify the number of channels sent, (packet size) edit the Packet Size parameter found in the RZ_UDP_Send macro setup properties.

Receiving Scalar Data Construct

When data is received, the NewPack signal will output a logic high (1) denoting that a packet header has been found. As data is being received, the Busy signal will output a logic high (1) and as soon as the header has been received, NewPack will go low (0). The Busy signal will then remain high until the entire packet has been received. The duration of the busy signal is then dependent on the number of channels to send (packet size). Each high duration of the Busy signal results in one received packet. This means a single packet received results in one sample received per channel.

If reset goes high (1) at any time, receiving data is halted and the macro will wait until a new header is found. Any data that was received will still be available on the multi-channel output.

Note: Since the data packets are received serially, multi-channel data is not received at the same time on the Output. There will be a time shift in channels two and higher directly proportional to the channel number.



In this circuit construct, software triggers are used to send commands to the peripheral device (head tracker). The multi-channel output contains the tracking information and can be further processed and/or stored to the data tank.

UDP Test Application

In addition to the RPvdsEx macros, the UDP Ethernet interface also provides a software test application which can be used to connect to a specified UDP interface in order to send or receive packets from an RZ multi-processor device. The UDP Test Application was written in MSVC++ to illustrate the portability of the UDP Ethernet interface.

The UDP Test Application is installed to: C:\TDT\RPvdsEx\Examples\RZ UDP\

Running the Application

Once the application is running, connecting to a UDP interface and sending, or receiving packets from an RZ processor is extremely easy.

Packets can be loaded, saved, and edited. Additionally, the packet format can be converted to double or integer format.

To load an existing packet configuration:

1. Select **Open** from the **File** menu.
2. Browse to the desired *.hex file and click the **Open** button.

   The specified *.hex file will now display any packet information.

To save a packet configuration:

1. Select **Save** or **Save As** from the **File** menu.
2. Type the desired name of the *.hex file and click the **Save** button.

To create a new packet:

1. Double-click anywhere in the packet window to access the **Edit Values** dialog box.

   or

   Right-click the packet window to access the **Packet Dialog** menu.
2. Select the **New Packet** option. This prompts the **Edit Values** dialog box.

To edit an existing packet:

1. Select the desired packet and right-click to access the **Packet Dialog** menu.

2. Select the **Edit Packet** option. This prompts the **Edit Values** dialog box.

To convert the Test Application packet format:

1. Right-click the packet window to access the **Packet Dialog** menu.
2. Select **Convert To**.
3. Select the desired format for the selected packet.

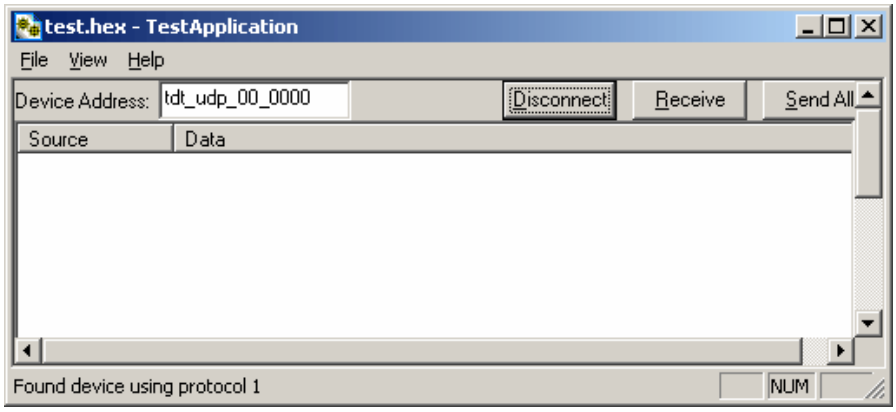
Example: Using the Test Application

In this example we will send packets from the PC to an RZ through the UDP interface.

To establish a connection to the RZ:

1. First, run the Test Application by double-clicking the **TestApplication.exe** icon.
2. Enter the **NetBIOS** name or **IP address** of the RZ processor you wish to send a packet to in the **Device Address** text box.
3. Click the **Check** button.

   A connection is established and the status bar indicates a device has been found. Packets may now be received or sent from this RZ processor.

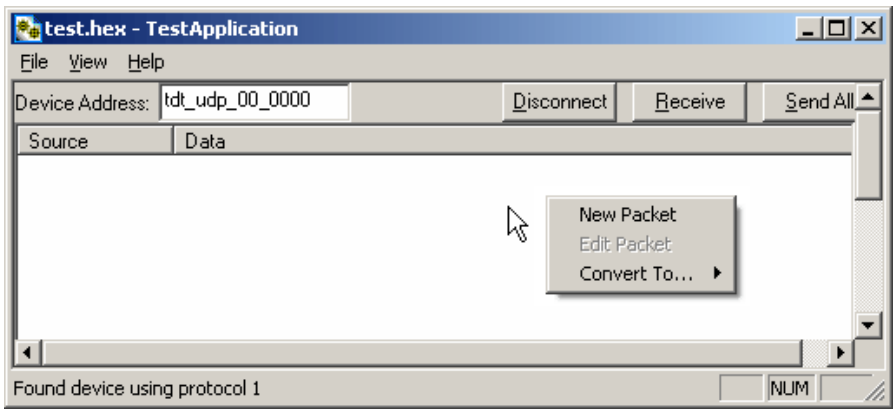


To send a data packet to the RZ processor:

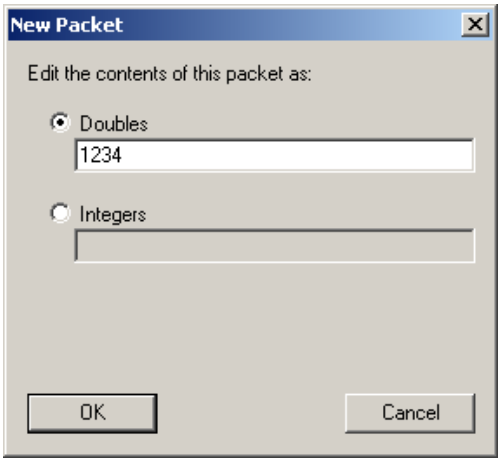
1. Double-click anywhere in the Test Application packet window.

   or

   Right-click to bring up a selection dialog box and select **New Packet**.

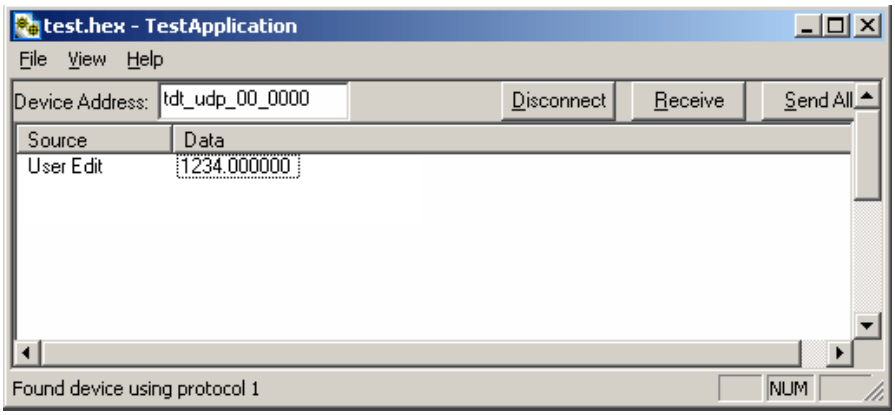


   This prompts a dialog box where values can be edited.



2. Click the **Doubles** radio button and enter "**1234**".
3. Click **OK**.

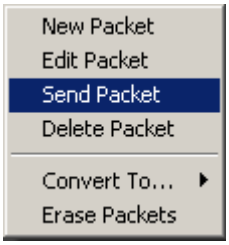
   The configured data packet is shown in the Test Application packet window.



4. Click the **Send All** button to send all data packets to the RZ processor.

   or

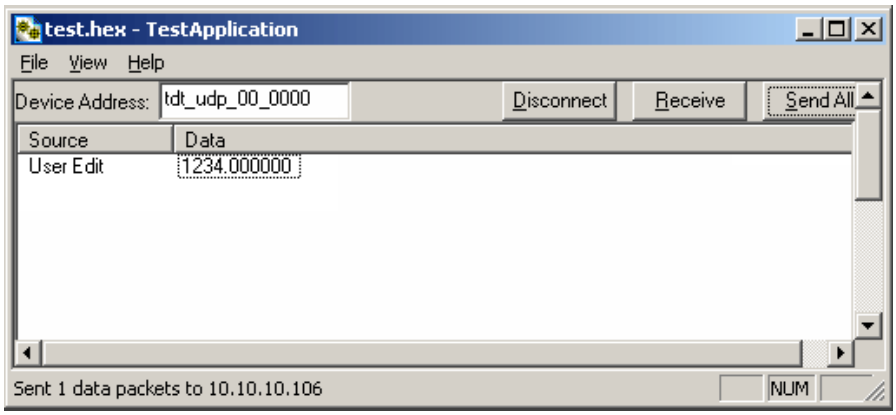
   Send an individual packet by right-clicking on the desired packet and selecting **Send Packet** from the Packet Dialog menu.



   The status bar displays that the packet was sent to the RZ processor. Data packets are received through RPvdsEx using the RZ_UDP_Rec macro.

To receive a data packet sent from the RZ processor:

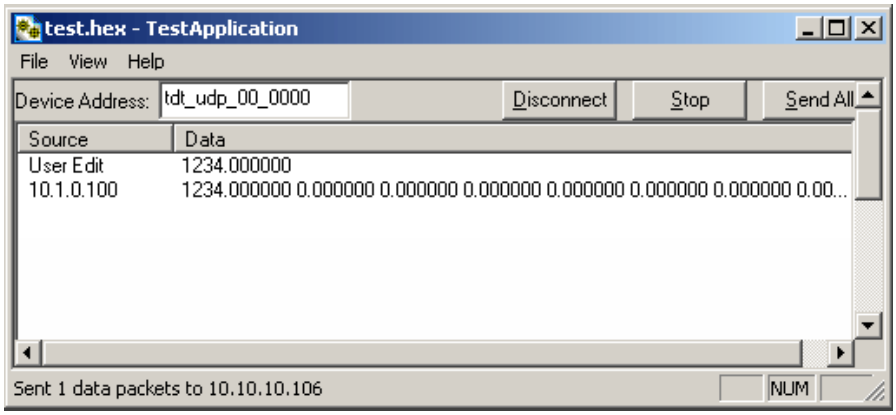
1. First, run the Test Application by double-clicking the **TestApplication.exe** icon.



2. Enter the **NetBIOS** name or **IP address** of the RZ processor you wish to send a packet to in the **Device Address** text box.
3. Click the **Check** button.
4. Click the **Receive** button.

   The button changes to **Stop** in order to notify that it is waiting for a data packet to be sent from the RZ processor. Data packets are sent through RPvdsEx using the RZ_UDP_Send macro.
5. At this time you may configure the circuit to send a data packet from the RZ processor to the Test Application.

   Once received, the data packet will be displayed in the Test Application packet window. The Source column will display the IP address the data packet was received from while the Data column displays the data packet itself.



The Test Application runs separate threads for sending and receiving data so it is possible to listen (wait for a data packet to be received) while sending, connecting to a device, or disconnecting from a device.

Writing a Custom Software Application

The Test Application is designed to be used as a diagnostic tool for the UDP Ethernet Interface. Custom software applications are fully supported for any computer language that supports IP network protocols. Several basic steps are required in order to configure the UDP interface for sending and receiving data packets as illustrated in the following Python code.

The basic initialization script below must be included to initialize the UDP interface:

```
# import network methods
import socket

# UDP command constants
CMD_SEND_DATA          = 0x00
CMD_GET_VERSION        = 0x01
CMD_SET_REMOTE_IP      = 0x02
CMD_FORGET_REMOTE_IP   = 0x03

# enter RZ's IP address or NetBIOS name here:
TDT_UDP_HOSTNAME = 'TDT_UDP_0000000'

# Important: the RZ UDP interface port is fixed at 22022
UDP_PORT = 22022

# create a UDP socket object
sock = socket.socket( socket.AF_INET,      # Internet
                      socket.SOCK_DGRAM ) # UDP

# connect the PC to the target UDP interface
sock.connect((TDT_UDP_HOSTNAME, UDP_PORT))

# configure the header. Notice that it includes the
header

# information followed by the command 2 (set remote IP)

# and 0 (no data packets for header).
packet = struct.pack('4B', 0x55, 0xAA, CMD_SET_REMOTE_IP,
0)

# Sends the packet to the UDP interface, setting the
remote IP

# address of the UDP interface to the host PC
sock.send(packet)
```

The code above simply sends a command packet to the UDP interface listening Port (22022) and tells it to set the UDP interface remote IP to the host PC IP address. Once this has been done, any data packets sent by the UDP Ethernet interface will go to this IP address.

Note: The listening port on the UDP Ethernet interface is 22022 and cannot be changed.

The code structure below is necessary to receive a packet from the UDP interface:

```
while 1:

    # Receive a data packet from the UDP interface
    packet = sock.recv(1024)

# Process received packet
```

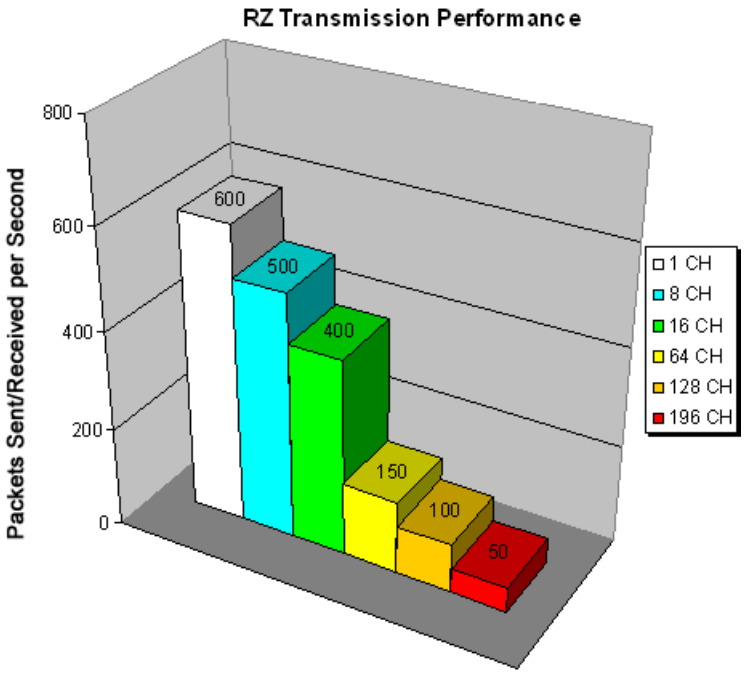
```
    # ...
```

The code structure below is necessary to send a packet of 16 channels to the UDP interface:

```
# begin sending data
NPACKETS = 16

# configure the header. Notice that the command is now 0

# (sending data packets) and the number of packets
following is 16
header = struct.pack('4B', 0x55, 0xAA, CMD_SEND_DATA,
NPACKETS)
count = 0
while 1:

    # this example uses fake data
    fakeval = count % 10
    data = range(fakeval, NPACKETS + fakeval)
    # append sixteen 32-bit words to the header

    # '>' in the format string is used to force big-endian
    packet = struct.pack(">%di" % len(data), *(i for i in
data))
    # send the data packet to the UDP interface.
    print 'sending packet', count, '...'
    sock.send(header + packet)
count += 1
    # slow it down for demonstration purposes
    time.sleep(.2)
```

UDP Interface Performance

The UDP interface is a 10Mb Ethernet interface, but the usable bandwidth is significantly lower due to limitations of the Ethernet hardware. A graph below displays the expected throughput for different numbers of packets sent or received per second depending on the number of channels transmitted on an RZ processor.



The bandwidth for transmitting data from an RZ through the UDP interface decreases depending on the width (or number of channels) of packets sent or received. Transmission of a single packet (single channel) provides a high amount of data resolution since the packets are transmitted at a much higher rate and would respond quickly to abrupt changes in value. Transmitting multiple packets (large number of channels) allows more information to be sent in parallel but reduces data resolution.

Relative Performance

A typical application might involve sending a packet size of 16 channels 100 times per second or a packet size of 100 channels 10 times per second. As shown in the diagram above, the UDP interface will be able to send a packet size of 16 channels 400 times per second or a packet size of 128 channels 100 times per second.

As a result, the UDP performance is relative to the size of the packet, dictated by the number of channels transmitted.

Typical RZ Transmission Performance with the RZUDP-20 Table

The table below displays the expected throughput for different numbers of packets sent or received per second depending on the number of channels transmitted on an RZ processor.

Number of Channels (32-bit Words)	Packets Sent/Received per Second
1	600
8	500
16	400

Number of Channels (32-bit Words)	Packets Sent/Received per Second
32	300
64	150
128	100
192	50

Technical Specifications

Interfaces	Standard Ethernet (for direct connections to a PC an Ethernet crossover cable is required) RS-232 Serial Port (9-Pin)
Ethernet Speed	10 Mbps
Serial Speed	115,200 bits/sec
Supported Network DHCP (Dynamic Host Protocols	Configuration Protocol), UDP, HTTP (for configuration)
Transfer Rates	Dependent on data packet size (see Typical RZ Transmission Performance with the RZUDP-20 Table above)

RZ5P Fiber Photometry Processor

RZ5P Overview

The RZ5P Processor is equipped with two 400 MHz Sharc digital signal processors networked on a multiprocessor architecture that features efficient onboard communication and memory access. The RZ5P is an optimized solution for fiber photometry and multi-channel neurophysiology.

The RZ5P features four channels of analog input and four channels of analog output. Its fiber optic input port can acquire up to 32 channels of neurophysiological signals to be processed in real-time. Data can be input from a PZ amplifier at a sampling rate of up to ~50 kHz. The RZ5P also features 24-bits of digital I/O and an onboard monitor speaker with volume control.

This manual provides hardware information for the RZ5P. For a full application guide specific to fiber photometry using the RZ5P, see the Fiber Photometry User Guide for RZ5P.

Power and Communication

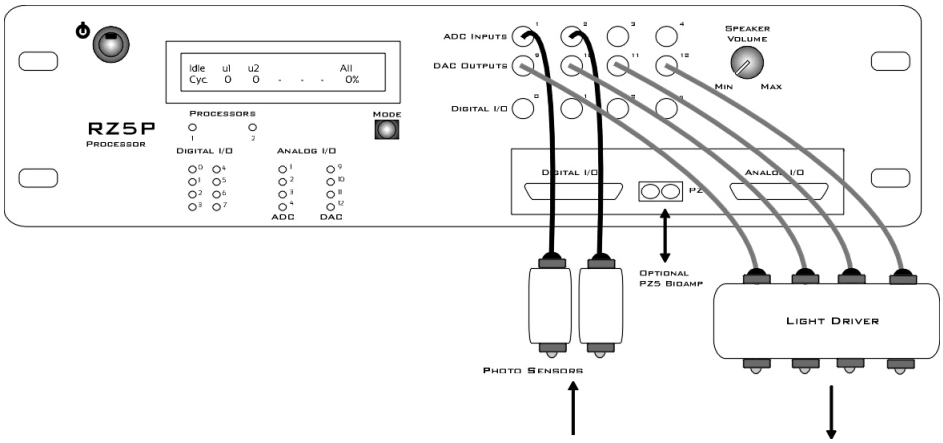
The RZ5P's integrated Optibit optical interface ensures fast and reliable data transfer from the RZ5P to the PC. Connectors are provided on the back panel and are color coded for correct wiring. The RZ5P's integrated power supply is shipped from the factory configured for the desired voltage setting (110 V or 220V). If you need to change the voltage setting, please contact TDT support at +1.386.462.9622 or email support@tdt.com.

Software Control

The RZ5P is intended for use with TDT's Synapse software. When custom control is required, see the RZ5D BioAmp Processor section in this manual for details on developing circuits in the System 3's RPvdsEx circuit design software. Note: PZ related macros should be moved to DSP-2 for the RZ5P.

Fiber Photometry Connections

On the front panel of the RZ5P, connect photo sensors to ADC BNCs 1 and 2 and connect light drivers to DAC BNCs 9 - 12.



Fiber Photometry System Connection Diagram

The Analog I/O DB25 connector can also be used for the connections. See "DB25 Analog I/O Pinout" on page 1-82.

RZ5P Features

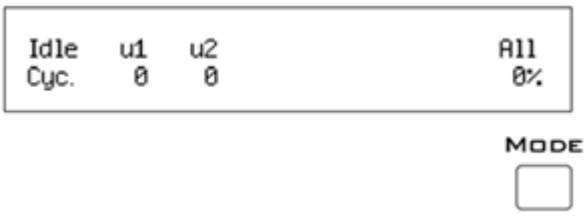
DSP Status Displays

The RZ5P include status lights and a display screen to report the status of the individual processors.

Status Lights

Two LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The corresponding LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second).

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Reset).

Note: When burning new microcode or if the firmware on the RZ5P is blank, the display screen will report a cycle usage of 99% and the processor status lights will flash red.

Status Indicators	Description
Cyc:	processing cycle usage (note: limited to 2 digits; ex: 110 displayed as 10)
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
Opt:	Connection (sync) status of PZ amplifier

Important! The status lights flash when a DSP goes over its processor cycle usage limit, even if only for a particular cycle.

PZ Preamplifier Port

The RZ5P acquires digitized signals from a PZ preamplifier or digital headstage manifold over a fiber optic cable through the port labeled 'PZ' on the front panel. This port can input up to 32 channels at a maximum sampling rate of ~50 kHz. The PZ port can be used with any of the PZ preamplifiers including the PZ2, PZ3, and PZ5 or the PZ4 digital headstage manifold.

Onboard Analog I/O

The RZ5P is equipped with four channels of 16-bit PCM D/A and four channels of 16-bit PCM A/D. All 8 channels can be accessed via front panel BNCs marked ADC and DAC or via a 25-pin analog I/O connector. See the *Synapse Manual* for information on enabling analog I/O.

Monitor Speaker

The RZ5P is equipped with an onboard speaker tied to analog output channel 9. The speaker is provided primarily for audio monitoring of a single channel of input during recording.

Digital I/O

24 bits of programmable digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ5P and bits 0 - 3 of byte C are available through

BNC connectors on the front panel labeled Digital. See "RZ5P Technical Specifications" on page 1-81, for the DB25 pinout and BNC channel mapping.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable
*Note: Byte C Bits 0 - 3 are available via front panel BNCs				

See the *Synapse Manual* for information on enabling digital I/O and configuring data direction.

The RZ5P digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table depicting the different voltage outputs and thresholds for both type.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

LED Indicators

The RZ5P contains 16 LED indicators for the analog and digital I/O. These indicators are located directly below the display screen and DSP status LEDs. They display information relative to the various analog and digital I/O. The following tables illustrate the possible display options and their associated descriptions.

Digital I/O

These LEDs indicate the state of the 8 bit-addressable I/O of byte C.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog I/O

These LEDs indicate state of the ADC and DAC channels.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than +/-100 mV

Light Pattern	Description
Dim Green	Analog I/O channel signal voltage is less than +/-5 V
Solid Green	Analog I/O channel signal voltage is between +/-5 V to +/-9 V
Solid Red	Analog I/O channel clip warning (voltage greater than +/-9 V)

UDP Ethernet Interface (Optional)

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP Communications Interface" on page 1-51, for more information.

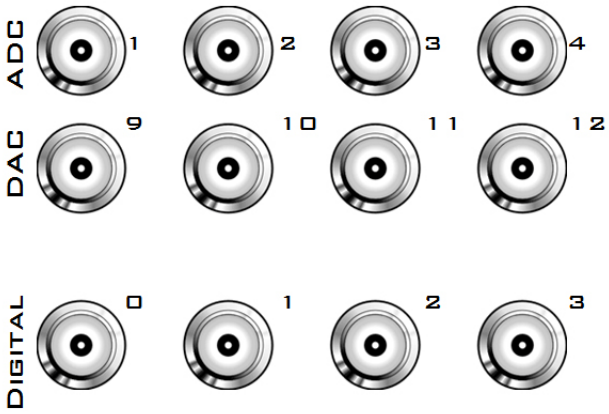
RZ5P Technical Specifications

Note: Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

DSP	Two 400 MHz DSPs, 2.4 GFLOPS peak per DSP
Memory	64 MB SDRAM per DSP
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	10 Ohms
A/D	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Port	One input for PZ5, PZ2, PZ3 or PZ4, up to 32 channels
Digital I/O	8 programmable bits: 3.3 V, 25 mA max load 2 programmable bytes(16 bits): 5.0 V, 35 mA max load

BNC Channel Mapping

Please note channel numbering begins at the top left block of BNCs for both analog and digital I/O and is printed on the face of the device to minimize miswiring.



Maps to:

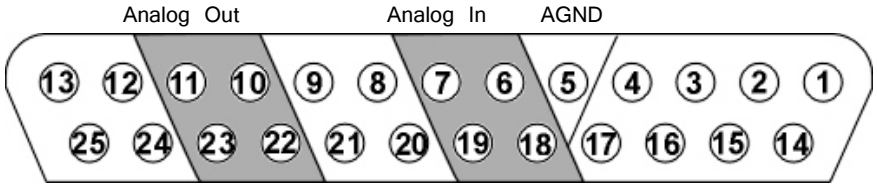
Ch 1-4 Analog In

Ch 9-12 Analog Out

Port C

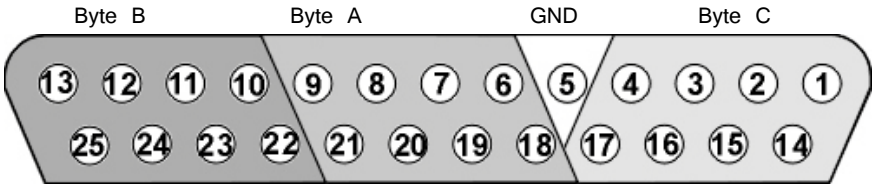
Bits 0-3 Digital I/O

DB25 Analog I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	AGND	Analog Ground		18	A1	ADC Analog Input Channels
6	A2	ADC Analog Input Channels		19	A3	
7	A4			20	NA	Not Used
8	NA	Not Used		21	NA	
9	NA			22	A9	DAC Analog output Channels
10	A10	DAC Analog Output Channels		23	A11	
11	A12			24	NA	Not Used
12	NA	Not Used		25	NA	
13	NA					

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable Digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Byte A Word Addressable Digital I/O Bits 1, 3, 5 and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Byte B Word Addressable Digital I/O Bits 1, 3, 5 and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

RZ5 BioAmp Processor

RZ5 Overview

The RZ5 BioAmp Processor is available with either one or two 400 MHz Sharc digital signal processors networked on a multiprocessor architecture that features efficient onboard communication and memory access. The optimized multi-DSP architecture provides nearly five gigaflops of processing power, making the RZ5 a versatile solution for real-time processing and simultaneous acquisition.

The RZ5 acquires and processes up to 32 channels of neurophysiological signals in real-time. Data can be input from two Medusa preamplifiers at a sampling rate of ~25 kHz. The RZ5 also supports microstimulation applications. The RZ5 can be used with one of TDT's stimulus isolators (MS16 or MS4) to comprise a complete microstimulation system. For more information, see "MS4/MS16 Stimulus Isolator" on page 8-31.

The RZ5 also features eight channels of analog I/O, 24 bits of digital I/O and an onboard monitor speaker with volume control.

Power and Communication

The RZ5's Optibit optical interface ensures fast and reliable data transfer from the RZ5 to the PC and is integrated into the device. Connectors are provided on the back panel and are color coded for correct wiring. The RZ5's power supply is also integrated into the device and is shipped from the factory configured for the desired voltage setting (110 V or 220V). If you need to change the voltage setting, please contact TDT support at 386.462.9622 or support@tdt.com.

The RZ5 is UL compliant, see the *RZ5/RZ5D/RZ6 Operations Manual* for power and safety information.

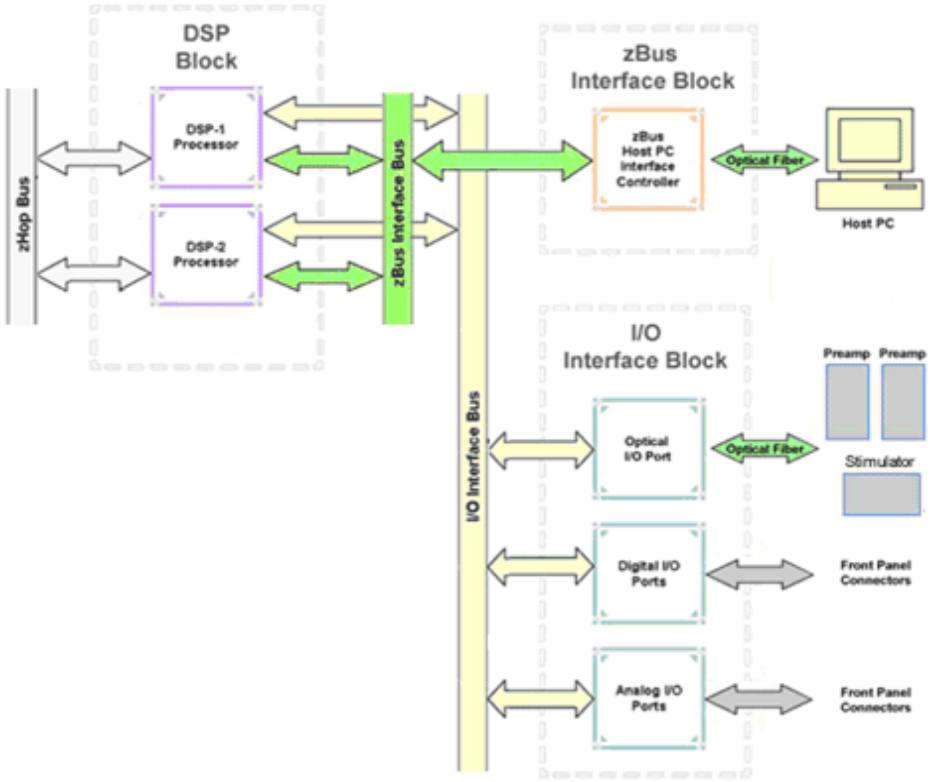
Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-

time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see "MultiProcessor Circuit Design" and "Multi-Channel Circuit Design" in the *RPvdsEx Manual*.

RZ5 Architecture

The RZ5 processor utilizes a multi-bus architecture and offers three dedicated, data buses for fast, efficient data handling. While the operation of the system architecture is largely transparent to the user, a general understanding is important when developing circuits in RPvdsEx.



As shown in the diagram above, the RZ5 architecture consists of three functional blocks:

The DSPs

Each DSP in the DSP Block is connected to 64 MB SDRAM and a local interface to the three data buses: two buses that connect each DSP to the other functional blocks and one that handles data transfer between the DSPs (as described further in Distributing Data Across DSPs below). This architecture facilitates fast DSP-to-off-chip data handling.

Because each DSP has its own associated memory, access is very fast and efficient. However, large and complex circuits should be designed to balance memory needs (such as data buffers and filter coefficients) across processors.

When designing circuits also note that the maximum number of components for each RZ5 DSP is 768.

The zBus Interface The zBus Interface provides a connection to the PC. Data and host PC control commands are transferred to and from the DSP Block through the zBus Interface Bus, allowing for large high-speed data reads and writes without interfering with other system processing.

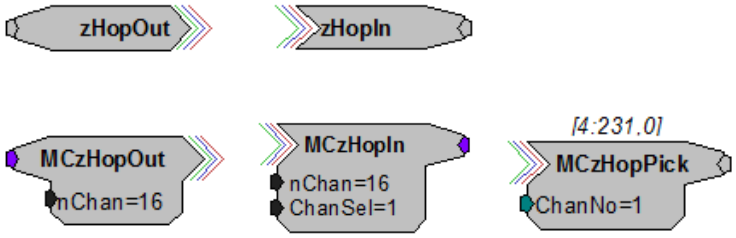
The I/O Interface The I/O Interface serves as a connection to outside signal sources or output devices. It is used to input data from the preamplifier inputs and digital and analog channels. The I/O Interface Bus provides a direct connection to each DSP.

Distributing Data Across DSPs

To reap the benefits of added power made possible by multi-DSP modules, processing tasks must be efficiently distributed across the available DSPs. That means transferring data across DSPs. The RZ5 architecture provides the zHop Bus for this type of data handling.

The zHop Bus

The zHop Bus allows the transfer of single or multi-channel signals between each DSP in the RZ5.



In RPvdsEx data is transferred across the zHop Bus using paired zHop Components, including zHopIn, zHopOut, MCzHopIn, MCzHopOut, and MCzHopPick. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

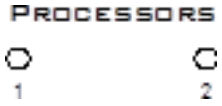
The zHop Bus introduces a single sample delay However, this delay is taken care of for the user in OpenEx when Timing and Data Saving macros are used.

RZ5 Features

DSP Status Displays

The RZ5 include status lights and a display screen to report the status of the individual processors.

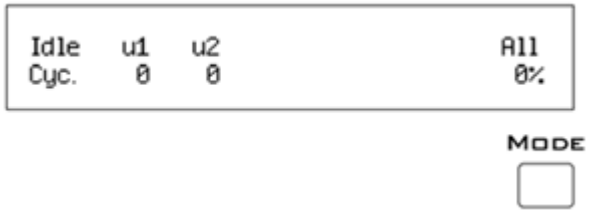
Status Lights



Two LEDs report the status of the multiprocessor's individual DSPs and will be lit solid green when the corresponding DSP is installed and running. The corresponding

LED will be lit dim green if the cycle usage on a DSP is 0%. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash red (~1 time per second).

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run!, Idle, or Reset, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the bottom right of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Reset).

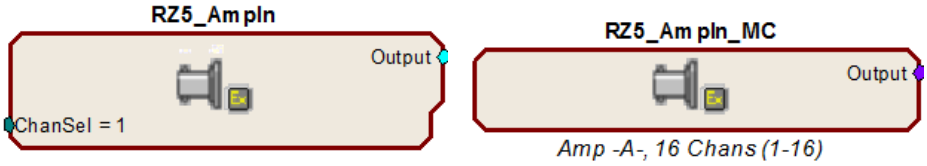
Note: When burning new microcode or if the firmware on the RZ5 is blank, the display screen will report a cycle usage of 99% and the processor status lights will flash red.

Status Indicators	Description
Cyc:	cycle usage (**note:** limited to 2 digits; ex: 110 displayed as 10)
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used
Opt:	Connection (sync) status of amplifiers A and B

Important! Status lights flash when a DSP goes over the cycle usage limit, even if only for a particular cycle. this helps identify periodic overages caused by components in time slices.

Amplifier and Onboard Analog I/O

The RZ5 is equipped with both amplifier input and onboard analog I/O capabilities. The fiber optic ports allow a direct connection to Medusa Preamplifiers. Physiological signals are digitized on the preamplifier and transferred across noiseless fiber optics. The RZ5_AmpIn_MC and RZ5_AmpIn macros automatically apply the necessary scale factors and channel offsets for configuring the preamplifier fiber optic ports.



The following table provides a quick overview of the amplifier and analog I/O features and how they must be accessed during circuit design. When the RZ5_AmpIn_MC and RZ5_AmpIn macros are not used, reference the table and be sure to use the appropriate component, channel offset, scale factor and so forth. Also, see the *RPvdsEx Manual* for more information on circuit design.

Analog I/O	Description	Components	Chan.	Notes
ADC Inputs	Analog Input	AIn	1 - 4	Accessed through ADC Input BNCs or Analog I/O labeled DB25
DAC Outputs	Analog Output	DacOut	9 - 12	Accessed through DAC Output BNCs or Analog I/O labeled DB25
Optical Amp-A	Medusa PreAmp Input	AIn	17 - 32	When the RZ5_AmpIn_MC or RZ5_AmpIn is NOT USED, apply a scale factor of .000833
Optical Amp-B	Medusa PreAmp Input	AIn	33 - 48	When the RZ5_AmpIn_MC or RZ5_AmpIn is NOT USED, apply a scale factor of .000833

Onboard Analog I/O

The RZ5 is equipped with four channels of 16-bit PCM D/A and four channels of 16-bit PCM A/D. All 8 channels can be accessed via front panel BNCs marked ADC and DAC or via a 25-pin analog I/O connector. See "RZ5 Technical Specifications" on page 1-93 for the DB25 pinout.

Fiber Optic Preamplifier Ports

The RZ5 acquires digitized signals from a Medusa preamplifier over a fiber optic cable. This provides loss-less signal acquisition between the amplifier(s) and the base station. Two fiber optic ports are provided to support simultaneous acquisition from up to two preamplifiers. Each port can input up to 16 channels at a maximum sampling rate of ~25 kHz.

The fiber optic ports can be used with any of the Medusa preamplifiers including the RA16PA, RA4PA, or RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Channels are numbered as follows:

Amp-A 17 – 32

Amp-B 33 – 48

Note: When using the RZ5_AmpIn_MC and RZ5_AmpIn macros, the necessary scale factors and channel offsets for configuring the fiber optic ports are automatically applied.

Fiber Oversampling (acquisition only)

The fiber optic cable that carries the signals to the fiber optic input ports on the RZ5 has a transfer rate limitation of 6.25 Mbits/s. With 16 channels of data and 16 bits per sample, this limitation translates to a maximum sampling rate of ~25 kHz.

However, the need may arise to run a circuit at a higher sampling rate while still acquiring data via a fiber optic port. The two fiber optic ports on the RZ5 can oversample the digitized signals that have already been sampled up to 2X or ~50 kHz. This will allow the RZ5 to run a DSP chain at ~50 kHz and still sample data acquired through an optically connected preamplifier that digitized the incoming data stream at its maximum rate of ~25 kHz.

Oversampling is performed on the base station. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

Fiber Optic Output (Stimulator) Port

The output port, labeled Stimulator, can be used to transfer microstimulation waveforms to the Stimulus Isolator and/or to control its digital output.

Important! This fiber optic port is disabled if the sampling rate of the system is set to a value greater than ~25 kHz.

Monitor Speaker

The RZ5 is equipped with an onboard speaker. To use the speaker feed the desired signal to output channel 9 using a DacOut component. The speaker is provided primarily for audio monitoring of a single channel of electrophysiological potentials during recording.

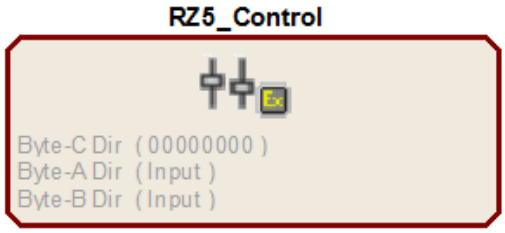
Digital I/O

24 bits of programmable digital I/O is divided into three bytes (A, B, and C) as described in the chart below. All digital I/O lines are accessed via the 25-pin connector on the front of the RZ5 and bits 0 - 3 of byte C are available through BNC connectors on the front panel labeled Digital. See "RZ5 Technical Specifications" on page 1-93, for the DB25 pinout and BNC channel mapping.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

Digital I/O	Description	DB25	BNCs	Notes
Byte A	bits 0 - 7	Yes	No	byte addressable
Byte B	bits 0 - 7	Yes	No	byte addressable
Byte C	bits 0 - 7	Yes	Yes*	bit addressable
*Note: Byte C Bits 0 - 3 are available via front panel BNCs				

The data direction for the Digital I/O is configured using the RZ5_Control macro in RPvdsEx.



Double-click the macro to access the settings on the Digital I/O tab. The RZ5_Control macro also offers a Direction Control Mode parameter that enables the macro inputs and allows the user to control data direction dynamically. For more information on using the RZ5_Control macro see the help provided in the macro's properties dialog box. For more information on addressing and "Digital I/O" see the *RPvdsEx Manual*.

Note: By default, all digital I/O are configured as inputs.

The RZ digital I/O ports have different voltage outputs and logic thresholds depending on the type. Below is a table depicting the different voltage outputs and thresholds for both type.

Digital I/O Type	Voltage Output		Voltage Input	
	logic high	logic low	logic high	logic low
byte addressable	5 V	0 V	≥ 2.5 V	0 - 2.45 V
bit addressable	3.3 V	0 V	≥ 1.5 V	0 - 1.4 V

LED Indicators

The RZ5 contains 16 LED indicators for the analog and digital I/O. These indicators are located directly below the display screen and DSP status LEDs and display information relative to the various analog and digital I/O contained on the RZ5. The following tables illustrate the possible display options and their associated descriptions.

Digital I/O - Byte C

8-bit, bit addressable byte C LED indicators are located to the bottom left of the RZ5 front panel.

Light Pattern	Description
Dim Green	Bit is configured for output and is currently a logical low (0)
Solid Green	Bit is configured for output and is currently a logical high (1)
Dim Red	Bit is configured for input and is currently a logical low (0)
Solid Red	Bit is configured for input and is currently a logical high (1)

Analog I/O - ADC Inputs and DAC Outputs

ADC and DAC LED indicators are labeled and located to the right of the byte C LED indicators.

Light Pattern	Description
Off	Analog I/O channel signal voltage is less than +/-100 mV
Dim Green	Analog I/O channel signal voltage is less than +/-5 V
Solid Green	Analog I/O channel signal voltage is between +/-5 V to +/-9 V
Solid Red	Analog I/O channel clip warning (voltage greater than +/-9 V)

UDP Ethernet Interface (Optional)

The RZ UDP Ethernet interface is designed to transfer data to or from a PC. RZ devices equipped with a UDP interface contain an additional port located on the back panel. See "RZ-UDP Communications Interface" on page 1-51, for more information.

Specialized DSP/Optical Interface Boards (Optional)

The RZ Standard DSP Boards can be replaced with specialized DSP Boards which include an optical interface for communication and control of RZ compatible devices, such as the IZ2 Stimulator and RV2 Video Processor. RZ devices equipped with one or more specialized DSP boards include an optical port for each card. The ports are located on the back panel and labeled for easy identification.

RZDSP-I This board supports the IZ2 Stimulator, allowing the RZ device to function as a controller or base station. See "Software Control" on page 8-11, for more information on using and designing circuits for the stimulator.

RZDSP-P This board supports PZ amplifier input, providing an alternate method for acquiring data from a PZ amplifier. It can be used to expand the number of channels that can be acquired on any RZ processor. Access to this input can be enabled in the PZ control macro.

RZDSP-V This board supports the RV2 Video Tracking System, allowing the RZ device to function as a controller or base station. See "RV2 Video Processor" on page 9-3, for more information on using and designing circuits for the RV2.

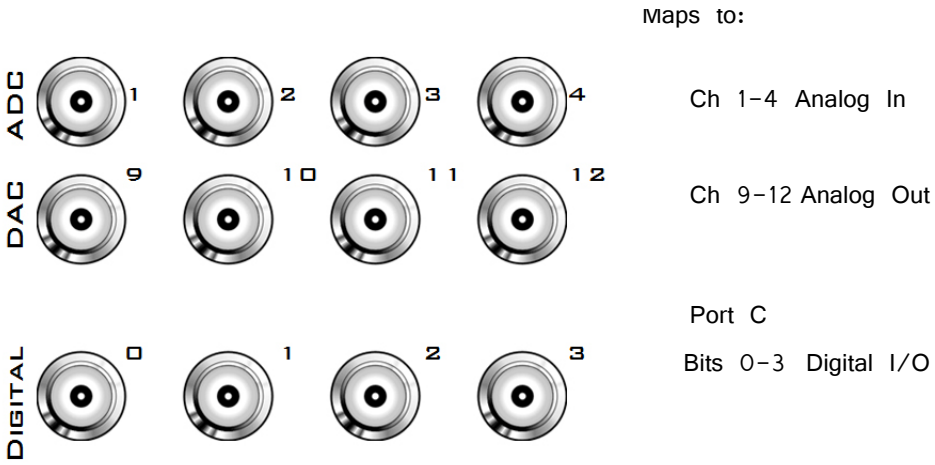
RZ5 Technical Specifications

Note: Technical Specifications for amplifier A/D converters are found under the preamplifier's technical specifications.

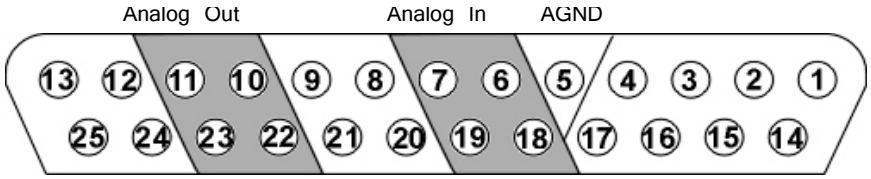
DSP	400 MHz DSPs, 2.4 GFLOPS peak per DSP One or Two
Memory	64 MB SDRAM per DSP
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz*
Frequency Response	DC - 0.44*Fs (Fs = sample rate)
Voltage Out	+/- 10.0 Volts, 175 mA max load
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Output Impedance	10 Ohms
A/D	4 channels, 16-bit PCM
Sample Rate	Up to 48828.125 Hz*
Frequency Response	DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	82 dB (20 Hz - 20 kHz at 9.9 V)
Input Impedance	10 kOhms
Fiber Optic Ports	
Stimulator (MS16)	One output for MS16 Stimulus Isolator When used with the Stimulus Isolator, the sampling rate is limited to 24.414 kHz.
Preamplifier (Medusa)	Two 16-channel inputs
Digital I/O	8 programmable bits: 3.3V, 25mA max load 2 programmable bytes(16 bits): 5.0 V, 35 mA max load
***The Stimulator fiber optic port is disabled if the sampling rate of the system is set to a value greater than ~25 kHz.**	

BNC Channel Mapping

Please note channel numbering begins at the top left block of BNCs for both analog and digital I/O and is printed on the face of the device to minimize miswiring.

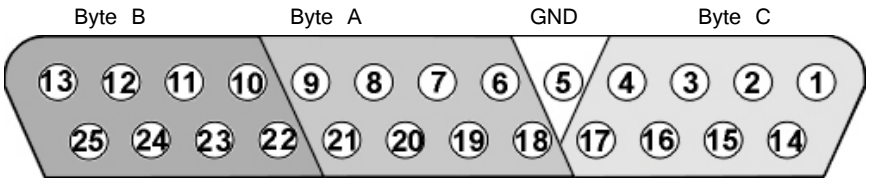


DB25 Analog I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	AGND	Analog Ground		18	A1	ADC Analog Input Channels
6	A2	ADC Analog Input Channels		19	A3	
7	A4			20	NA	
8	NA			21	NA	
9	NA			22	A9	DAC Analog Output Channels
10	A10	DAC Analog Output Channels		23	A11	
11	A12			24	NA	
12	NA			25	NA	
13	NA					

DB25 Digital I/O Pinout



Pin	Name	Description		Pin	Name	Description
1	C0	Byte C Bit Addressable Digital I/O Bits 0, 2, 4, and 6		14	C1	Byte C Bit Addressable Digital I/O Bits 1, 3, 5, and 7
2	C2			15	C3	
3	C4			16	C5	
4	C6			17	C7	
5	GND	Digital I/O Ground		18	A0	Byte A Word Addressable Digital I/O Bits 0, 2, 4 and 6
6	A1	Byte A Word Addressable Digital I/O Bits 1, 3, 5 and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word Addressable Digital I/O Bits 0, 2, 4 and 6
10	B1	Byte B Word Addressable Digital I/O Bits 1, 3, 5 and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

Part 2: Data Streamers

RS4 Data Streamer

RS4 Overview

The RS4 Data Streamer is a high performance data storage array designed to store data streamed from the RZ2, our most powerful processor for high channel count data acquisition. Off-loading data streaming tasks from an RZ2 to the RS4 improves real-time performance and allows you to acquire continuous data over several days or weeks. Access to the RS4 storage array can be provided through a network connection, direct connection to a PC, or data transfer to a USB storage device.

The RS4 allows streaming of up to 1024 16-bit channels at rates up to ~25 kHz and fewer channels at rates up to ~50 kHz. Streamed data is stored as individual channels and can be stored in different numeric formats (Short, Float, etc.). Stored data can be easily reincorporated into the OpenEx data tank format for post processing. The RS4 is available with either 4 terabytes or 8 terabytes of storage and features 1 or 4 streaming ports.

Power and Communication

Data is transferred to the RS4 through its streaming ports located on the back panel of the device. A special version of the RZ2 provides matching ports used to connect and stream data to the RS4. These ports ensure fast and reliable data transfer from the RZ2 and are color coded for correct wiring. Communication to the RS4 is provided through a touch screen user interface independent from the TDT system. Firmware updates for the RS4 interface are available online through the TDT web server. See “Config Tab” on page 2-19 for more information.

The RS4 contains an integrated switched-mode power supply. The power supply auto-detects your region’s voltage setting and no further configuration is needed. A switch located on the back panel of the RS4 is used to enable/disable the power supply.

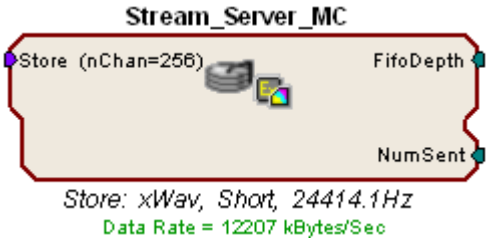
Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx) on the RZ2 processor through TDT run-time applications such as OpenEx or custom applications. A single RPvdsEx storage macro is provided to configure the RZ2 to send data to the RS4. Once connected to the RZ2, a properly configured RS4 will automatically store the data it receives.

See the "RZ2 BioAmp Processor" on page 1-3 for more information on the RZ2. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see "MultiProcessor Circuit Design" and "Multi-Channel Circuit Design" in the *RPvdsEx Manual*.

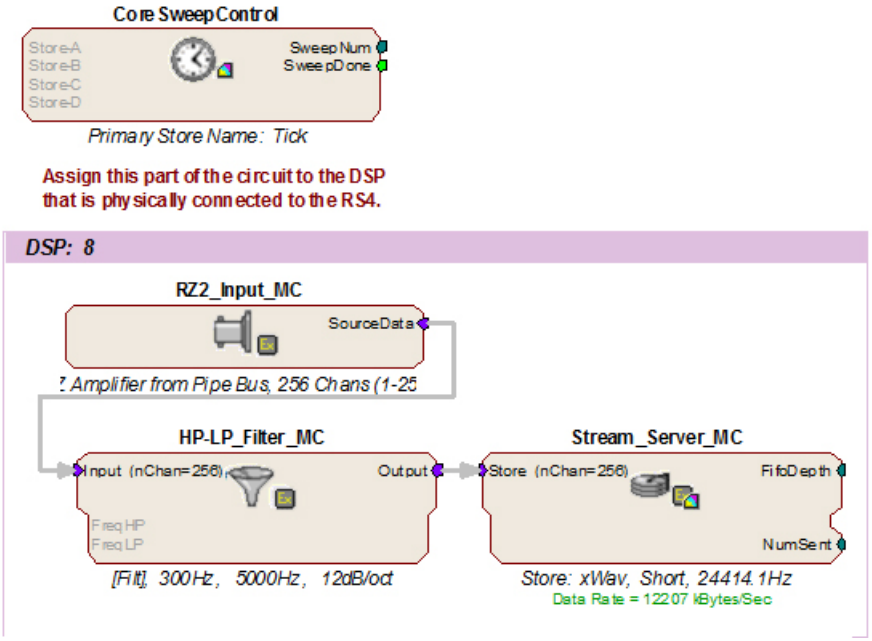
Distributing Data to the RS4

The Stream_Server_MC macro is provided for configuring data storage from the RZ2 to the RS4. The macro provides settings for the number of channels, storage format, and decimation factor. See the macro internal help for more information.



Note: The macro parameter summary, below the macro, lists important information such as the store name, data format, sample rate, and calculated data rate.

The following example illustrates a typical acquisition circuit designed for use with the RS4.



In this example, all circuit timing is handled by the CoreSweepControl macro. Acquisition and filtering are provided by the RZ2_Input_MC and HP-LP_Filter_MC macros. As data is input from a PZ amplifier, it is filtered and sent to the RS4 through the Stream_Server_MC macro.

It is important that the Stream_Server_MC macro is assigned to the DSP in the RZ that is physically connected to the RS4 (in this case, DSP-8) via fiber optic cables.

Recording Sessions

When an RZ2 begins streaming data to the RS4, a recording period or session is initiated. A session is defined as any length of continuous streaming data sent to an RS4 streaming port. Each streaming port on the RS4 can initiate a session and sessions may run concurrently. When data is no longer streaming to the port or if streaming has been paused for longer than 1 second, the session is concluded and a new session will begin when a new data stream is presented.

For long recording sessions, the RS4 touchscreen configuration settings include an option to "Segment files every" with several time options to periodically close and reopen the session and save data in multiple, smaller data files. See "Ports Tab" on page 2-14 for more information.

Important! When recording data in OpenEx's Preview mode, ensure that you place the hardware into Idle mode prior to switching to Record mode. Switching directly from Preview to Record mode will NOT terminate the data session. Failure to do this will cause any data recorded in Preview mode to be prepended to the data obtained in Record mode.

Data Transfer Rate

The maximum data rate for each RS4 streaming port is 12.5 MB/s. This equates to streaming 256 16-bit channels at a sampling rate of ~25 kHz per streaming port. With four ports available, up to 1024 channels can be streamed to the RS4.

Note: When recording data it is important to compare the data rate calculated by the macro to the actual data rate reported by the RS4. If the reported data rate in the RS4 is not similar to the calculated data rate in the macro, this may indicate a hardware problem. If so, contact TDT.

File System Check

Occasionally the RS4 will perform a file system check during the boot process. This is to ensure the integrity of the storage array and file system. You can view the progress of the file system check in the Status tab (see "Status Tab" on page 2-17, for more information) of the RS4 interface.

Note: The more files present on the storage array, the longer the file system check will take.

Hardware Requirements

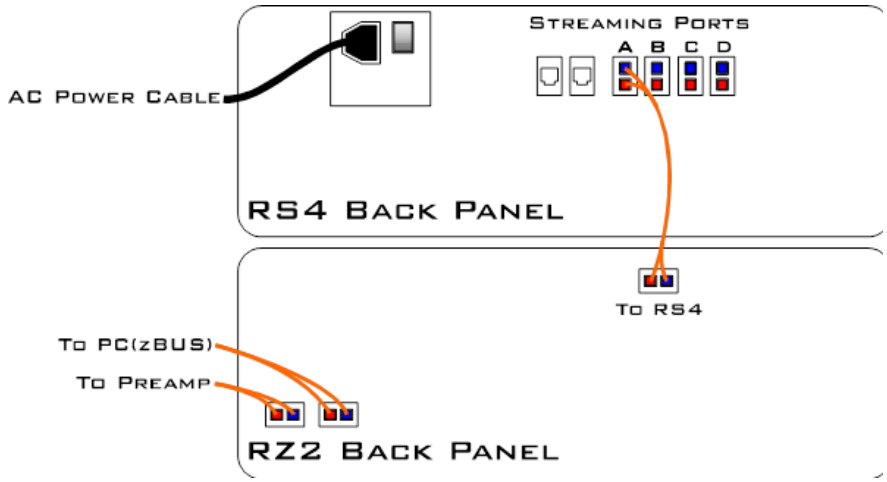
Basic requirements include an RS4, RZ2 equipped with at least one streaming port, and one fiber optic cable for connection between the RS4 and RZ2.

Optional requirements for accessing data on the RS4 include a PC equipped with an Ethernet port or an Ethernet jack connected to a local area network, and an Ethernet cable.

Setting-Up Your Hardware

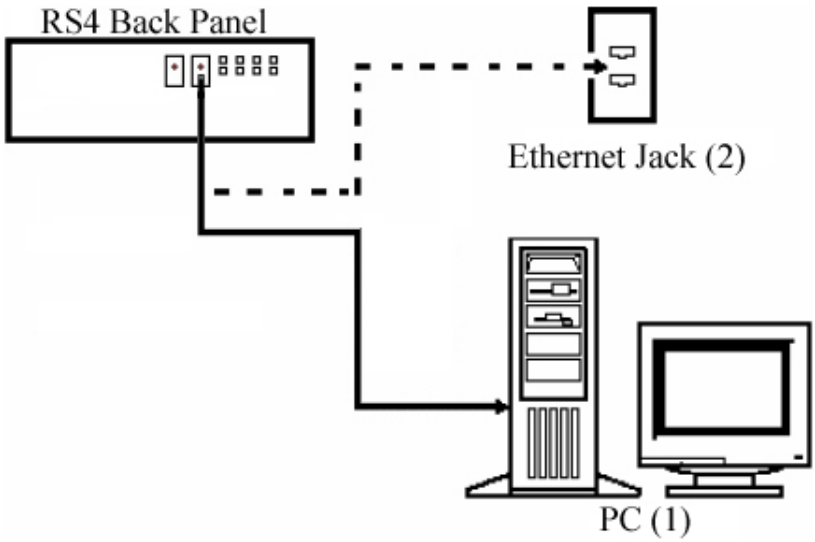
Basic setup for the RS4 Data Streamer includes connection to one or more RZ2 BioAmp Processors. Optionally, an Ethernet connection for direct connection to a PC or network is supported. Connect the RZ2 as illustrated in the following diagram.

Important! Make sure that all cables are connected before powering on the RS4.



RS4 to RZ2 Connection Diagram

In the diagram above, a single RZ2 provides one streaming input to the RS4. Additional RZ2 devices can be connected to the same RS4 provided it has vacant streaming ports (B, C, or D) available. The RZ2 is also connected to a preamplifier and PC (see "RZ2 BioAmp Processor" on page 1-3 for specific information). The fiber optic cables are color coded to prevent wiring errors.



RS4 PC and Network Connection Diagram

The diagram above illustrates possible connections from the RS4 to a PC (1) or network (2). Connect the Ethernet cable to the RS4 port labeled Network.

Configuring the RS4

Default configuration settings allow the RS4 to begin streaming data immediately. The RS4 supports the DHCP (Dynamic Host Configuration) protocol for automatic configuration of network parameters. Once connected to an active network, the RS4 will attempt to lease an IP address.

The DHCP Protocol

DHCP or "Dynamic Host Configuration Protocol" is a protocol used by networked devices (clients) to obtain various parameters necessary for the clients to operate in an IP (Internet Protocol) network. By using this protocol, system administration workload greatly decreases, and devices can be added to the network with minimal or no manual configuration.

DHCP automates the assignment of IP addresses, subnet masks, default gateway, and other IP parameters. Three modes for allocating IP addresses exist: Dynamic, Reserved, and Manual. The RS4 relies on Dynamic mode for its IP configuration. If no DHCP server responds, the device falls back on Manual mode and must be configured with the following default static IP configuration:

IP Address: **10.1.0.42**

Netmask: **255.255.255.0**

You can configure the IP address manually through the touchscreen interface. See "To enable manual configuration:" below or "Status Tab" on page 2-17.

Dynamic mode

In dynamic mode a client is provided with a temporary IP address for a given length of time. The duration is dependent on the server configuration and may range from several hours to months.

The RS4 will automatically renew the current IP address as needed. This renewal is used by properly functioning clients to maintain the same IP address throughout their connection to a network.

Accessing the RS4 Storage Array

There are two methods provided for accessing the RS4 storage array:

- Directly connecting to a PC
- Connection to a local area network

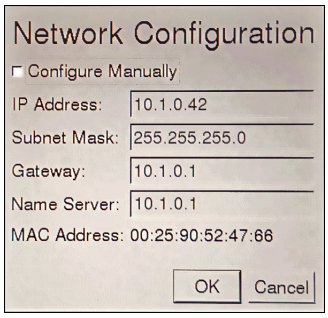
Direct Connection to a PC

Direct connection to a PC allows data on the RS4 to be viewed and modified through the standard Microsoft Windows file sharing protocol.

Important: When using a Static IP, the RS4 Current IP must be set to "Configure Manually" using the touch screen interface.

To enable manual configuration:

1. Touch the **Status Tab and then** touch the **Current IP field,** to display the Network Configuration window.



2. Touch the **Configure Manually** check box and click OK to accept the default value.

Using Windows 7

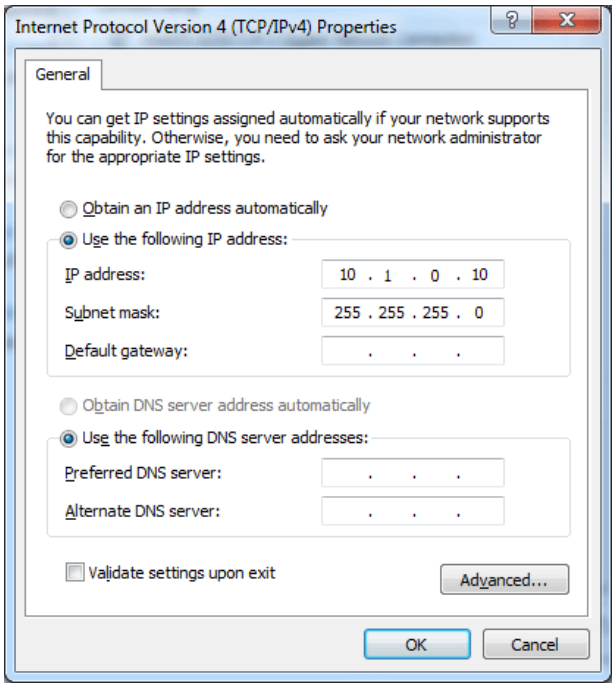
To access the RS4 file system through a PC, running Windows 7:

3. You will have to configure the PC TCP/IP settings. Open Control Panel then double-click **Network and Sharing Center**.
4. Click the desired connection link (this is usually a Local Area Connection).
5. In the status dialog, click the **Properties** button.
6. In the item list, select **Internet Protocol (TCP/IP)** or if there are multiples, select **Internet Protocol (TCP/IPv4)**.
7. Click the **Properties** button.
8. Select **Use the following IP address** and enter these values:

   IP address: 10.1.0.x; where x can be any value, 1 to 254 except 42

   Subnet mask: 255.255.255.0

   Default gateway: Leave empty

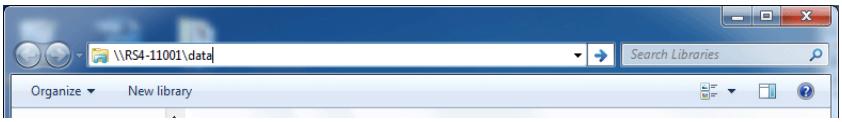


9. Click **OK**. The RS4 can now be accessed by the PC.
10. Obtain the RS4 device address.

a. Press the **Ports** tab on the RS4 interface.

b. The device address is displayed at the top of the page to the right of **Device Name** field.

11. Enter the device address as shown in a windows address bar to access the RS4 file system.



The path **RS4-#XXXX\data** is used to access the RS4 storage array. Where # is the total number of streaming ports on the RS4 back panel, XXXX is the device **serial number** while the data folder contains the **data** saved to the storage array.

12. Access the files on the RS4 by reading or writing.

WARNING!: Do not attempt to write to the RS4 storage array at any time while data is actively streaming. Doing so may corrupt data currently being stored.

Using Windows XP

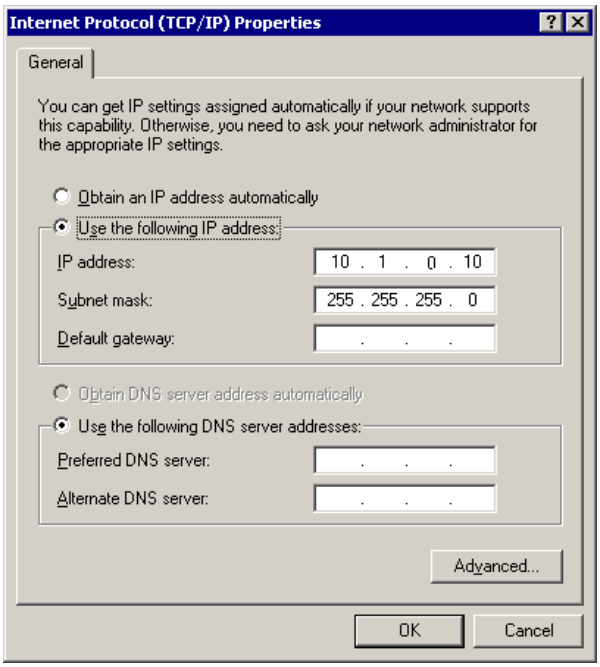
To access the RS4 file system through a PC:

1. You will have to configure the PC TCP/IP settings. Open **Control Panel** then double-click **Network Connections**.
2. Right-click the desired connection (this is usually a Local Area Connection) and select **Properties**.
3. Select Internet Protocol (TCP/IP) or if there are multiples, select Internet Protocol (TCP/IPv4).
4. Click the **Properties** button.
5. Select **Use the following IP address** and enter these values:

   IP address: 10.1.0.x, where x can be any value from 1 to 254 except 42.

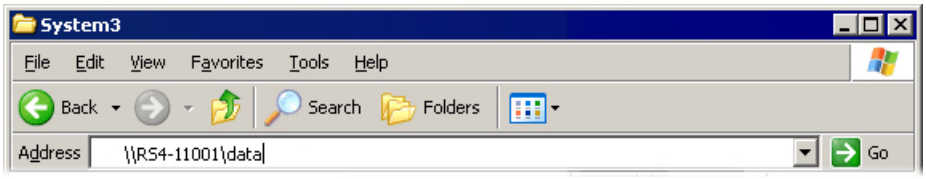
   Subnet mask: 255.255.255.0

   Default gateway: Leave empty



6. Click **OK**. The RS4 can now be accessed by the PC.
7. Obtain the RS4 device address. Press the **Ports** tab on the RS4 interface.

   The device address is displayed at the top of the page to the right of **Device Name** field.
8. Enter the device address as shown in a windows address bar to access the RS4 file system.



   The path **RS4-#XXXX\data** is used to access the RS4 storage array. Where # is the total number of streaming ports on the RS4 back panel, XXXX is the device serial number while the data folder contains the data saved to the storage array.
9. Access the files on the RS4 by reading or writing.

WARNING!: Do not attempt to write to the RS4 storage array at any time while data is actively streaming. Doing so may corrupt data currently being stored.

Connecting Through a Network

Connection to a local area network also allows data to be viewed and modified through the standard Microsoft Windows file sharing protocol from any PC connected to the same network as the RS4.

To access the RS4 file system through a network:

DHCP must be enabled on the network in order to access the RS4. If DHCP is disabled or not supported, you can connect the RS4 directly to a PC (see "Direct

Connection to a PC" on page 2-7 for more information).

1. Obtain the RS4 device address.
2. Press the **Ports** tab on the RS4 interface.

   The device address is displayed at the top of the page to the right of **Device Name** field.
3. Enter the device address in a windows address bar to access the RS4 file system.
4. Access the files on the RS4 by reading or writing.

    WARNING!: Do not attempt to write to the RS4 storage array at any time while data is actively streaming. Doing so may corrupt data currently being stored.

Finding the MAC Address

In some labs, the network administrator may require RS4 users to provide the device's MAC address.

To determine the address, follow the instructions below:

1. On the touchscreen interface, press the Status tab.
2. Press in the Current IP field.

   A Network Configuration dialog is opened and the MAC address is displayed at the bottom of the pop-up window.

Note: If the RS4 does not automatically identify on a network, you can force it to reset its IP address by unplugging the Ethernet cable the plugging it in again.

Moving Stored Data to a Data Tank

Data stored on the RS4 can be easily reincorporated into the OpenEx DataTank format for post processing.

RS4 Storage Format

The RS4 stores data in a format similar to the OpenEx DataTank format.

Data stored on the RS4:

- Contain an *.sev file for each channel recorded in the stream.
- Do not contain other Data Tank file types (.tbk, .tdx, .tev, .tsq).
- Stores all of the channel data files in a single Data Tank folder.

These features allow single and multi-channel data to be copied and pasted directly into any OpenEx Data Tank folder.

Naming Convention

When connected to an active network, TDT's OpenEx software sends information to the RS4 via a broadcast UDP packet allowing it to properly name the streaming data sent to the RS4.

For example, if you are recording channel 1 for the event wavA on Block-3 from DemoTank2 the RS4 will store in the following location and format:

\data\DemoTank2\Block-3\DemoTank-Block-3_wavA_ch1.sev

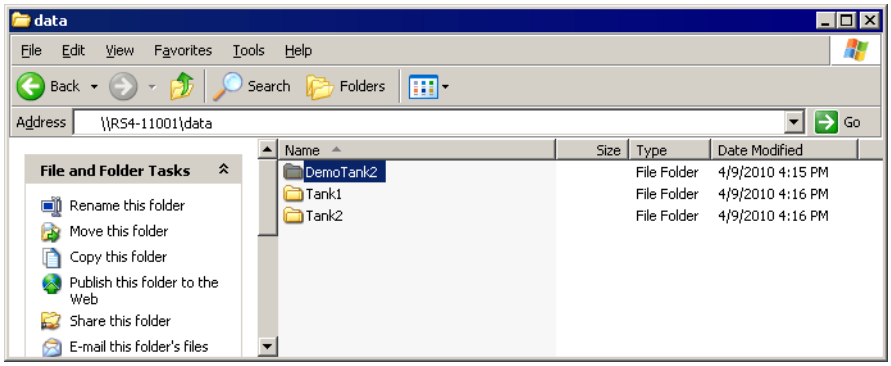
Without the OpenEx network information the RS4 falls back to the default data format:

\data\Event name-year-month-day-hour-minute-second\unnamed.sev

Note: The default format is also used if phantom storage is disabled in the Stream_Server_MC macro. See the macro internal help for more information.

To move blocks to a Data Tank:

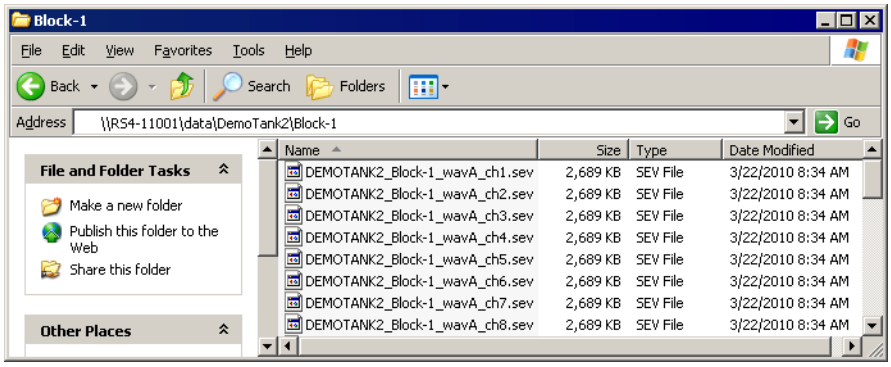
1. Access the RS4 file system on the local PC using the process described above.
2. Select the desired Data Tank.



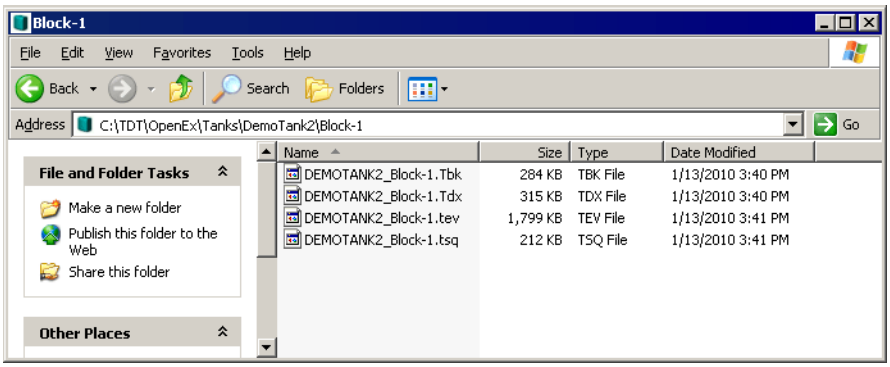
3. Copy the selected Data Tank to the local PC Data Tank.
4. If the Data Tanks share the same name, select **Yes to All** when asked to confirm possible overwrites. This will NOT overwrite data currently stored on the local drive since only the *.sev files are copied.
5. If you wish to move only a single block, copy the desired block and place it into the local PC Data Tank folder.

To move individual channels to a Data Tank:

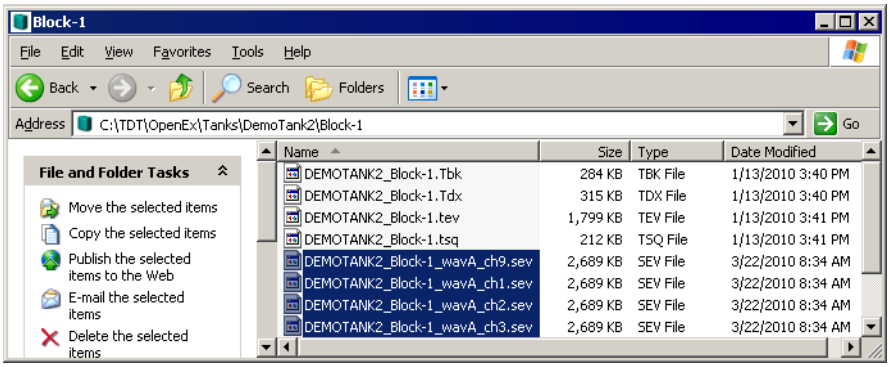
1. Access the RS4 file system on the local PC using the process described above.



2. Copy and paste the desired file(s) to the local PC Data Tank folder.
3. Open the Data Tank you wish to move the data to by browsing to the block folder in the Data Tank folder on the local PC.



4. Copy and paste the desired data from the RS4 to the local PC.



Note: Data sets containing a large number of channels, or long recording periods may take longer to display and process on the RS4 and will also lengthen the amount of time for file system checks. TDT recommends removing data that is no longer needed on the RS4 ("Storage Tab" on page 2-15 for more information on deleting data).

After moving, the data can be processed using one of TDT's Data Tank applications (such as OpenExplorer). To access the data using these applications simply select the associated block then select the event name (in this case Block-1 and wavA).

RS4 Features

Power Button

A power button located on the front plate of the RS4 is used to turn the device on and off. Prior to powering on/off, the device will enter a brief boot/shutdown period.

Important! Always power the RS4 down during an Idle state. Idle status can be checked in the Ports tab. Failure to power down during Idle status may result in the RS4 performing a file system check during the next boot process and possible data loss.

To turn off the RS4:

1. Ensure that the RS4 is in the Idle state prior to shutdown. To do this, press the Ports tab and verify that the current session name is Idle on all data ports.
2. Press the power button on the front panel.

Note: If the RS4 becomes unresponsive and fails to shutdown normally, you can shut the device down by holding the power button for longer than five seconds. This will force the device to shutdown. After a forced shutdown, the RS4 may perform a file system check.

LCD Touch Screen

The LCD touch screen allows navigation through the RS4 interface. To make a selection, gently press the touch screen on the desired item. Standard click and drag options for the storage array are also supported in order to select multiple file system objects. To click and drag, gently press your finger on the start location then slide down the screen until the desired items are selected.

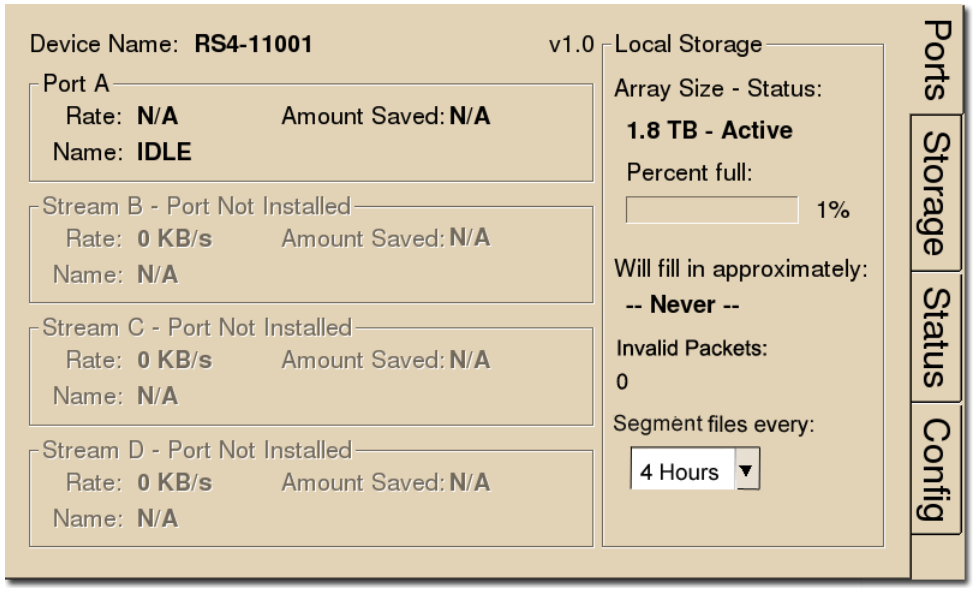
Interface

The interface reports information and allows configuration of available options. A selection tab located on the right-side of the screen allows the user to select between the available pages. To navigate to the desired window, press the corresponding tab on the right side of the LCD screen.

Ports Tab

The Ports tab provides information for storage array streams, local storage rates, and storage size.

Note: Keep in mind that the total available storage is based on the amount of free memory space after system allocation. For example, although the system specifications list 8 terabytes of storage space, 7.2 terabytes are actually available for data storage.



Firmware Version: The currently installed firmware version number is displayed to the left of the local storage label on the Ports tab. This is useful for identifying the current firmware version and also to verify that a recent firmware update has been installed.

Device Name: Displays the assigned device name.

Port A, B, C, D: Displays port information regarding the currently installed storage array.

Rate: Displays the approximate current data transfer rate in kB/s. This rate incorporates overheads in the data transfer protocol and may differ slightly from the data rate calculated by the macro.

Amount Saved: Displays the amount of data saved to the storage array during the current recording session.

Name: Displays the current session name. See "Naming Convention" on page 2-11 for more information.

Local Storage: This area displays information relative to the currently installed array.

Array Size - Status: Displays the status of the storage array.

nTB - Active: Array is properly configured and its maximum storage space (nTB) is listed.

Not Ready: No array is detected or the array is not yet ready

Percent Full: Displays the percentage of space that has been used on the storage array.

Will fill in approximately: Displays an estimate of how much time it will take to fill the storage array with data based on the data rates for the current session(s).

Segment files every: For long recordings, set a value to indicate when the RS4 should close the recording session and open a new session. This allows the user to access the raw data for parallel processing before the recording is over.

The exact length of each file will be a multiple of a fixed block size, based on the sampling rate. It will be as close as possible to the selected setting value (i.e. 1hr, 4hr, etc.), but will not be exact (within 0.1 seconds or so of the exact desired duration). There will however be no overlap in the data at the beginnings and ends of the files.

The files will be named as follows:

{TANK}_{BLOCK}_{STORE}_ch1.sev

{TANK}_{BLOCK}_{STORE}_ch1-1h.sev

{TANK}_{BLOCK}_{STORE}_ch1-2h.sev

...

{TANK}_{BLOCK}_{STORE}_ch2.sev

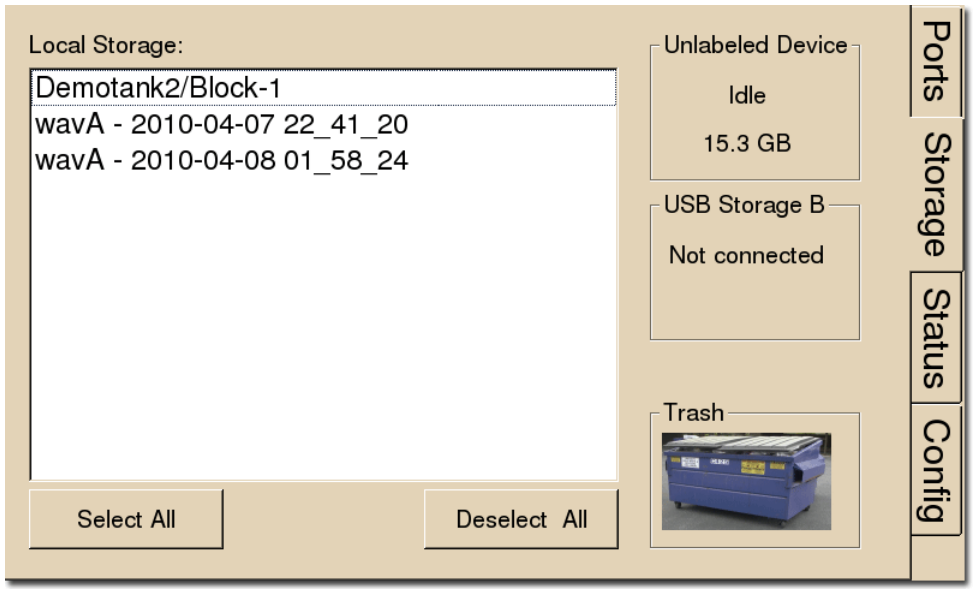
{TANK}_{BLOCK}_{STORE}_ch2-1h.sev

{TANK}_{BLOCK}_{STORE}_ch2-2h.sev

Note: If using Phantom Headers to merge the RS4 data with your other tank data, and using TTank to read it, only the first chunk will be accessible because it matches the expected naming scheme.

Storage Tab

The Storage tab provides a list of file system objects stored on the currently installed storage array. Items may be selected and deleted or moved and copied to a USB device. Status information for any connected USB Storage devices is displayed.



Local Storage: Data items stored on the RS4 storage array are populated in the local storage list. Multiple items may be selected using press and drag techniques.

Select All: Press to select all items in the list.

Deselect All: Press to deselect all items in the list.

USB Storage A, B: Displays connection information for USB devices detected on USB ports A and B. Select item(s) from the local storage list and press the desired USB Storage connection indicator to prompt the copy dialog. From this dialog you may:

Copy: Press to copy the selected item(s) to the desired USB Storage device. Copied items remain on the storage array.

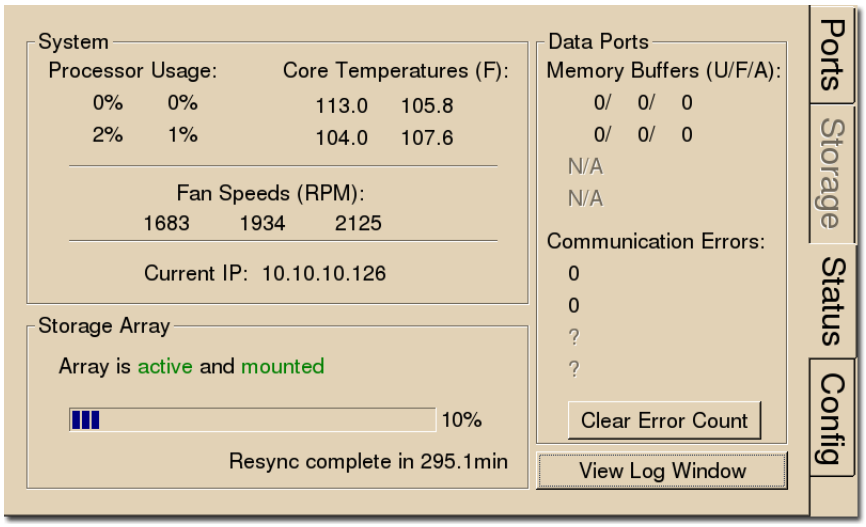
Move: Press to move the selected item(s) to the desired USB storage device. Moved items are copied onto the USB storage device and deleted from the storage array.

Cancel: Press to cancel the current USB data transfer.

Note: When moving or copying items the RS4 interface may become temporarily unresponsive.

Trash: Select item(s) from the local storage list and press the Trash icon to permanently delete them. A dialog will prompt asking to confirm the deletion of the item(s).

Status Tab



The Status tab provides system information such as processor usage rates, core temperatures, fan speeds, device IP address, array reformat progress, memory buffer allocation, and communication errors. Log information can also be retrieved from this tab.

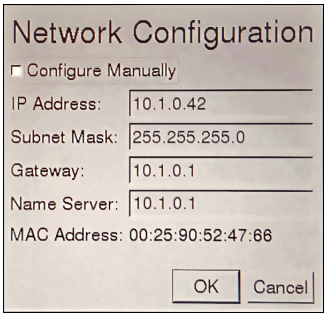
System: Displays important system status information.

Processor Usage: Displays the current percent usage for each processor core.

Core Temperatures (F): Displays the current processor core temperatures measured in Fahrenheit.

Fan Speeds (RPM): Displays the approximate rpm for all three fans located inside of the RS4.

Current IP: Displays the currently assigned IP address for the RS4. Press to display Network Configuration Window.



Configure Manually - select to enable manual configuration and make fields editable.

Storage Array: Displays information about the state of the current storage array.

Active and mounted: Storage array is available and ready to store data.

Active and not mounted: A support storage array is available but is not configured to store data.

Array was not found!: The system did not detect a supported storage array.

Progress bar: Displays progress for various processes which run on the RS4 including:

Reformatting: When reformatting a storage array, the progress completed (%) as well as the estimated amount of time remaining is displayed.

Resyncing: If a mirrored array type has been formatted, the progress completed (%) as well as the estimated amount of time remaining for the Resync process is displayed. See "Mirrored" on page 2-20, for more information.

File System Check: If the RS4 is performing a file system check, the progress completed (%) and estimated amount of time remaining is displayed. During this time the status array will not be ready.

Check button: When the storage array is in mirrored configuration, disk check button appears at the bottom left corner. Pressing the **Check** button begins a disk check to see if the data on both images are identical. This process can take several hours. A progress bar and an estimated time to completion are displayed.

During this time the Ports tab will report that the array status is "Checking". No data access should occur during checking.

The button will stay depressed for the duration of the disk check.

You can stop the disk check at any time by pressing the **Check** button again.

TDT recommends performing a disk check on a mirrored configuration every 7-30 days.

Data Ports: Displays storage information for all installed memory buffers and any communication errors present.

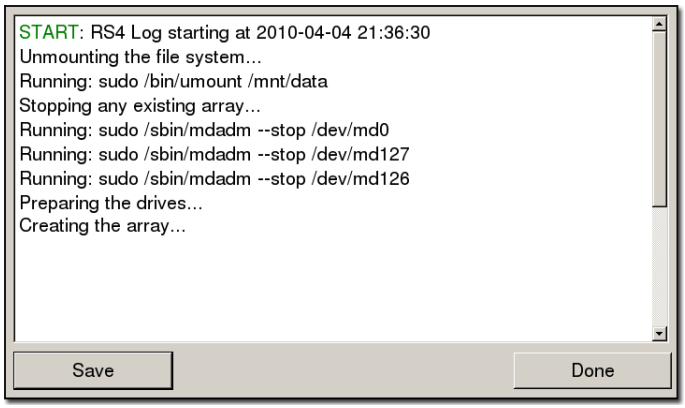
Memory Buffers (U/F/A): Displays the number of memory buffers currently used, free, and allocated.

Communication Errors: Displays the current count of communication errors between the RS4 and interfaced RZ2s. This value should be zero. If not, the current data session may not contain valid data.

If the count increases continuously at a high rate (>1500 errors per second), the RZ connected to that port might not be synchronized to the PCI card. Check the fiber optic connection from the RZ device to the PCI card and use zBusMon to confirm RZ to PC communication.

Clear Error Count: Press to clear all communication errors currently listed.

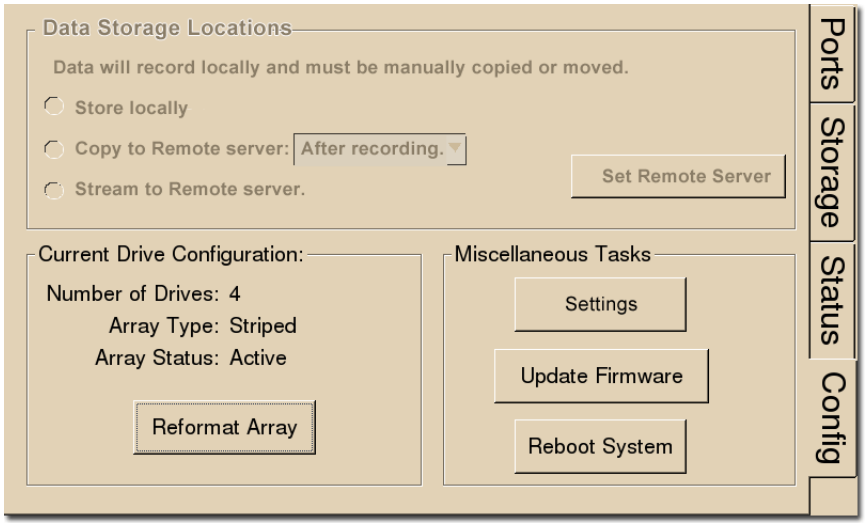
View Log Window: A log stores relevant messages and any communication errors encountered while the RS4 is in use. Click to open and view the log window. The log.txt file can be copied from the storage array for transfer to a PC.



Note: Individual comments can be saved as well. Use standard drag techniques to highlight the desired comment(s) and click **Save** to write the selection to the log.txt file.

Config Tab

The Config tab provides options for reformatting the currently installed storage array, updating the RS4 firmware, and rebooting the system.



Data Storage Locations: Not currently implemented.

Current Drive Configuration: Displays information about the currently installed data drives.

Number of Drives: Displays the number of drives currently installed and optionally their corresponding array usage.

Array Type: Displays the currently configured array type and the status of the drives.

Striped: Array type is currently configured as striped.

Mirrored(UUUU): Array type is currently configured as mirrored. A U indicates that a drive is up and running. A _ indicates a drive failure.

Missing: No array type is detected. See "Config Tab" on page 2-19, for more information.

Array Status: Displays the current status of the array.

Preparing: Storage array is currently being reformatted.

Resyncing: Storage array is being reformatted as a mirrored array and is currently resyncing the mirrored partitions. See Mirrored below for more information.

N/A: Storage array is not detected.

Active: Storage array is detected and configured.

Reformat Array: Press to prompt the reformat array dialog. This dialog will ask for confirmation as well as the desired array type: Striped or Mirrored. Reformatting an array will erase all data contained in the array. Note: When reformatting an array, the interface may become temporarily unresponsive.

Miscellaneous Tasks: Provides options for updating the current RS4 firmware and rebooting the system.

Settings: Press to display the settings window, then set date and time and select unit of measure for temperature.

Update Firmware: Press to update the RS4 firmware. Firmware is downloaded from the TDT server and automatically installed on the RS4. Connection to a network that has Internet connectivity is required to retrieve any updates.

Reboot System: Press to reboot the system.

Storage Array Types

Two RAID based array types are supported on the RS4, Striped and Mirrored. When reformatting the storage array, either type may be selected for the new format. Each type has advantages and disadvantages and is suited for particular situations.

Striped

Striped array types offer quick reformatting (several minutes), efficient data storage, and performs streaming tasks at the maximum transfer rate. This type does NOT protect against data drive failures and loss of a data drive will result in loss of data. Since the data is not backed-up as is the case in mirrored arrays, striped storage arrays offer twice the amount of storage space that mirrored arrays provide. This format is useful for those who wish to stream large amounts of data and are using an external solution to provide data recovery in the event of drive failure.

Mirrored

Mirrored array types offer data loss prevention at the cost of some transfer rate limitations and reduced storage space. Unlike striped array types, data drives are mirrored and data is backed-up. This results in longer write times and also a much longer reformatting period (hours). This format is useful for those who are streaming smaller amounts of data and are concerned with data loss prevention.

Mirrored arrays will prevent data loss if any single drive fails. RS4 devices that contain four data drives, in some cases, are protected if two of the four data drives fail. The storage capacity, however, is cut in half.

A resyncing status is displayed while reformatting a mirrored array. This status is unique to the mirrored array type and is verification for the mirrored partitions of the array. One partition is read while another partition is simultaneously written to. This ensures that mirrored partitions are in sync to provide data loss prevention. Prior to completion of the resyncing process, data loss prevention is disabled.

Note: If the resyncing process is interrupted by a loss of power or shutdown of the system, it will resume to where it left off prior to the interruption.

To reformat the RS4 storage array:

1. Press the **Config** tab on the RS4 interface.
2. Press the **Reformat Array** button.
3. Press the desired array type or press Cancel to exit.

USB Ports

Two USB 2.0 ports are provided for small/slower data transfers (typically less than several GB of data) or for access to the storage array when no network or PC is available. The ports support connections at any time while the device is powered.

When supported USB media is detected, the interface will display only the total space existing on the media as a reference. It does NOT display available space on the media.

Note: TDT recommends that you do not attempt to copy or move files using the USB ports while a recording session is active.

Device Status LEDs

The device status LEDs report streaming or network activity. The following tables display the status LED indicators.

Video

Not currently implemented.

Network

Status	Information
Off	No network traffic detected.
Lit	Network traffic is present and detected on the RS4.

Storage

Status	Information
Off	No storage access to the RS4 is detected.
Lit	Storage access to the RS4 is in progress

Ethernet Ports

Two Ethernet ports are provided on the back panel, Video and Network.

Video Port

Not currently implemented.

Network Port

The Network port allows connections to either a PC or local area network via a standard Ethernet cable. The RS4 supports automatic DHCP protocol, see “The DHCP Protocol” on page 2-7 for more information.

Troubleshooting

The following section provides examples and solutions to some of the errors that could be encountered while using the RS4 Data Streamer.

Device Will Not Power Up

Check the position of the power supply switch. If set to the “O” position the power supply is disabled. To enable, simply ensure that the switch is in the “1” position and attempt to power on the RS4. If the device does not power up after verifying that the power supply is enabled contact TDT.

Can’t Access the RS4 Storage Array

Check the Ethernet cable connection to ensure that the RS4 is connected to a network or PC using the Network Ethernet port located on the back panel of the RS4. If the Ethernet cable is connected to the Video Ethernet port, network traffic will cause the Video status LED to light up. See “Setting-Up Your Hardware” on page 2-6 for connection diagrams.

If you are attempting to access the RS4 through a network, ensure that the server supports DHCP. If not, the RS4 will default to its static IP address (10.1.0.42). If you encounter this issue, see “Direct Connection to a PC” on page 2-7 for information on how to access the RS4 using a direct connection to a PC.

RS4 Interface Becomes Slow or Unresponsive

Researchers who use the OpenEx preview mode extensively may find the interface to behave sluggishly. The RS4 does not throw out data recorded while in preview mode. Data recorded in preview mode is stored as unnamed data on the RS4 and is readily distinguishable from legitimate data recorded during an actual experiment. TDT recommends removing unnecessary data remaining on the storage array.

RS4 Is Not Correctly Naming Data

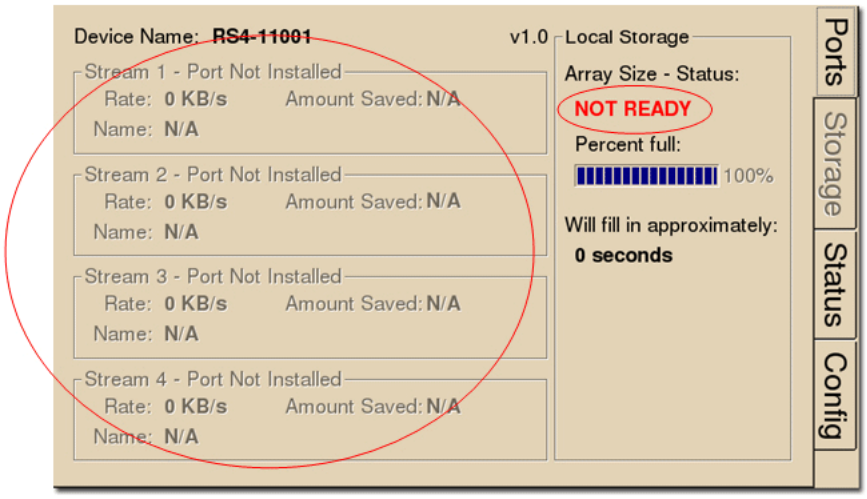
When connected to an active network, TDT's OpenEx software sends information to the RS4 via a broadcast UDP packet allowing it to properly name the streaming data sent to the RS4. If the RS4 is powered on before connecting the necessary network cables it may default to the basic naming format:

\data\Event name-year-month-day-hour-minute-second\unnamed.sev

Power off the RS4, connect all the necessary cables then power the RS4 back on.

Port Tab Errors

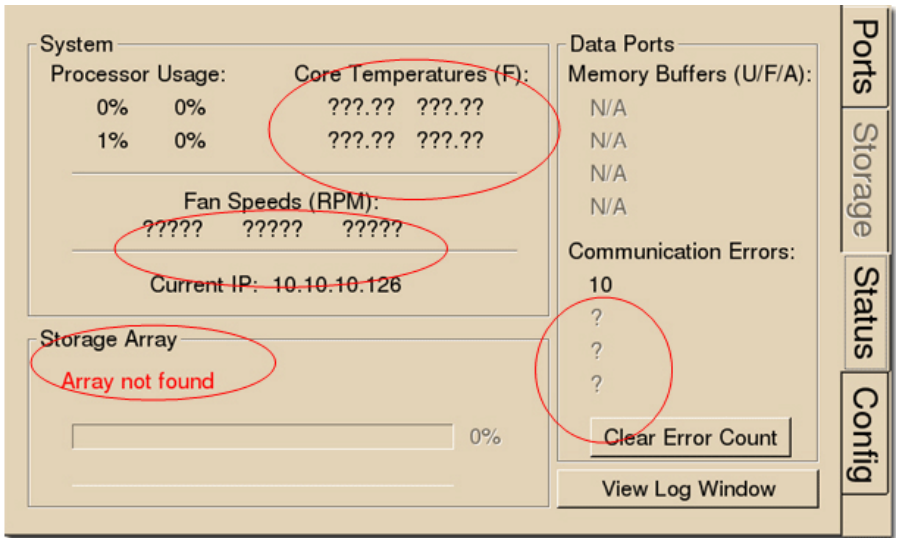
Below is an example of errors that can be encountered on the Port tab.



Ports that are not currently installed will be displayed in grayed out text. In most cases it is normal to see 3 of the 4 Streams disabled (since RS4 devices come installed with 1 or 4 data ports). Hardware failures can cause all ports to be grayed out. If you encounter this issue, contact TDT.

Array status messages will determine whether or not a storage array is currently installed properly. If the NOT READY status is displayed, the storage array may require reformatting (Check the Status tab for more details). See "Storage Array Types" on page 2-20 for information on reformatting.

Status Tab Errors



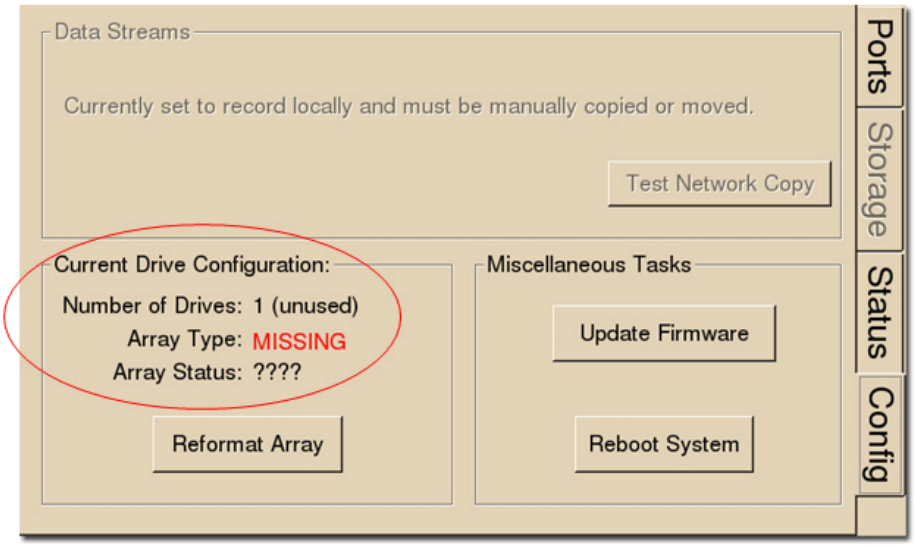
Temperature sensor failures will be displayed as ???.?? in the Status tab. If you encounter this issue, contact TDT.

Typical fan speed rates should be 1500 RPM and 3500 RPM under heavy processing loads. Fan failures will be displayed as ????? in the Status tab. If you encounter this issue, contact TDT.

Unformatted storage arrays will cause an Array not found status to be displayed. This may also be caused by disk drive failures within the RS4. You may attempt to reformat the storage array. See “Storage Array Types” on page 2-20 for information on reformatting. If reformatting is not desired, contact TDT.

Communication errors are compiled per recording session for currently installed streaming ports and will indicate if a streaming port had a communication failure at some point during the session. Data recorded during the session may be invalid. Communication errors may result from wiring errors between the RZ2 and RS4. Cycling power on the RZ2(s) may fix the issue. Refer to the “RS4 to RZ2 Connection Diagram” on page 2-6 for a proper wiring example. If the wiring is correct this may indicate a bad fiber optic cable that will need to be replaced.

Config Tab Errors



Drive configuration errors may occur if the RS4 is unable to detect a properly formatted storage array. You may attempt to reformat the storage array. See “Storage Array Types” on page 20 for information on reformatting. If reformatting is not desired, contact TDT.

Note: If using a mirrored array type, drive failures will be displayed using an underscore.

For Example, if drives 1 and 2 fail the Array Type will read:

Array Type: **Mirrored (_ _UU)**

Data in these scenarios are most likely recoverable. If you encounter this issue contact TDT. You may attempt to recover the data by accessing the RS4 file system to move the data to a local PC prior to reformatting the array.

RS4 Technical Specifications

Processing Cores	4
Storage Array Size	4 Terabytes or 8 Terabytes
Streaming Ports	
Number of Ports	1 or 4
Port Speed	12.5 MB/sec (per port)

PO8e Streaming Interface for the RZ

PO8e Overview

The RZ PO8e interface is an optional interface for RZ processor devices and is designed to transfer high channel-count data to a PCI Express card interface (PO8e) for real-time processing in custom applications. The PO8e card can be in the same computer as the TDT system, or in a dedicated computer.

The RZ connects to the PO8e card via a special DSP (RZDSP-U). This DSP has an interface located on the back panel of the RZ processor and connects to the PO8e via orange fiber optic cables provided with the system.

Data streamed through the PO8e is buffered at several points while the system copies it from the RZ to PC memory. When data is generated on the RZ unit and fed into the PO8e HAL object in Synapse Processing Tree (or the Stream_Remote_MC macro in RPvdsEx), this data is placed in a 10000 sample (per channel) FIFO buffer on the RZ processor. Data from this FIFO is transferred over the fiber optic link to the PO8e PCI Express card.

A shared library is provided (PO8eStreaming) along with a C/C++ interface for writing custom applications to collect data from the PO8e card in real-time. In the PO8eStreaming library a dedicated software thread actively attempts to read from the PCI Express card and places the transferred data into a RAM buffer. This structure allows the application program to query the API when convenient and read data in larger blocks. The RAM buffer is limited only by available memory, though the programmer should consume the data as soon as possible since this interface can transfer at rates up to ~12.5 MB/second.

PO8e Installation

Synapse has a built-in object for the Processing Tree to stream data to the PO8e. This must be added to your Hardware Rig in Synapse and then simply connect the desired output stream to the PO8e object. See the Synapse manual for more information.

For RPvdsEx circuit design, the TDT drivers installs the PO8e circuit macro here:

C:\TDT\RPvdsEx\Macros\Device\PO8e_Streamer\

The PO8eStreaming libraries and examples can be found in:

C:\TDT\RPvdsEx\Examples\PO8e\

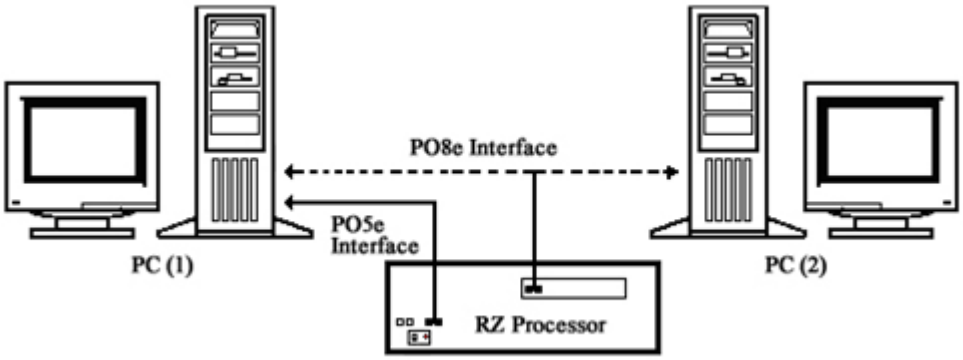
PO8e Hardware Requirements

Basic requirements include a paired fiber optic cable, an RZ processor equipped with the RZDSP-U card.

The PO8e requires a Windows or Linux computer with a PCI Express slot.

Setting-Up Your Hardware with the PO8e

In order to setup the RZ PO8e interface, connect the fiber optic cable from the RZ back panel to the PO8e card installed in the computer. The PO8e can be installed in the same computer as the PO5/e card or in a separate computer. For more information on setting up or configuring the RZ processor see the *System 3 Installation Guide.*



PO8e Connection Diagram

The diagram above illustrates the possible PO8e connections from the RZ processor to the TDT PC (1) or to a separate PC (2).

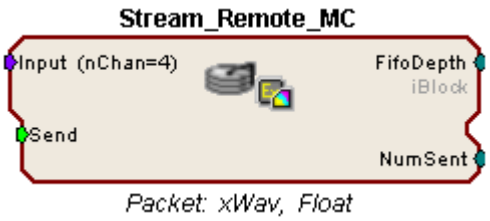
PO8e Circuit Design

If using Synapse, use the PO8e HAL to stream data to the PO8e and skip this section. If using RPvdsEx in OpenEx, stream to the PO8e interface using the RPvdsEx macros named Stream_Remote_MC. This macro operates on multi-channel data and can be configured to specify the number of channels and data type.

Stream_Remote_MC Macro

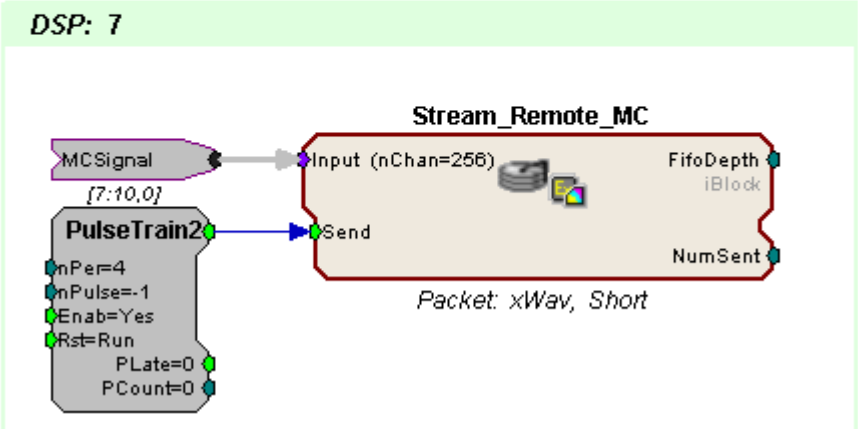
The Stream_Remote_MC macro is used to send data from the RZ to the PO8e card. All data is organized into packets according to the number of words (specified by the packet size) set in the macro setup properties dialog.

The macro accepts a multi-channel data stream as well as a logic input that tells the macro to send out a packet.



Sending Data Construct

Data is sent whenever the "Send" input receives a rising trigger (logic high (1)). Up to 256 channels can be sent on each Send signal. This occurs in one sample period. If the number of channels is greater than 256, data is sent in blocks and grouped together on the PO8e card's buffer.



In this circuit, 256 channels of data in Short format are sent to the PO8e card every fourth sample. The CoreSweepControl macro is required in any circuit using the Stream_Remote_MC macro. The Stream_Remote_MC macro must be placed on the special DSP that is physically connected to the PO8e card (DSP #7 in this case).

Note: To modify the number of channels sent and the data format, edit the parameters found in the Stream_Remote_MC macro setup properties.

About PO8e Streaming

PO8eStreaming is a library of methods for accessing data on one or several PO8e interfaces through a custom Windows or Linux application.

Both C and C++ interfaces are provided to this library. The C interface creates a pointer to a connected card, and then that pointer is passed to each subsequent function. TDT also has Python and Matlab libraries available.

Users should be mindful of using good 'closed loop' access when working with PO8eStreaming. This means always releasing any open connections to PO8e cards.

A typical PO8e access session for a client consists of five main steps:

1. Run the circuit on the RZ device that streams to the PO8e card.
2. Call connectToCard to get a pointer to an available PO8e card.
3. Call startCollecting to begin reading from PO8e card.
4. Perform any number of buffer operations.
5. Call releaseCard to release the card object from memory.

Organization of PO8e Streaming Methods

PO8eStreaming methods can be divided into three basic groups:

- Setup and Control -- The methods in this group are used to setup access to any PO8e card(s) in the system.
- Hardware Data Access -- The methods in this group are used to read data from PO8e card(s).
- Hardware Information Retrieval -- The methods in this group are used to access information pertaining to current data stream, including number of channels and sample size in bytes.

Setup and Control *PO8e*

cardCount

Description: cardCount returns the number of PO8e cards detected in the system. Call this first to determine the possible values for the "index" passed to the constructor.

C++ prototype:
```
static int cardCount();
```

C prototype:
```
int cardCount();
```

Returns: The number of PO8e cards in the system.

Sample Code

C++
```
int totalCards = PO8e::cardCount();
```

C
```
int totalCards = cardCount();
```

connectToCard

Description: Returns a pointer to the specified card index. Note that the index will be consistent across system boots and is dependent on the PCIe bus layout, so if you move the cards between slots their respective indices can change.

C++ prototype:
```
static PO8e* connectToCard(unsigned int cardIndex = 0);
```

C prototype:
```
void* connectToCard(unsigned int cardIndex = 0);
```

Arguments: *cardIndex* Specify the target card by index.

Returns: Pointer to PO8e instance.

Sample Code This code sample creates a PO8e object pointing to the first card identified in the system.

C++
```
PO8e *card = PO8e::connectToCard(0);
```

C
```
void *card = connectToCard(0);
```

releaseCard

Description: Free the PO8e card objects through this interface. It is done this way to ensure that in Windows the objects are freed from the correct heap context.

C++ prototype:
```
static void releaseCard(PO8e *card);
```

C prototype:
```
void releaseCard(void* card);
```

Arguments:

card Pointer to PO8e object.

Sample Code This code sample releases the card object memory.

C++
```
PO8e::releaseCard(card)
```

C
```
releaseCard(card)
```


startCollecting

Description: Call this to start collecting a data stream from the PO8e card. Collected data will be buffered as needed.

C++ prototype:
```
bool startCollecting(bool detectStops = true);
```

C prototype:
```
bool startCollecting(void* card, bool detectStops = true);
```

Arguments:

detectStops Tell the PO8e to detect when the stream from the RZ is stopped.

Returns:

pointer Pointer to PO8e instance.

Sample Code

Description: This code sample tells an existing PO8e object to begin collecting data.

C++
```
card->startCollecting(true);
```

C
```
startCollecting(card, true);
```

stopCollecting

Description: Call this to stop collecting a data stream from the PO8e card.

C++ prototype:
```
void stopCollecting();
```

C prototype:
```
void stopCollecting(void* card);
```

Sample Code

Description: This code sample stops data collection on a PO8e object.

C++
```
card->stopCollecting();
```

C
```
stopCollecting(card);
```

waitForDataReady

Description: This function provides a means to efficiently wait for data to arrive from the RZ unit.

C++ prototype:
```
size_t waitForDataReady(int timeout = 0xFFFFFFFF);
```

C prototype:
```
int waitForDataReady(void* card, int timeout = 0xFFFFFFFF);
```

Arguments:

int	*timeout*	Maximum duration (in ms) to wait for streaming to begin.

Sample Code

Description: This code sample blocks execution until buffered data is ready on the card.

C++
```
card->waitForDataReady();
```

C
```
waitForDataReady(card);
```

samplesReady

Description: Returns the number of samples (per channel) that are currently buffered.

C++ prototype:
```
size_t samplesReady(bool *stopped = 0);
```

C prototype:
```
int samplesReady(void* card, bool *stopped = 0);
```

Arguments:

bool pointer	*stopped*	The value pointed to will be set to true if the underlying mechanisms detect that data has stopped flowing.

Sample Code

Description: This code returns the number of samples (per channel) currently buffered on the card and detects if streaming has stopped.

C++
```
bool stopped;
```

```
size_t numSamples = card-
>samplesReady(&stopped);

if (stopped)

    PO8e::releaseCard(card);
```

C

```
bool stopped;

int numSamples = samplesReady(card,
&stopped);

if (stopped)

    releaseCard(card);
```

readChannel

Description: Copy the data buffered for an individual channel. Note that this call does NOT advance the data pointer. Use calls to flushBufferedData to discard the data copied using this function. The user is responsible for ensuring that the buffer is large enough to hold nSamples * dataSampleSize( ) bytes. The optional offsets array should be nSamples long and will be populated with the data offset of each block. This allows a user to detect if the buffer on the RZ unit has overflowed.

C++ prototype:

```
int readChannel(int chanIndex, void *buffer,
int nSamples, int64_t *offsets = NULL);
```

C prototype:

```
int readChannel(void* card, int chanIndex,
void *buffer, int nSamples, int64_t
*offsets);
```

Arguments:

int *chanIndex* The channel to read data from.

void pointer *buffer* The location to write buffered data to.

int *nSamples* The number of samples to read.

in64_t pointer *offsets* The location to write the buffer indices to.

Returns:

int Number of samples that were read.

Sample Code

Description: This code sample reads 1 sample from channel 2 and stores it in buff.

C++

```
short buff[8192];

card->readChannel(2, buff, 1);
```

C

```
short buff[8192];

readChannel(card, 2, buff, 1);
```

readBlock

Description: Copy the data buffered for all channels. Note that this call does NOT advance the data pointer. Use calls to flushBufferedData to discard the data copied using this function.

The data will be grouped by channel and the number of samples returned applies to all channels. The user is responsible for ensuring that the buffer is large enough to hold nSamples * numChannels( ) * dataSampleSize( ) bytes. The optional offsets array should be nSamples long and will be populated with the data offset of each block. This allows a user to detect if the buffer on the RZ unit has overflowed.

C++ prototype:
```
int readBlock(void *buffer, int nSamples, int64_t *offsets = NULL);
```

C prototype:
```
int readBlock(void* card, void *buffer, int nSamples, int64_t *offsets);
```

Arguments:

void pointer	*buffer*	The location to write buffered data to.
int	*nSamples*	The number of samples to read.
in64_t pointer	*offsets*	The location to write the buffer indices to.

Returns:

int — Number of samples that were read.

Sample Code

Description: This code sample reads 1 sample from all channels, stores it in a buffer and flushes that data from the card.

C++
```
short buff[1024];
card->readBlock(buff, 1);
card->flushBufferedData(1);
```

C
```
short buff[1024];
readBlock(card, buff, 1);
flushBufferedData(card, 1);
```

flushBufferedData

Description: Releases samples from each buffered channel.

C++ prototype:
```
void flushBufferedData(int numSamples = -1, bool freeBuffers = false);
```

C prototype:
```
void flushBufferedData(void* card, int numSamples = -1, bool freeBuffers = false);
```

Arguments:

int	*numSamples*	Number of samples to release. Passing -1 releases all buffered samples.
bool	*freeBuffers*	Controls the optional freeing of the underlying data buffers.

Sample Code

Description: This code sample flushes one sample from all channels.

C++
```
card->flushBufferedData(1);
```

C
```
flushBufferedData(card, 1);
```

Hardware Information Retrieval

numChannels

Description: Counts the number of channels in the current stream. This value is set in the Stream_Remote_MC macro. Changing the number of channels mid-stream triggers an error condition.

C++ prototype:
```
int numChannels();
```

C prototype:
```
int numChannels(void* card);
```

Returns:

int — Number of channels in the current data stream.

Sample Code

Description: This code determines how many channels are in the current stream.

C++
```
int nChannels = card->numChannels();
```

C
```
int nChannels = numChannels(card);
```

numBlocks

Description: Counts the number of blocks that the current stream is divided into. This value is set in the Stream_Remote_MC macro. Each block will contain the same number of channels, so dividing the value from numChannels( ) by this value will leave no remainder. Changing the number of blocks mid-stream triggers an error condition.

C++ prototype:
```
int numBlocks();
```

C prototype:
```
int numBlocks(void* card);
```

Returns:

int — Number of blocks the current data stream is divided into.

Sample Code

Description: This code determines how many blocks are in the current stream.

C++
```
int nBlocks = card->numBlocks();
```

C
```
int nBlocks = numBlocks(card);
```

dataSampleSize

Description: Returns the size in bytes of each data sample (per channel). This value is set in the Stream_Remote_MC macro. Changing the data type during a stream triggers an error condition.

C++ prototype:
```
int dataSampleSize();
```

C prototype:
```
int dataSampleSize(void* card);
```

Returns:

int	Size of each data sample in bytes.

Sample Code

Description: This code determines how many bytes are in each sample.

C++
```
int size = card->dataSampleSize();
```

C
```
int size = dataSampleSize(card);
```

getLastError

Description: This returns the most recent error.

C++ prototype:
```
int getLastError();
```

C prototype:
```
int getLastError(void* card);
```

Returns:

int	The most recent error code.

Sample Code

Description: This code determines how many channels are in the current stream.

C++
```
int nChannels = card->getLastError();
```

C
```
int nChannels = getLastError(card);
```

Examples

The example files below are installed with the TDT drivers package.

Files: C:\TDT\RPvdsEx\Examples\PO8e\PO8eTest.rcx, PO8eTest.exe, PO8e.h

Hardware: RZ2 Real-Time Processor

Overview: PO8eTest.exe connects to any PO8e card(s) in the PC, waits for a stream then displays the data rate that each PO8e card is receiving. PO8eTest.rcx streams 256 channels of floats to the PO8e card at 6.1 kHz. Launch PO8eTest.exe first, run the circuit and then set the zBusA trigger high to begin streaming.

Part 3: RX Processors

RX8 Multi I/O Processor

RX8 Overview

The RX8 is a high channel count, high sample rate analog I/O system which provides a maximum of 24 channels of analog I/O and generates a maximum sampling rate of 100 kHz per channel. Each bank of four or eight channels of I/O is user configurable with either PCM or sigma-delta converters. The 24-bit sigma-delta converters are ideal for audio applications. The 16-bit PCM analog converters have an excellent dynamic range and almost no group delay. These converters are excellent for acquiring signal information and controlling external devices, such as motors.

The RX8 is equipped with either two or five 100 MHz, 1600 MFLOPS Sharc DSPs and can control audio feedback systems or motor controls in real-time. Built in digital filters, waveform generators, and logic control components give end users the ability to design and control virtually any presentation system.

Power and Communication

The RX8 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using the Optibit (PO5/FO5) PC interface. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

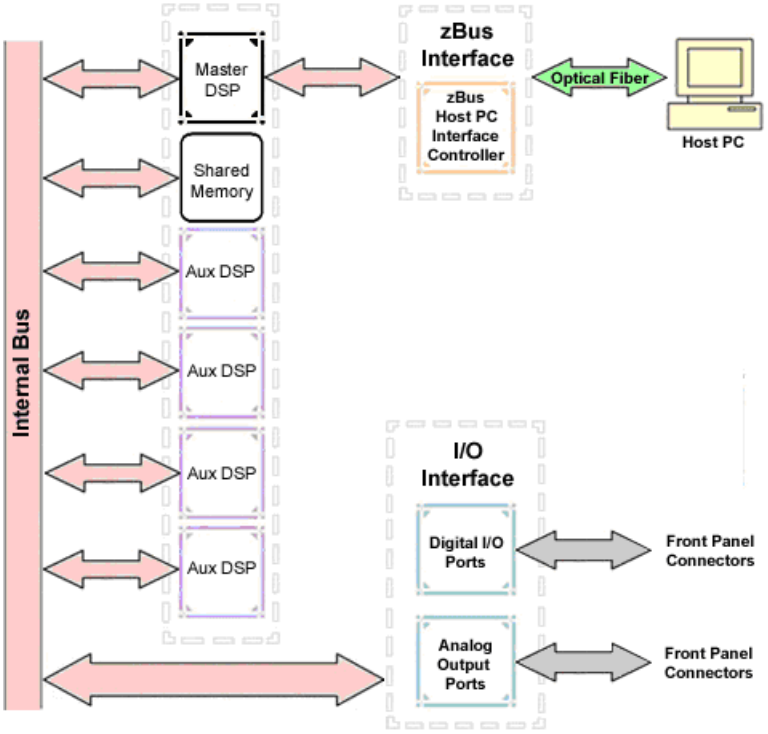
Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RX Architecture

Each RX multiprocessor device is equipped with either two or five digital signal processors (DSPs). The multi-DSP architecture allows processing tasks to be distributed across multiple processors and enables data to be transferred to the PC quickly and efficiently. The DSPs include one master and one or four auxiliary DSP(s). 128 MB SDRAM of system memory is shared by all DSPs. When designing circuits the maximum number of components for each RX DSP is 256.

Each DSP communicates with an internal bus to send and receive information from the I/O controller and the shared memory. The master DSP supervises overall system boot up and operation. The master DSP also acts as the main data interface between the zBus (host PC) and the multi-DSP environment.

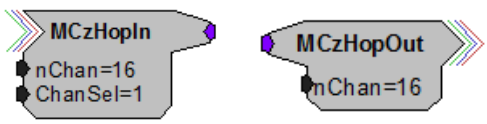
Because the zBus communicates only with the master processor, these devices operate most efficiently when the circuit related processing tasks assigned to the master DSP are minimized, allowing more processor power (cycles) for communication and overhead tasks.

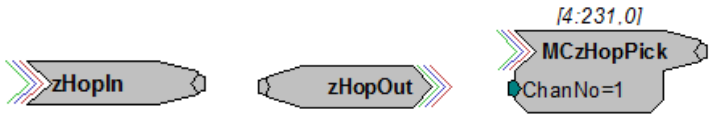


The RX8 contains two DB25 connectors for interfacing with 24 bits of digital I/O and 24 channels of analog I/O.

Distributing Data Across DSPs

In RPvdsEx data can be transferred between each of the auxiliary DSPs as well as the master DSP using zHop components.





Components such as MCzHopIn and MCzHopOut can be used for multi-channel signals while components such as zHopIn, zHopOut, and MCzHopPick are used with single-channel signals. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

The zHop Bus introduces a single sample delay. However, this delay is taken care of for the user in OpenEx when Timing and Data Saving macros are used.

See "MultiProcessor Circuit Design" in the *RPvdsEx Manual* for these and other multiprocessor circuit design techniques.

RX8 Features

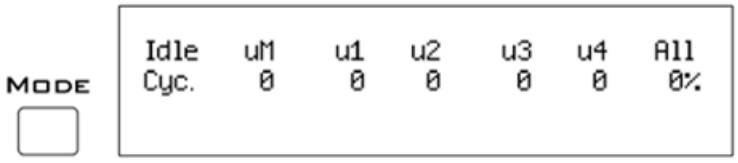
DSP Status Displays

All high performance RX multiprocessors include status lights and a display screen to report the status of the individual processors.

Status Lights

Up to five LEDs report the status of the multiprocessor's individual DSPs. When the device is turned on, they will glow steadily. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash very rapidly (~3 times per second).

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run! or Idle, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the left of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Booting DSP) or alert the user when the device's microcode needs to be reprogrammed (Firmware Blank).

Status Indicators

Cyc:	cycle usage
Ovr:	processor cycle overages
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used

Important! The status lights will flash (~3 times a second) to alert the user when a device goes over the cycle usage limit, even if only for a particular cycle. This helps to identify periodic overages caused by components in time slices.

Bits Lights

The RX8's eight Bits lights are user configurable. By default the Bits lights indicate the logic level (lit when high) for the eight bit-addressable digital I/O lines. The Bits lights can also act as logic level lights for any of the other bytes of digital I/O.

Analog Input/Output

The RX8 can have a maximum of 24 channels of analog I/O accessed via the 25-pin connector on the front panel. Each bank of up to eight channels of I/O is user configurable with either PCM or sigma-delta converters.

Sigma-delta converters provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. **When equipped with sigma-delta, the RX8 DAC Delay is 23 samples and the RX8 ADC Delay is 47 samples.**

This device can sample at rates up to ~100 kHz. For additional information on sampling rates for both PCM and sigma-delta converters, see "Realizable Sampling Rates for the RX8" on page 3-9.

Note: Because of device timing constraints at higher sampling rates, only the first 23 channels of analog I/O are processed when operating the RX8 at ~100 kHz.

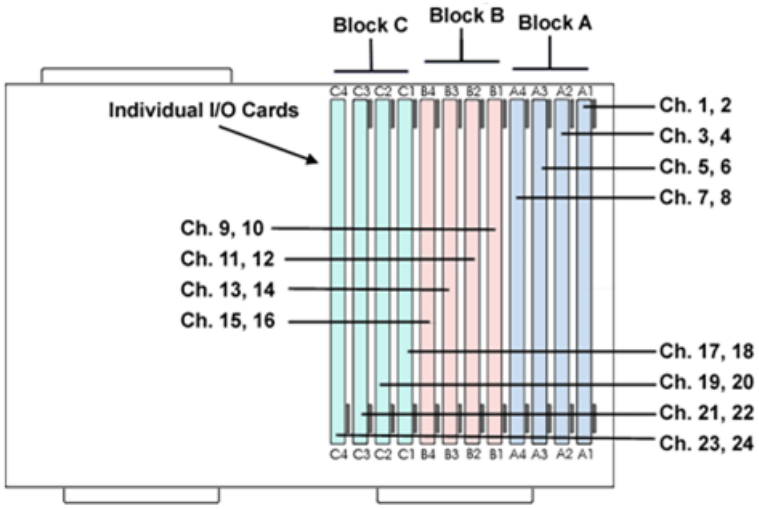
The analog I/O of each device is custom configured at the factory. Problems will arise if end users do not carefully note the configuration of their RX8 device. This topic provides information about configurations and channel numbering. The RX8's analog I/O channels are accessed via a 25-pin connector on the front panel. If you know what channel numbers your device uses, See "RX8 Technical Specifications" on page 3-10 or the Analog I/O pinout diagram.

Organization of Analog I/O Blocks

The RX8 has three blocks of I/O ports. Each block can house up to eight channels for a total of 24 channels of analog I/O. Blocks can only be filled by analog I/O modules of the same type.

For example:

A block can be configured with all D/A's or all A/D's, but not a mixture of D/A's and A/D's. In addition, the D/A's and A/D's must be of the same type (either PCM or sigma-delta).



Note: Block C can only be configured with outputs.

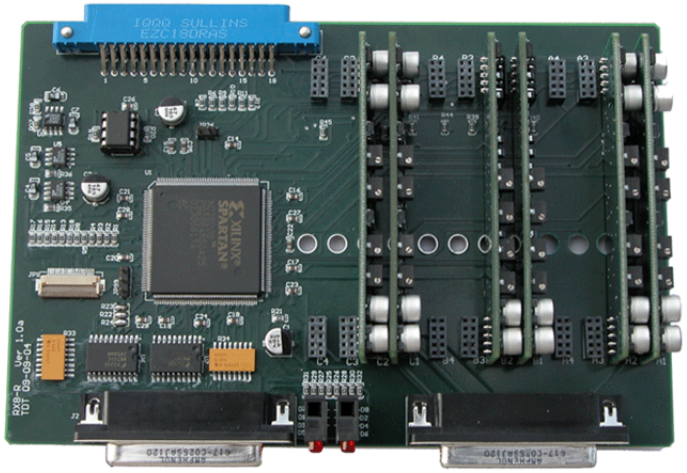
Channel Numbers

Starting with block A and ending with block C, channels are numbered sequentially from 1 to 24. The channel numbering is independent of whether the analog I/O board is an input or output.

For example:

The analog I/O of an RX8 that has four A/D's in the first two slots of Block A and four D/A's in the first two slots of Bank C, would be accessed with the A/D's as channels 1-4 and the D/A's as channels 17-20.

The photo below shows one possible configuration of the RX8's I/O boards. This configuration uses channels 1-4, 9-12, and 17-20.



Digital I/O

The RX8 processor includes 24 bits of programmable I/O in two eight bit word-addressable bytes and eight bits of bit-addressable I/O. Digital I/O lines are accessed via the 25-pin connector on the front panel and can be configured as

inputs or outputs. See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

CAUTION!: The first eight bits of bit-addressable digital I/O on RX devices are unbuffered. When used as inputs, overvoltages on these lines can cause severe damage to the system. TDT recommends when sending digital signals into the device, never send a signal with amplitude greater than five volts into any digital input.

Configuring the Programmable I/O Lines

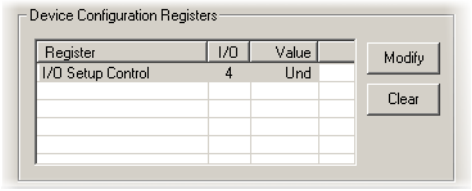
Each of the eight bit-addressable bits can be independently configured as inputs or outputs. The digital I/O lines can be configured as inputs or outputs in groups of eight bits – that is as byte A and byte B. Note, however, that the bytes must be addressed as if part of a word, not as individual bytes. See "Addressing Digital Bits In A Word" in the *RPvdsEx Manual* for more information.

By default, all bits are configured as inputs. This default setting is intended to prevent damage to equipment that might be connected to the digital I/O lines. The user can configure the bits in the RPvdsEx configuration register. The configuration register is also used to determine what the eight front panel Bits lights represent.

To access the bit configuration register:

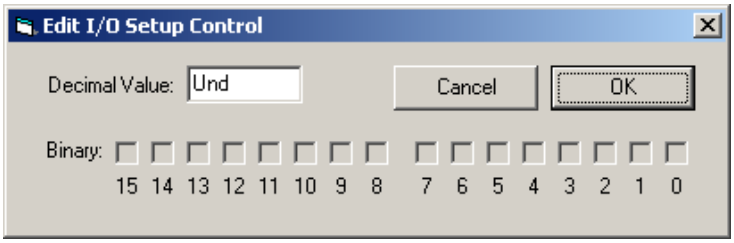
1. Click the **Device Setup** command on the **Implement** menu.
2. In the Set Hardware Parameters dialog box, click the **Device Type** box and select **RX8 Multi-Chan I/O** from the list.

   The dialog expands to display the **Device Configuration Register**.



3. Click **Modify** to display the **Edit I/O Setup Control** dialog box.

   In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.



4. To enable the check boxes, delete **Und** from the **Decimal Value** box.
5. To determine the desired value, select or clear the check boxes according to the table below. By default, all check boxes are cleared (value = 0). Selecting a check box sets the corresponding bit in the bitmask to one.

6. When the configuration is complete, click **OK** to return to the **Set Hardware Parameters** dialog box.

Bit #	Description
0-7	Each of these bits controls the configuration of one of the eight addressable bits as inputs or outputs. Setting the bit to one will configure that bit as an output.
8-9	Each of these bits controls the configuration of one of the two addressable bytes as inputs or outputs. Setting the bit to one will configure that byte as an output. bit 8 controls byte A, and bit 9 controls byte B.
10-11	bits 10 – 11 are not used.
12-14	Create a bit code that determines how the front panel Bits lights are used, see table below.
15	Not used.

Bit Codes for Controlling the Bit Lights (Boxes 12-14)

By default, check boxes 12 –14 in the **Edit I/O Setup Control** dialog box (previous diagram) are cleared to create the bit code 000. This configures the eight front panel Bits lights to act as activity lights (glow when high) for the eight bit addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as activity lights for any of the other four bytes of digital I/O.

Bit Flags	Bits set to 1	Bit Lights Used For …
000 ☐ ☐ ☐ 14 13 12	None	Logical level lights for bit-addressable I/O lines
100 ☑ ☐ ☐ 14 13 12	14	Logical level lights for byte A
101 ☑ ☐ ☑ 14 13 12	12, 14	Logical level lights for byte B

XLink

The XLink is not supported at this time.

Realizable Sampling Rates for the RX8

PCM converters support a broad range of sampling rates up to the maximum of ~100 kHz. Realizable sampling rates can easily be determined in the device set-up dialog in RPvdsEx.

Sigma-Delta converters support a more limited set of sampling rates as shown in the table below. When using Sigma-Delta converters, the user must ensure a valid sampling rate is set for the device.

Note: The Check Realizable button in the device set-up dialog in RPvdsEx is used to calculate the true sampling rate of the system when an arbitrary sampling rate is used. This rate is based on the PCM converters. If your RX8 contains any sigma-delta converters you must use the following values for arbitrary sampling rates.

Supported Arbitrary Sample Rates for Sigma-Delta Converters

Standard Rate	Actual/Arbitrary Rate (Hz)		Standard Rate	Actual/Arbitrary Rate (Hz)
6 kHz	6103.52		25 kHz	24414.06
	6975.45			27901.79
	8138.025			32552.08
	9765.63			39062.50
12 kHz	12207.03		50 kHz	48828.13
	13950.89			55803.57
	16276.04			65104.17
	19531.25			78125.00
			100 kHz	97656.25

RX8 Technical Specifications

DSP	100 MHz Sharc ADSP 21161, 600 MFLOPS Peak Two or Five
Memory	128 MB SDRAM
D/A	up to 24 channels, 16-bit PCM or 24-bit sigma-delta
Sample Rate	Up to 97.65625 kHz*†
Frequency Response	Sigma-delta or PCM: DC - Nyquist (~1/2 sample rate)
Voltage Out	+/- 10.0 Volts
S/N (typical)	Sigma-delta: 97 dB (20 Hz - 20 kHz at 10 V) PCM: 80 dB (20 Hz - 20 kHz at 10 V)
THD (typical)	Sigma-delta: -84 dB (1 kHz output at 5 Vrms) PCM: -70 dB (1 kHz output at 5 Vrms)
Sample Delay	Sigma-delta: 23 samples or PCM: 4 samples
A/D	up to 16 channels, 16-bit PCM or 24-bit sigma-delta
Sample Rate	Up to 97.65625 kHz*†

Frequency Response	Sigma-delta: DC - Nyquist (~1/2 sample rate) PCM: DC - 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
Voltage In	+/- 10.0 Volts
S/N (typical)	Sigma-delta: 97 dB (20 Hz - 20 kHz at 10 V) PCM: 80 dB (20 Hz - 20 kHz at 10 V)
THD (typical)	Sigma-delta: -84 dB (1 kHz output at 5 Vrms) PCM: -65 dB (1 kHz output at 5 Vrms)
Sample Delay	Sigma-delta: 47 samples or PCM: 4 samples
Digital I/O	24 bits programmable (8 bits addressable and a 16 bit word, addressable as 2 bytes)
Input Impedance	10 kOhms
Output Impedance	10 Ohms

***Note:** Because of device timing constraints at higher sampling rates, only the first 23 channels of analog I/O are processed when operating the RX8 at 100 kHz.

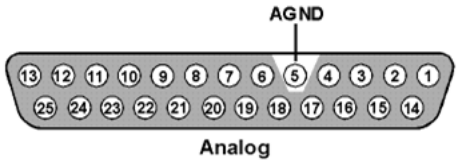
†Note: See "Realizable Sampling Rates for the RX8" on page 3-9 for a list of supported sampling rates.

Note: zBus chasis (ZB1PS) required for power and communication.

DB25 Connector Pinouts

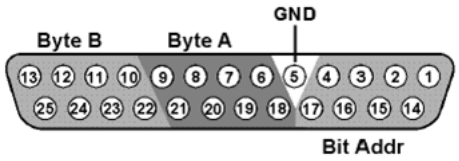
TDT Recommends accessing the RX8 I/O via a PP24 patch panel.

Analog I/O



Pin	Name	Description		Pin	Name	Description
1	A1	Analog I/O Channels Input or Output Depending on Custom Configuration		14	A2	Analog I/O Channels Input or Output Depending on Custom Configuration
2	A3			15	A4	
3	A5			16	A6	
4	A7			17	A8	
5	AGND	Analog Ground		18	A9	
6	A10	Analog I/O Channels Input or Output Depending on Custom Configuration		19	A11	
7	A12			20	A13	
8	A14			21	A15	
9	A16			22	A17	Analog Outputs
10	A18	Analog Outputs		23	A19	
11	A20			24	A21	
12	A22			25	A23	
13	A24					

Digital I/O



Pin	Name	Description		Pin	Name	Description
1	BA0	Bit Addressable digital I/O Bits 0, 2, 4, and 6		14	BA1	Bit Addressable digital I/O Bits 1, 3, 5, and 7
2	BA2			15	BA3	
3	BA4			16	BA5	
4	BA6			17	BA7	
5	GND	Digital I/O Ground		18	A0	Byte A Word addressable digital I/O Bits 0, 2, 4, and 6
6	A1	Byte A Word addressable digital I/O Bits 1, 3, 5, and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word addressable digital I/O Bits 0, 2, 4, and 6
10	B1	Byte B Word addressable digital I/O Bits 1, 3, 5, and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

RX6 Multifunction Processor

RX6 Overview

The RX6 Multifunction Processor is a high performance multiple DSP device for researchers who need to acquire or produce high sample rate signals. The RX6 supports complex research, multimodal, and experimental paradigms on a single high-bandwidth device.

The RX6 equipped with either two or five 100 MHz, 1600 MFLOPS Sharc DSPs, combines a powerful multiprocessor architecture and high-speed data transfer with two channels of 24-bit sigma-delta D/A converters and two channels of 24-bit sigma-delta A/D converters to provide superior high frequency signal generation and acquisition. Optionally, the RX6 can be equipped with a fiber optic input, allowing it to serve as a base station for a Medusa preamplifier.

Power and Communication

The RX6 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using the Optibit (PO5/FO5) PC interface. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

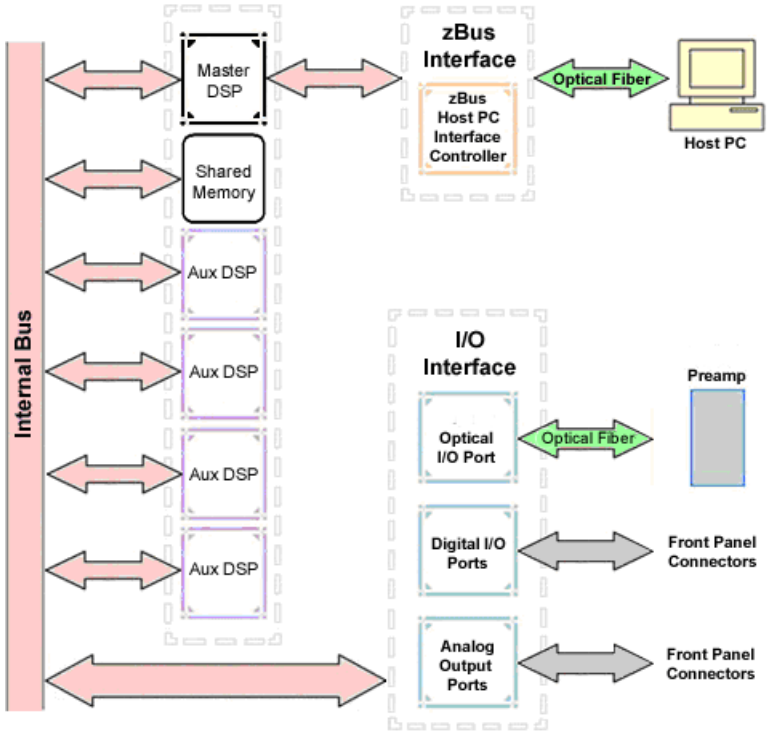
RX Architecture

Each RX multiprocessor device is equipped with either two or five digital signal processors (DSPs). The multi-DSP architecture allows processing tasks to be

distributed across multiple processors and enables data to be transferred to the PC quickly and efficiently. The DSPs include one master and one or four auxiliary DSP(s). 128 MB SDRAM of system memory is shared by all DSPs. When designing circuits the maximum number of components for each RX DSP is 256.

Each DSP communicates with an internal bus to send and receive information from the I/O controller and the shared memory. The master DSP supervises overall system boot up and operation. The master DSP also acts as the main data interface between the zBus (host PC) and the multi-DSP environment.

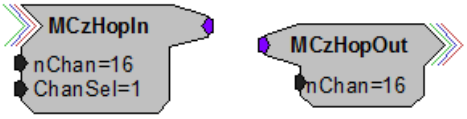
Because the zBus communicates only with the master processor, these devices operate most efficiently when the circuit related processing tasks assigned to the master DSP are minimized, allowing more processor power (cycles) for communication and overhead tasks.

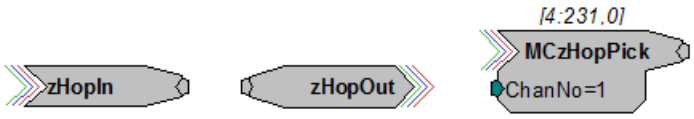


The RX6 contains a DB25 connector for interfacing with 24 bits of digital I/O and four BNC connectors for interfacing with four channels of analog I/O. An optional fiber optic Medusa preamp port enables connections for up to 16 channels of analog input.

Distributing Data Across DSPs

In RPvdsEx data can be transferred between each of the auxiliary DSPs as well as the master DSP using zHop components.





Components such as MCzHopIn and MCzHopOut can be used for multi-channel signals while components such as zHopIn, zHopOut, and MCzHopPick are used with single-channel signals. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

The zHop Bus introduces a single sample delay. However, this delay is taken care of for the user in OpenEx when Timing and Data Saving macros are used.

See "MultiProcessor Circuit Design" in the *RPvdsEx Manual* for these and other multiprocessor circuit design techniques.

RX6 Features

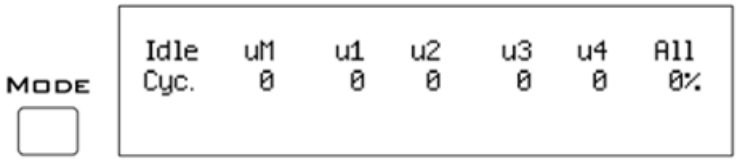
DSP Status Displays

All high performance RX multiprocessors include status lights and a display screen to report the status of the individual processors.

Status Lights

Up to five LEDs report the status of the multiprocessor's individual DSPs. When the device is turned on, they will glow steadily. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash rapidly (~3 times per second).

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run! or Idle, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the left of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Booting DSP) or alert the user when the device's microcode needs to be reprogrammed (Firmware Blank).

Status Indicators

Cyc:	cycle usage
Ovr:	processor cycle overages
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used

Important! The status lights will flash (~3 times a second) to alert the user when a device goes over the cycle usage limit, even if only for a particular cycle. This helps to identify periodic overages caused by components in time slices.

Fiber Optic Port - Optional

The RX6 can include a single fiber optic port most often used with the HTI3, but may also be used to acquire digitized signals from a Medusa preamplifier over a fiber optic cable. This provides loss-less signal acquisition between the amplifier and the base station. The port can input up to 16 channels at a maximum sampling rate of ~25 kHz. See "Fiber Oversampling", below for more information. The fiber optic port can be used with any of the Medusa preamplifiers including the RA16PA, RA4PA, or RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Channels are numbered as follows:

Amp-A	1 - 16

Fiber Oversampling

The fiber optic cable that carries the signals to the fiber optic input ports has a transfer rate limitation of 6.25 Mbits/s. With 16 channels of data and 16 bits per sample, this limitation translates to a maximum sample rate of 24.414 kHz.

However, the need may arise to run a circuit at a higher sample rate while still acquiring data via a fiber optic port. The fiber optic port on the RX6 can oversample the digitized signals that have already been sampled up to 4X or ~100 kHz. This will allow an RX6 to run a DSP chain at ~50 kHz or ~100 kHz, and still sample data acquired through an optically connected preamplifier that digitized the incoming data stream at a maximum rate of ~25 kHz.

Oversampling is performed on the base station. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

Amp Status and Clip Warning Lights

If the RX6 includes a fiber optic port for a Medusa Preamplifier, an Amp light is located to the right of the fiber optic port. This light is used to indicate the power status or provide a clip warning for the connected amplifier.

When an amplifier is not connected the Amp light will flash in a slow steady pattern. The light is lit when the amplifier is connected and begins to flash quickly when the voltage on the battery for the corresponding amplifier is low. When any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier, the corresponding light will flash rapidly to warn that clipping may occur if

the signal exceeds the maximum input voltage. See the preamplifier user guide for more information on input range and clip warnings.

Important! The Li-ion batteries voltage decreases rapidly once the battery low light is on. Data acquisition will suffer if the battery is not charged soon after the light goes on.

Amplifier Status Patterns

Light Pattern	Amplifier Status
Solid	Connected
Very slow flash (~1 every two seconds)	Not connected
Slow flash (~1 per second)	Connected and charging
Rapid flash	Battery low
Very rapid flash	Clip Warning

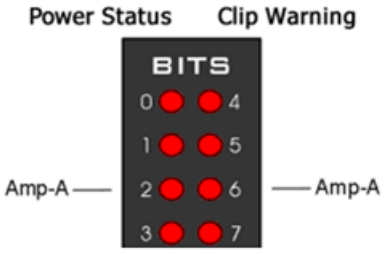
Note: If the amplifier appears to be connected and the amplifier status light is flashing slowly, check to ensure that the device is connected properly.

Bits Lights

The RX6's eight Bits lights are user configurable. By default the Bits lights indicate the logic level (light when high) for the eight bit-addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as logic level lights for any of the other two bytes of digital I/O.

Using the Bits Lights to Display Amplifier Status

Note: Because clip warning and amplifier status are always displayed using the Amp lights (located directly to the right of each fiber optic port), **TDT recommends using the Bits lights for other applications**. See "Amp Status and Clip Warning Lights" on page 3-16 for more information.



When the Bits lights are configured to display the amplifier status, the left column of lights indicates the power status and the right column indicates a clip warning for the amplifier. The table above shows the light pattern and corresponding amplifier status for the power status lights (0-3). Clip lights flash very rapidly when any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier.

Analog Input/Output

The RX6 has two channels of 24-bit, sigma-delta D/A and two channels of 24-bit, sigma-delta A/D, each accessible through BNC connectors. Sigma-delta converters provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. **The RX6 DAC Delay is 43 samples and the RX6 ADC Delay is 70 samples.**

This device can sample at rates up to ~260 kHz for a realizable bandwidth of ~109 kHz. For specific information on the actual sampling rates see "Realizable Sampling Rates for the RX6" on page 3-20.

Important! Because some RX6 models can acquire analog signals using a Medusa preamplifier via an optional fiber optic port, **the sigma-delta A/D inputs on all RX6 models are offset and accessed as A channels 128 and 129.**

Digital I/O

The RX6 processor includes 24 bits of programmable I/O in two eight bit word-addressable bytes and eight bits of bit-addressable I/O. Digital I/O lines are accessed via the 25-pin connector on the front panel and can be configured as inputs or outputs.

See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

The first four bits of digital I/O (bits 0-3) can also be used for submicrosecond event timing. See the "TimeStamp" component in the *RPvdsEx Manual* for more information.

CAUTION!: The first eight bits of bit-addressable digital I/O on RX devices are unbuffered. When used as inputs, overvoltages on these lines can cause severe damage to the system. TDT recommends when sending digital signals into the device, never send a signal with amplitude greater than five volts into any digital input.

Configuring the Programmable I/O Lines

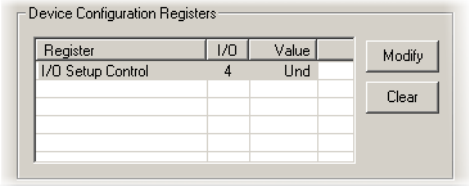
Each of the eight bit-addressable bits can be independently configured as inputs or outputs. The digital I/O lines can be configured as inputs or outputs in groups of eight bits – that is as byte A and byte B. Note, however, that the bytes must be addressed as if part of a word, not as individual bytes. See "Addressing Digital Bits In A Word" in the *RPvdsEx Manual* for more information.

By default, all bits are configured as inputs. This default setting is intended to prevent damage to equipment that might be connected to the digital I/O lines. The user can configure the bits in the RPvdsEx configuration register. The configuration register is also used to determine what the eight front panel Bits lights represent.

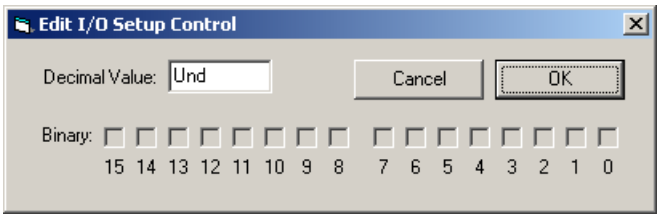
To access the bit configuration register in RPvdsEx:

1. Click the **Device Setup** command on the **Implement** menu.
2. In the **Set Hardware Parameters** dialog box, click the Device Type box and select the RX6 Multi-Function from the list.

   The dialog expands to display the **Device Configuration Register**.



3. Click **Modify** to display the **Edit I/O Setup Control** dialog box.



In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.

4. To enable the check boxes, delete **Und** from the **Decimal Value** box.
5. To determine the desired value, select or clear the check boxes according to the table below. By default, all check boxes are cleared (value = 0). Selecting a check box sets the corresponding bit in the bitmask to one.
6. When the configuration is complete, click **OK** to return to the **Set Hardware Parameters** dialog box.

Bit_#	Description
0-7	Each of these bits controls the configuration of one of the eight addressable bits as inputs or outputs. Setting the bit to one will configure that bit as an output.
8-9	Each of these bits controls the configuration of one of the two addressable bytes as inputs or outputs. Setting the bit to one will configure that byte as an output. bit 8 controls byte A, and bit 9 controls byte B.
10-11	bits 10 – 11 are not used.
12-14	Create a bit code that determines how the front panel Bits lights are used, see table below.
15	Not used.

Bit Codes for Controlling the Bit Lights (Boxes 12-14)

By default, check boxes 12 –14 in the **Edit I/O Setup Control** dialog box (previous diagram) are cleared to create the bit code 000. This configures the eight front panel Bits lights to act as activity lights (glow when high) for the eight bit addressable digital I/O lines. The Bits lights can also be configured to provide

information about amplifier status or act as activity lights for any of the other four bytes of digital I/O.

Bit Flags	Bits set to 1	Bit Lights Used For ...
000 	None	Logical level lights for bit-addressable I/O lines
010 	13	Amplifier Clip Warning/Power Status display
100 	14	Enable logical level lights for byte A
101 	12, 14	Enable logical level lights for byte B

XLink

The XLink is not supported at this time.

Realizable Sampling Rates for the RX6

The following table shows the actual sampling rate values for the RX6. The X's on the table correspond to realizable frequencies for the A, DAC, Optical input, and Digital I/O. For example, the Digital I/O accepts a sampling rate up to 390625.0 Hz and the Audio ADC and DAC each accept a sampling rate up to 260416.67 Hz. The maximum realizable sampling rates are accepted as the maximum sampling rate without distortion. Each of the inputs and outputs will function above these sampling rates, but distortion will be present in the signal.

Standard Rate	Actual/Arbitrary Rate (Hz)	Audio A	Audio DAC	Optical/AMP Input	Digital I/O
6 kHz	6103.52	x	x	x	x
	6975.45	x	x		x
	8138.025	x	x		x
	9765.63	x	x		x
12 kHz	12207.03	x	x	x	x
	13950.89	x	x		x
	16276.04	x	x		x

Standard Rate	Actual/Arbitrary Rate (Hz)	Audio A	Audio DAC	Optical/AMP Input	Digital I/O
	19531.25	x	x		x
25 kHz	24414.06	x	x	x	x
	27901.79	x	x		x
	32552.08	x	x		x
	39062.50	x	x		x
50 kHz	48828.13	x	x	x*	x
	55803.57	x	x		x
	65104.17	x	x		x
	78125.00	x	x		x
100 kHz	97656.25	x	x	x*	x
	111607.14	x	x		x
	130208.33	x	x		x
	156250.00	x	x		x
200 kHz	195312.50	x	x		x
	223214.29	x	x		x
	260416.67	x	x		x
	312500.00				x
400 kHz	390625.00				x

[x] = Fully functional [x*] = Sampling limited to 25KHz

RX6 Technical Specifications

The RX6 can be equipped with a fiber optic input port which may be used with a Medusa or Adjustable Gain preamplifier. Specifications for the AD converters of those devices are found under the preamplifier's technical specifications.

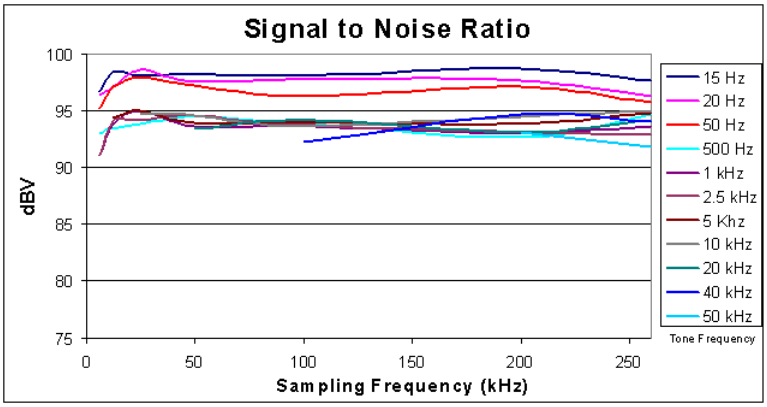
DSP	100 MHz Sharc ADSP 21161, 600 MFLOPS Peak Two or Five
Memory	128 MB SDRAM
D/A	2 channels, 24-bit sigma-delta
Sample Rate	Up to 260.4166 kHz
Frequency Response	DC – 109 kHz
Voltage Out	+/- 10.0 Volts
S/N (typical)	105 dB (20 Hz - 20 kHz at 10 V)

THD (typical)	-92 dB (1 kHz output at 5 Vrms)
Sample Delay	43 samples
A/D	2 channels, 24-bit sigma-delta
Sample Rate	Up to 260.4166 kHz
Frequency Response	DC – 109 kHz
Voltage In	+/- 10.0 Volts
S/N (typical)	105 dB (20 Hz - 20 kHz at 10 V)
THD (typical)	-95 dB (1 kHz input at 5 Vrms)
Sample Delay	70 samples
Fiber Optic Ports	Optional Input (Medusa)
Digital I/O	24 bits programmable (8 bits addressable and a 16 bit word, addressable as 2 bytes)
Input Impedance	10 kOhms
Output Impedance	10 Ohms

Note: zBus chasis (ZB1PS) required for power and communication.

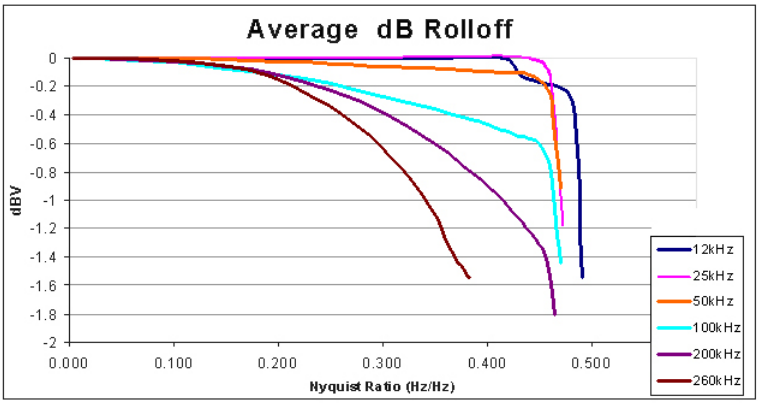
Signal-to-Noise Ratio Diagram

The following graph is of the signal to noise ratio with varying signal frequencies.



dB Rolloff Diagram

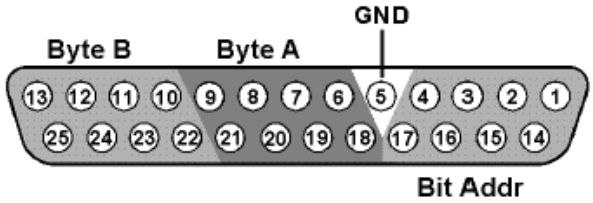
This graph shows the dB rolloff for the RX6 with varying sampling frequencies for both D/A and A/D. The sample delay remains relatively stable for varying frequencies.



DB25 Connector Pinout

TDT recommends the PP24 patch panel for accessing the RX6 I/O.

Digital I/O



Pin	Name	Description		Pin	Name	Description
1	BA0	Bit Addressable digital I/O Bits 0, 2, 4, and 6		14	BA1	Bit Addressable digital I/O Bits 1, 3, 5, and 7
2	BA2			15	BA3	
3	BA4			16	BA5	
4	BA6			17	BA7	
5	GND	Digital I/O Ground		18	A0	Byte A Word addressable digital I/O Bits 0, 2, 4, and 6
6	A1	Byte A Word addressable digital I/O Bits 1, 3, 5, and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word addressable digital I/O Bits 0, 2, 4, and 6
10	B1	Byte B Word addressable digital I/O Bits 1, 3, 5, and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

RX5 Pentusa Base Station

RX5 Overview

The RX5 Pentusa is a powerful multiple DSP device well suited for processing high channel count neurophysiology data in real-time. A streamlined hardware interface provides connections to up to 64 channels for neurophysiological data acquisition.

The RX5 is equipped with either two or five 100 MHz, 1600 MFLOPS Sharc DSPs and serves as a base station for up to four Medusa preamplifiers to form a powerful multi-channel amplifier system. The multiprocessor architecture provides simultaneous ~25 kHz sampling on every channel, 16-bit precision, fiber optic isolation, and the power of user-programmable real-time DSPs.

The RX5 also features front panel status indicators, 40 bits of configurable digital I/O, and four D/A converters for versatile experiment control and stimulus generation.

Power and Communication

The RX5 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using the Optibit (PO5/FO5) PC interface. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

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Each DSP communicates with an internal bus to send and receive information from the I/O controller and the shared memory. The master DSP supervises overall system boot up and operation. The master DSP also acts as the main data interface between the zBus (host PC) and the multi-DSP environment.

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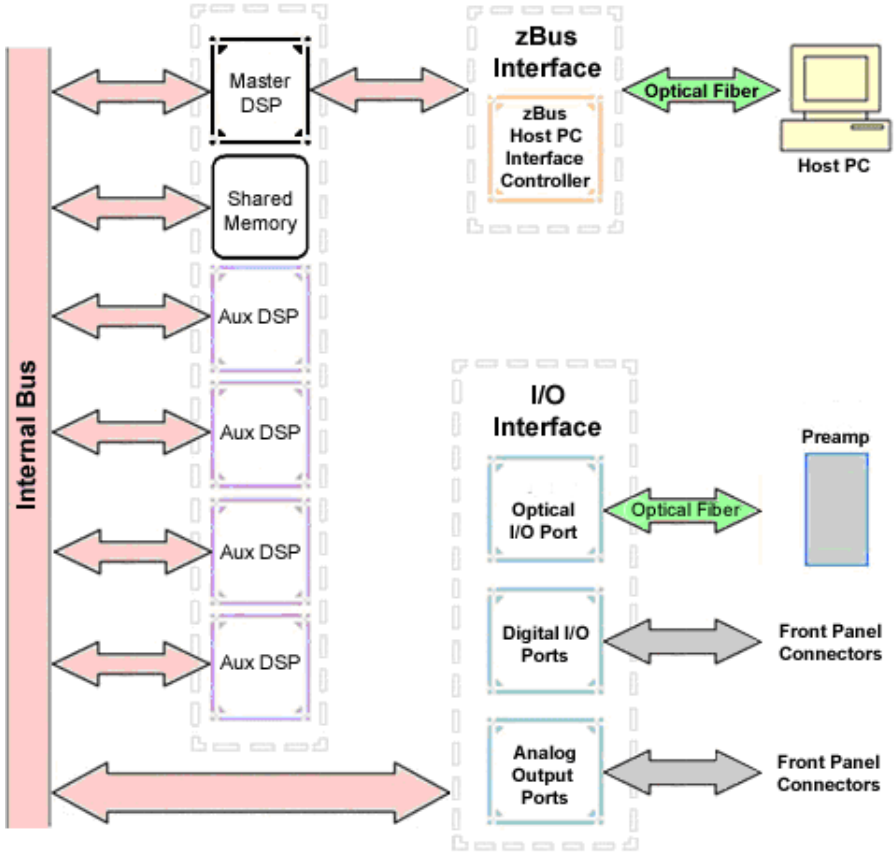

The RX5 contains two DB25 connectors for interfacing with 40 bits of digital I/O and 4 channels of analog output. A BNC connector is provided for access to the first analog output channel. Four fiber optic Medusa preamp ports enable connections for up to 64 channels of analog input.

Distributing Data Across DSPs

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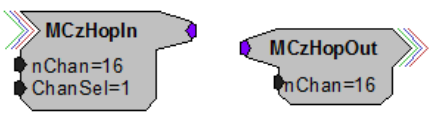

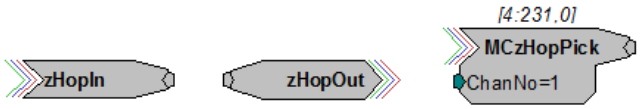

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See "MultiProcessor Circuit Design" in the *RPvdsEx Manual* for these and other multiprocessor circuit design techniques.

RX5 Features

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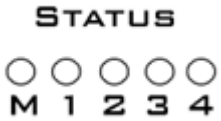
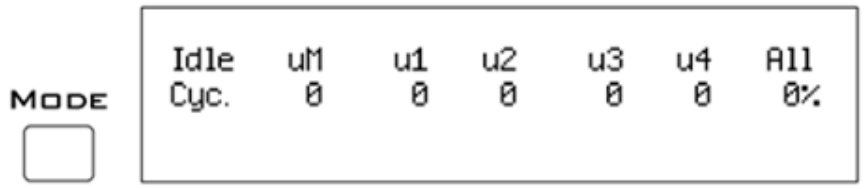
Status Lights



Up to five LEDs report the status of the multiprocessor's individual DSPs. When the device is turned on, they will glow steadily. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash rapidly (~3 times per second).

Front Panel Display Screen



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The user can cycle through the various status indicators using the Mode button to the left of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as

booting status (Booting DSP) or alert the user when the device's microcode needs to be reprogrammed (Firmware Blank).

Status Indicators

Cyc:	cycle usage
Ovr:	processor cycle overages
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used

Important! The status lights will flash (~3 times a second) to alert the user when a device goes over the cycle usage limit, even if only for a particular cycle. This helps to identify periodic overages caused by components in time slices.

Fiber Optic Ports

The RX5 base station acquires digitized signals from a Medusa preamplifier over a fiber optic cable. This provides loss-less signal acquisition between the amplifier and the base station. Two or four fiber optic ports are provided to support simultaneous acquisition from up to four preamplifiers. Each port can input up to 16 channels at a maximum sampling rate of ~25 kHz. The first two ports provide oversampling. See "Fiber Oversampling", below for more information.

The fiber optic ports can be used with any of the Medusa preamplifiers including the RA16PA, RA4PA, or RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Channels are numbered as follows:

Amp-A	1 – 16
Amp-B	17 – 32
Amp-C	33 – 48
Amp-D	49 - 64

Fiber Oversampling

The fiber optic cable that carries the signals to the fiber optic input ports has a transfer rate limitation of 6.25 Mbits/s. With 16 channels of data and 16 bits per sample, this limitation translates to a maximum sample rate of 24.414 kHz.

However, the need may arise to run a circuit at a higher sample rate while still acquiring data via a fiber optic port. The first two fiber optic ports can oversample the digitized signals that have already been sampled up to 4X or ~100 kHz. This will allow an RX5 to run a DSP chain at ~50 kHz or ~100 kHz, and still sample data acquired through an optically connected preamplifier that digitized the incoming data stream at a maximum rate of ~25 kHz.

Oversampling is performed on the base station. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

When acquiring up to 16 channels of data on the first fiber optic input port of the RX5, the signals will be oversampled 4X to 100 kHz. If data is being acquired only on the first two fiber optic ports, the signals will be oversampled 2X to ~50 kHz.

Amp Status and Clip Warning Lights

Amp lights are located to the right of each fiber optic port. These lights are used to indicate the power status or provide a clip warning for the connected amplifiers.

When an amplifier is not connected the Amp light will flash in a slow steady pattern. The light is lit when the amplifier is connected and begins to flash quickly when the voltage on the battery for the corresponding amplifier is low. When any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier, the corresponding light will flash rapidly to warn that clipping may occur if the signal exceeds the maximum input voltage. See the corresponding preamplifier section for more information on input range and clip warnings.

Important! The Li-ion batteries voltage decreases rapidly once the battery low light is on. Data acquisition will suffer if the battery is not charged soon after the light goes on.

Amplifier Status Patterns

Light Pattern	Amplifier Status
Solid	Connected
Very slow flash (~1 every 2 seconds)	Not connected
Slow flash (~1 per second)	Connected and charging
Rapid flash	Battery low
Very rapid flash	Clip Warning

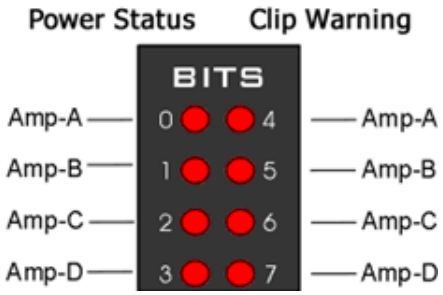
Note: If the amplifier appears to be connected and the amplifier status light is flashing slowly, check to ensure that the device is connected properly.

Bits Lights

The RX5's eight Bits lights are user configurable. By default the Bits lights indicate the logic level (light when high) for the eight bit-addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as logic level lights for any of the other four bytes of digital I/O.

Using the Bits Lights to Display Amplifier Status

Note: Because clip warning and amplifier status are always displayed using the Amp lights (located directly to the right of each fiber optic port), **TDT recommends using the Bits lights for other applications.** See "Amp Status and Clip Warning Lights" on page 3-29 for more information.



When the Bits lights are configured to display the amplifier status, the left column of lights indicates the power status and the right column indicates a clip warning for the corresponding amplifier.

"Amplifier Status Patterns" on page 3-29 shows the light pattern and corresponding amplifier status for the power status lights (0 - 3). Clip lights flash very rapidly when any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier.

Analog Output

The RX5 is equipped with four channels of 16-bit PCM D/A. The sampling rate is user selectable up to a maximum of ~100 kHz. The D/A is DC coupled and has a built-in upsampler for improved audio playback. The upsampler is controlled through one of the RX5's programmable bits and can be turned off to allow the D/A to drive external devices such as a stimulator. Channel one analog output can be accessed via a front Panel BNC (DAC-1). All four analog channels can be accessed via the DB25 Multi I/O connector (pins 14 – 17).

Digital I/O

The RX5 processor has 40 digital I/O lines. Eight bits are bit-addressable. The remaining 32 bits are four word-addressable bytes. Digital I/O lines are accessed via the two 25-pin connectors on the front of the RX5. See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

CAUTION!: The first eight bits of bit-addressable digital I/O on RX devices are unbuffered. When used as inputs, overvoltages on these lines can cause severe damage to the system. TDT recommends when sending digital signals into the device, never send a signal with amplitude greater than five volts into any digital input.

Configuring the Programmable I/O Lines

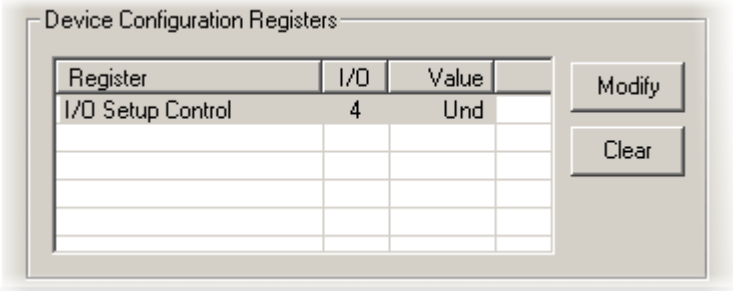
Each of the eight bit-addressable lines can be independently configured as inputs or outputs. The digital I/O lines can be configured as inputs or outputs in groups of eight bits – that is as byte A, byte B, byte C, and byte D. Note, however, that the bytes must be addressed as if part of a word, not as individual bytes. See "Addressing Digital Bits In A Word" in the *RPvdsEx Manual* for more information.

By default, all bits are configured as inputs. This default setting is intended to prevent damage to equipment that might be connected to the digital I/O lines. The user can configure the bits in the RPvdsEx configuration register. The configuration register is also used to determine what the eight front panel Bits lights represent.

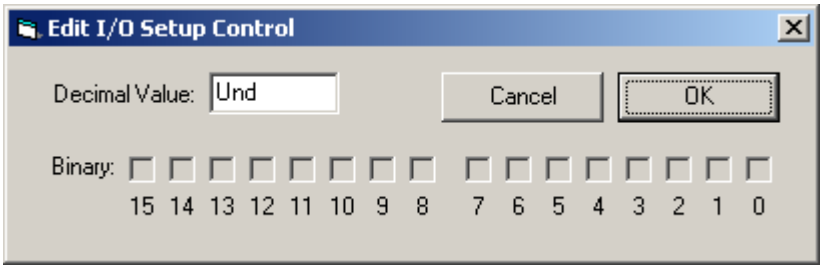
To access the bit configuration register in RPvdsEx:

1. Click the **Device Setup** command on the **Implement** menu.
2. In the **Set Hardware Parameters** dialog box, click the **Device Type** box and select the **RX5 Pentusa** from the list.

   The dialog expands to display the **Device Configuration Register**.



3. Click **Modify** to display the Edit I/O Setup Control dialog box.



In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.

4. To enable the check boxes, delete **Und** from the **Decimal Value** box.
5. To determine the desired value, select or clear the check boxes according to the table below. By default, all check boxes are cleared (value = 0). Selecting a check box sets the corresponding bit in the bitmask to one.
6. When the co**nfiguration is complete, click OK to return to the** Set Hardware Parameters dialog box.

Bit_#	Description
0-7	Each of these bits controls the configuration of one of the eight addressable bits as inputs or outputs. Setting the bit to one will configure that bit as an output.
8-11	Each of these bits controls the configuration of one of the four addressable bytes as inputs or outputs. Setting the bit to one will configure that byte as an output. bit 8 - byte A, bit 9 - byte B, bit 10 - byte C, and bit 11 - byte D
12-14	Create a bit code that determines how the front panel Bits lights are used, see table below.
15	Setting the bit to one will disable the D/A upsampler.

Bit Codes for Controlling the Bit Lights (Boxes 12-14)

By default, check boxes 12 –14 in the Edit I/O Setup Control dialog box (previous diagram) are cleared to create the bit code 000. This configures the eight front panel Bits lights to act as activity lights (lit when high) for the eight bit addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as activity lights for any of the other four bytes of digital I/O.

Bit Flags	Bits set to 1	Bit Lights Used For ...
000 	None	Logical level lights for bit-addressable I/O lines
010 	13	Amplifier Clip Warning/Power Status display
100 	14	Enable logical level lights for byte A
101 	12, 14	Enable logical level lights for byte B
110 	13, 14	Enable logical level lights for byte C
111 	12, 13, 14	Enable logical level lights for byte D

XLink

The XLink is not supported at this time.

RX5 Technical Specifications

Specifications for the A/D converters are found under the preamplifier's technical specifications.

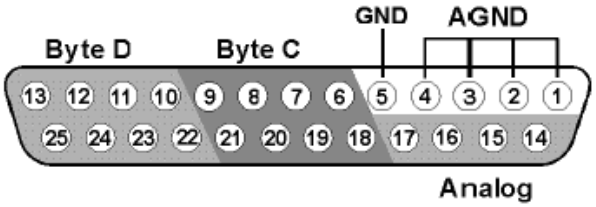
DSP	100 MHz Sharc ADSP 21161, 600 MFLOPS Peak Two or Five
Memory	128 MB SDRAM (Shared)
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 97.65625 kHz (8X upsampled to 200 kHz default operation)
Frequency Response	DC - Nyquist (~1/2 sample rate)
Voltage Out	+/- 10.0 Volts
Voltage Out Accuracy	+/- 10%
S/N (typical)	84 dB (20 Hz to 25 KHz) 82 dB with upsampling disabled
THD (typical)	-77 dB for 1 kHz output at 5 Vrms -74 dB with upsampling disabled
Output Impedance	10 Ohm
Fiber Optic Ports	Two or Four Inputs (Medusa)
Digital I/O	40 bits programmable (8 bits bit-addressable and a 32 bit word, addressable as 4 bytes)

Note: zBus chasis (ZB1PS) required for power and communication.

DB25 Connector Pinouts

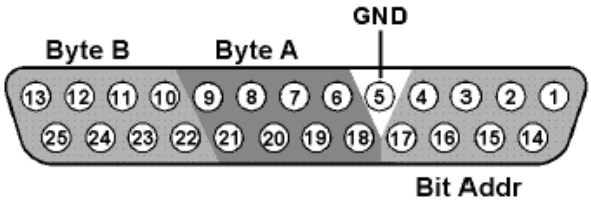
TDT recommends the PP24 patch panel for accessing the RX5 I/O.

Multi I/O



Pin	Name	Description		Pin	Name	Description
1	AGND	Analog Ground		14	A1	Analog Output Channels
2				15	A2	
3				16	A3	
4				17	A4	
5	GND	Digital I/O Ground		18	C0	Byte C Word addressable digital I/O Bits 0, 2, 4, and 6
6	C1	Byte C Word addressable digital I/O Bits 1, 3, 5, and 7		19	C2	
7	C3			20	C4	
8	C5			21	C6	
9	C7			22	D0	Byte D Word addressable digital I/O Bits 0, 2, 4, and 6
10	D1	Byte D Word addressable digital I/O Bits 1, 3, 5, and 7		23	D2	
11	D3			24	D4	
12	D5			25	D6	
13	D7					

Digital I/O



Pin	Name	Description		Pin	Name	Description
1	BA0	Bit Addressable digital I/O Bits 0, 2, 4, and 6		14	BA1	Bit Addressable digital I/O Bits 1, 3, 5, and 7
2	BA2			15	BA3	
3	BA4			16	BA5	
4	BA6			17	BA7	
5	GND	Digital I/O Ground		18	A0	Byte A Word addressable digital I/O Bits 0, 2, 4, and 6
6	A1	Byte A Word addressable digital I/O Bits 1, 3, 5, and 7		19	A2	
7	A3			20	A4	
8	A5			21	A6	
9	A7			22	B0	Byte B Word addressable digital I/O Bits 0, 2, 4, and 6
10	B1	Byte B Word addressable digital I/O Bits 1, 3, 5, and 7		23	B2	
11	B3			24	B4	
12	B5			25	B6	
13	B7					

RX7 Stimulator Base Station

RX7 Overview

The RX7 base station is a high performance processor available with either two or five 100 MHz, 1600 MFLOPS Sharc DSPs. You can use the base station's onboard DSPs to design and generate complex arbitrary waveforms or complex patterns of biphasic pulses in real-time. The RX7 has been developed specifically for microstimulation applications. As part of TDT's RX7G MicroStimulator system, the RX7's primary role is to control the MS16 stimulus isolator, transferring hardware control and stimulation information across fiber optics. This proven digital communication system optically isolates the RX7 from the electrical stimulator, eliminating AC power surges and noise. For more information see "MS4/MS16 Stimulus Isolator" on page 8-31.

The RX7 includes 40 bits of digital I/O, analog output, and can include one or two fiber optic input ports for acquisition of digitized data from Medusa preamplifiers. Acquired signals can be filtered, rectified, or smoothed for stimulus output or dynamic real-time stimulus control based on analog control signals from virtually any signal source.

Power and Communication

The RX7 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using the Optibit (PO5/FO5) PC interface. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

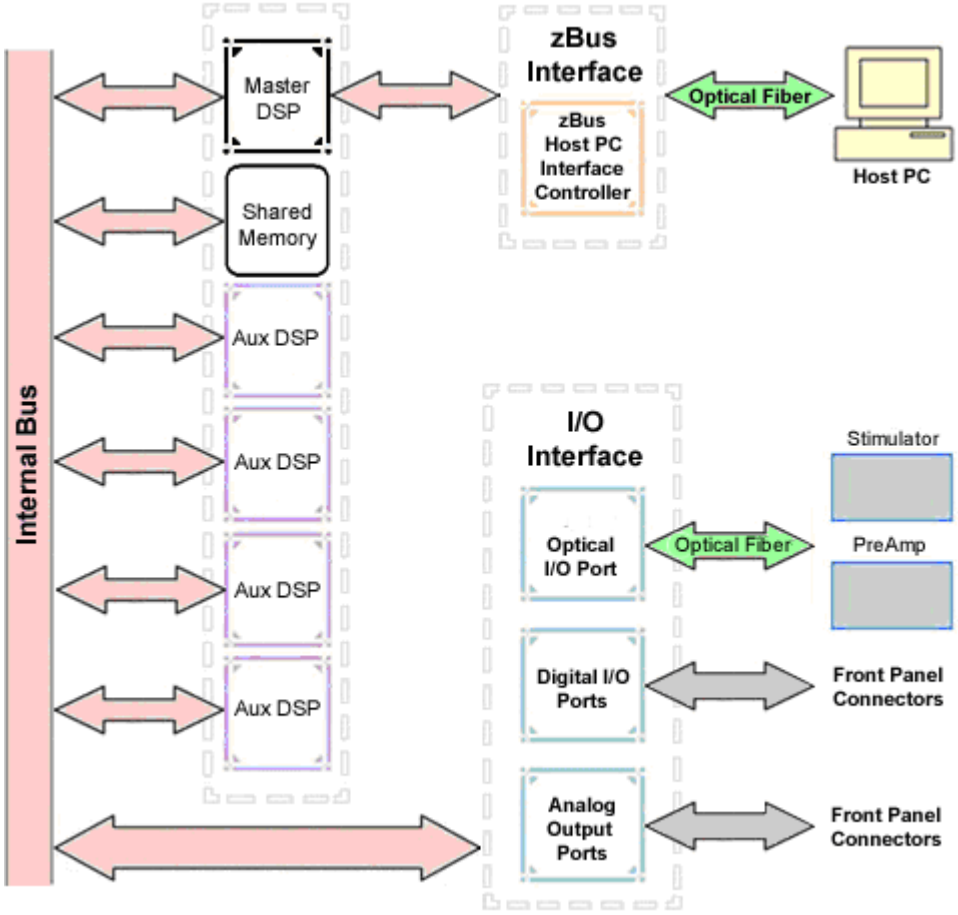
Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RX Architecture

Each RX multiprocessor device is equipped with either two or five digital signal processors (DSPs). The multi-DSP architecture allows processing tasks to be distributed across multiple processors and enables data to be transferred to the PC quickly and efficiently. The DSPs include one master and one or four auxiliary DSP(s). 128 MB SDRAM of system memory is shared by all DSPs. When designing circuits the maximum number of components for each RX DSP is 256.

Each DSP communicates with an internal bus to send and receive information from the I/O controller and the shared memory. The master DSP supervises overall system boot up and operation. The master DSP also acts as the main data interface between the zBus (host PC) and the multi-DSP environment.

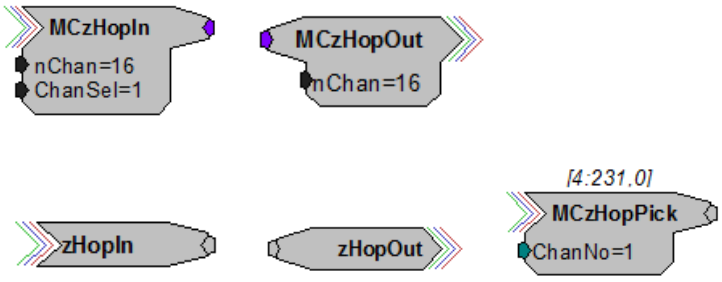
Because the zBus communicates only with the master processor, these devices operate most efficiently when the circuit related processing tasks assigned to the master DSP are minimized, allowing more processor power (cycles) for communication and overhead tasks.



The RX7 contains two DB25 connectors for interfacing with 40 bits of digital I/O and 4 channels of analog output. A BNC connector is provided for access to the first analog output channel. One or two fiber optic Medusa preamp ports enable connections for up to 32 channels of analog input.

Distributing Data Across DSPs

In RPvdsEx data can be transferred between each of the auxiliary DSPs as well as the master DSP using zHop components.



Components such as MCzHopIn and MCzHopOut can be used for multi-channel signals while components such as zHopIn, zHopOut, and MCzHopPick are used with single-channel signals. Up to 126 pairs can be used in a single RPvdsEx circuit.

Bus Related Delays

The zHop Bus introduces a single sample delay. However, this delay is taken care of for the user in OpenEx when Timing and Data Saving macros are used.

See "MultiProcessor Circuit Design" in the *RPvdsEx Manual* for these and other multiprocessor circuit design techniques.

RX7 Features

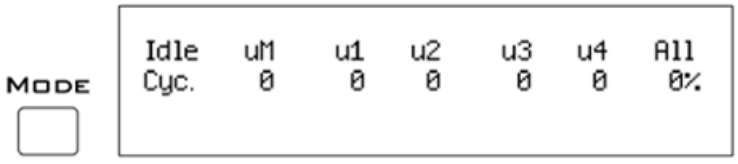
DSP Status Displays

All high performance RX multiprocessors include status lights and a display screen to report the status of the individual processors.

Status Lights

Up to five LEDs report the status of the multiprocessor's individual DSPs. When the device is turned on, they will glow steadily. If the demands on a DSP exceed 99% of its capacity on any given cycle, the corresponding LED will flash very rapidly (~3 times per second).

Front Panel Display Screen



The front panel display screen reports detailed information about the status of the system. The display includes two lines. The top line reports the system mode, Run! or Idle, and displays heading labels for the second line. The second line reports the user's choice of status indicators for each DSP followed by an aggregate value.

The user can cycle through the various status indicators using the Mode button to the left of the display. Push and release the button to change the display or push and hold the button for one second then release to automatically cycle through each of the display options. The display screen may also report system status such as booting status (Booting DSP) or alert the user when the device's microcode needs to be reprogrammed (Firmware Blank).

Status Indicators

Cyc:	cycle usage
Ovr:	processor cycle overages
Bus%:	percentage of internal device's bus capacity used
I/O%:	percentage of data transfer capacity used

Important! The status lights will flash (~3 times a second) to alert the user when a device goes over the cycle usage limit, even if only for a particular cycle. This helps to identify periodic overages caused by components in time slices.

Fiber Optic Output Port (Stimulator)

The output port, labeled Stimulator, can be used to transfer microstimulation waveforms to the MS16/MS4 Stimulus Isolator and/or to control its digital output. See the "MS4/MS16 Stimulus Isolator" on page 8-31.

Important! This fiber optic port is disabled if the sampling rate of the system is set to a value greater than ~25 kHz.

Fiber Optic Input Ports (Amp-A and Amp-B)

The RX7 base station can acquire digitized signals from a Medusa preamplifier over a fiber optic cable. This provides loss-less signal acquisition between the amplifier and the base station. Up to two fiber optic ports are provided to support simultaneous acquisition from up to two preamplifiers. Each port can input up to 16 channels at a maximum sampling rate of ~25 kHz. The fiber optic ports provide oversampling. See "Fiber Oversampling", below for more information.

The fiber optic ports can be used with any of the Medusa preamplifiers including the RA16PA, RA4PA, or RA8GA. The channel numbers for each port begin at a fixed offset regardless of the number of channels available on the connected device.

Channels are numbered as follows:

Amp-A	1 – 16
Amp-B	17 – 32

Fiber Oversampling (acquisition only)

The fiber optic cable that carries the signals to the fiber optic input ports on the RX7 has a transfer rate limitation of 6.25 Mbits/s. With 16 channels of data and 16 bits per sample, this limitation translates to a maximum sampling rate of ~25 kHz.

However, the need may arise to run a circuit at a higher sampling rate while still acquiring data via a fiber optic port. The first two fiber optic ports on an RX device can oversample the digitized signals that have already been sampled up to 4X or ~100 kHz. This will allow an RX7 to run a DSP chain at ~50 kHz or ~100 kHz, and still sample data acquired through an optically connected preamplifier that digitized the incoming data stream at its maximum rate of ~25 kHz.

Oversampling is performed on the base station. The signals being acquired will still be sampled at ~25 kHz on the preamplifier. This means that, even with oversampling, signals acquired by an optically connected preamplifier are still governed by the bandwidth and frequency response of the preamplifier.

When acquiring up to 16 channels of data on the first fiber optic input port of the RX7, the signals will be oversampled 4X to ~100 kHz. If the RX7 is equipped with a second fiber optic input port and data is being acquired on both ports, the signals on second port will be oversampled 2X to ~50 kHz.

Amp Status and Clip Warning Lights

Amp lights are located to the right of each fiber optic port. These lights are used to indicate the power status or provide a clip warning for the connected amplifiers.

When an amplifier is not connected the Amp light will flash in a slow steady pattern. The light is lit when the amplifier is connected and begins to flash quickly when the voltage on the battery for the corresponding amplifier is low. When any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier, the corresponding light will flash rapidly to warn that clipping may occur if the signal exceeds the maximum input voltage. See the corresponding preamplifier section for more information on input range and clip warnings.

Important! The Li-ion batteries voltage decreases rapidly once the battery low light is on. Data acquisition will suffer if the battery is not charged soon after the light goes on.

Amplifier Status Patterns

Light Pattern	Amplifier Status
Solid	Connected
Very slow flash (~1 every two seconds)	Not connected
Slow flash (~1 per second)	Connected and charging
Rapid flash	Battery low
Very rapid flash	Clip Warning

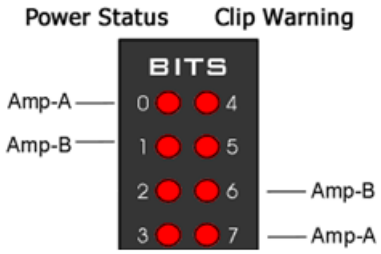
Note: If the amplifier appears to be connected and the amplifier status light is flashing slowly, check to ensure that the device is connected properly.

Bits Lights

The RX7's eight Bits lights are user configurable. By default the Bits lights indicate the logic level (light when high) for the eight bit-addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as logic level lights for any of the other four bytes of digital I/O.

Using the Bits Lights to Display Amplifier Status

Note: Because clip warning and amplifier status are always displayed using the Amp lights (located directly to the right of each fiber optic port), TDT recommends using the Bits lights for other applications. See "Amp Status and Clip Warning Lights " on page 3-39, for more information.



When the Bits lights are configured to display the amplifier status, the left column of lights indicates the power status and the right column indicates a clip warning for the corresponding amplifier.

"Amplifier Status Patterns" on page 3-39 shows the light pattern and corresponding amplifier status for the power status lights (0 - 3). Clip lights flash very rapidly when any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier.

Analog Output

The RX7 is equipped with four channels of 16-bit PCM D/A. The sampling rate is user selectable up to a maximum of ~100 kHz. The D/A is DC coupled and has a built-in upsampler for improved audio playback. The upsampler is controlled through one of the RX7's programmable bits and can be turned off to allow the D/A to drive external devices such as a stimulator. Channel one analog output can be accessed via a front Panel BNC (DAC-1). All four analog channels can be accessed via the DB25 Multi I/O connector (pins 14 – 17).

Important! When using the RX7 with the stimulus isolator, the sampling rate set for this device cannot exceed ~25 kHz—a limitation of the fiber optic connection between the RX7 and the stimulus isolator.

Digital I/O

The RX7 base station has 40 digital I/O lines. Eight bits are bit-addressable. The remaining 32 bits are four word-addressable bytes. Digital I/O lines are accessed via the two 25-pin connectors on the front of the RX7. See the "Digital I/O Circuit Design" section of the *RPvdsEx Manual* for more information on programming the digital I/O.

⚠ CAUTION!: The first eight bits of bit-addressable digital I/O on RX devices are unbuffered. When used as inputs, overvoltages on these lines can cause severe damage to the system. TDT recommends when sending digital signals into the device, never send a signal with amplitude greater than five volts into any digital input.

Configuring the Programmable I/O Lines

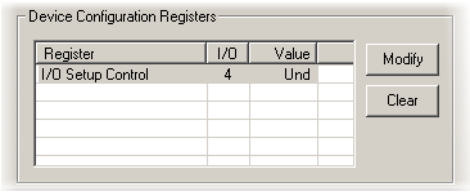
Each of the eight bit-addressable lines can be independently configured as inputs or outputs. The digital I/O lines can be configured as inputs or outputs in groups of eight bits – that is as byte A, byte B, byte C, and byte D. Note, however, that the bytes must be addressed as if part of a word, not as individual bytes. See "Addressing Digital Bits In A Word" in the *RPvdsEx Manual* for more information.

By default, all bits are configured as inputs. This default setting is intended to prevent damage to equipment that might be connected to the digital I/O lines. The user can configure the bits in the RPvdsEx configuration register. The configuration register is also used to determine what the eight front panel Bits lights represent.

To access the bit configuration register:

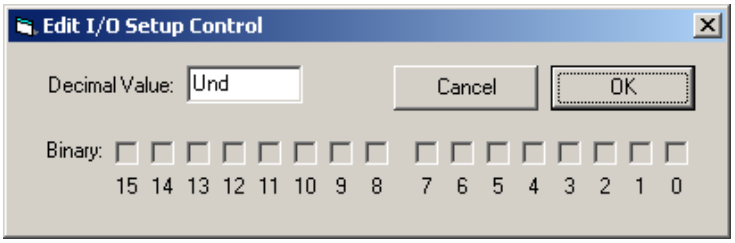
1. Click the **Device Setup** command on the **Implement** menu.
2. In the **Set Hardware Parameters** dialog box, click the **Device Type** box and select the **RX7 Elec-Stimulator** from the list.

   The dialog expands to display the **Device Configuration Register.**



3. Click **Modify** to display the **Edit I/O Setup Control** dialog box.

   In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.



4. To enable the check boxes, delete **Und** from the **Decimal Value** box.
5. To determine the desired value, select or clear the check boxes according to the table below. By default, all check boxes are cleared (value = 0). Selecting a check box sets the corresponding bit in the bitmask to one.
6. When the configuration is complete, click **OK** to return to the **Set Hardware Parameters** dialog box.

Bit #	Description
0-7	Each of these bits controls the configuration of one of the eight addressable bits as inputs or outputs. Setting the bit to one will configure that bit as an output.
8-11	Each of these bits controls the configuration of one of the four addressable bytes as inputs or outputs. Setting the bit to one will configure that byte as an output. bit 8 - byte A, bit 9 - byte B, bit 10 - byte C, and bit 11 - byte D
12-14	Create a bit code that determines how the front panel Bits lights are used, see table below.

Bit #	Description
15	Setting the bit to one will disable the D/A upsampler.

Bit Codes for Controlling the Bit Lights (Boxes 12-14)

By default, check boxes 12 –14 in the Edit I/O Setup Control dialog box (previous diagram) are cleared to create the bit code 000. This configures the eight front panel Bits lights to act as activity lights (glow when high) for the eight bit addressable digital I/O lines. The Bits lights can also be configured to provide information about amplifier status or act as activity lights for any of the other four bytes of digital I/O.

Bit Flags	Bits set to 1	Bit Lights Used For …
000 	None	Logical level lights for bit-addressable I/O lines
010 	13	Amplifier Clip Warning/Power Status display
100 	14	Enable logical level lights for byte A
101 	12, 14	Enable logical level lights for byte B
110 	13, 14	Enable logical level lights for byte C
111 	12, 13, 14	Enable logical level lights for byte D

XLink

The XLink is not supported at this time.

RX7 Technical Specifications

The RX7 is designed for use with the MS16 stimulus isolator. The RX7 is also equipped with a fiber optic input port for use with Medusa or Adjustable Gain preamplifiers.

Note: Specifications for the stimulus isolator D/As and the preamplifiers A/D are found under the technical specifications for those devices.

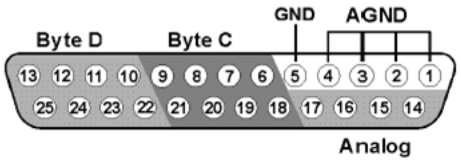
DSP	100 MHz Sharc ADSP 21161, 600 MFLOPS Peak Two or Five
Memory	128 MB SDRAM (Shared)
D/A	4 channels, 16-bit PCM
Sample Rate	Up to 97.65625 kHz (8X upsampled to 200 kHz default operation)*
Frequency Response	DC - Nyquist (~1/2 sample rate)
Voltage Out	+/- 10.0 Volts
Voltage Out Accuracy	+/- 10%
S/N (typical)	84 dB (20 Hz to 25 KHz) 82 dB with upsampling disabled
THD (typical)	-77 dB for 1 kHz output at 5 Vrms -74 dB with upsampling disabled
Output Impedance	10 Ohm
Fiber Optic Ports	One or Two Inputs, Output for Stimulator *
Digital I/O	40 bits programmable (8 bits bit-addressable and a 32 bit word, addressable as 4 bytes)

* **Note:** When used with the microstimulator, the sampling rate is limited to 24.414 kHz by the Stimulator Fiber Optic Port.

Note: zBus chasis (ZB1PS) required for power and communication.

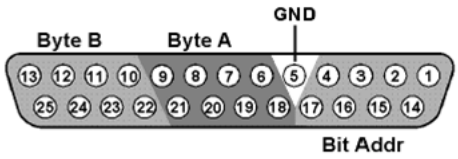
DB25 Connector Pinouts

Multi I/O



Pin	Name	Description	Pin	Name	Description
1	AGND	Analog Ground	14	A1	Analog Output Channels
2			15	A2	
3			16	A3	
4			17	A4	
5	GND	Digital I/O Ground	18	C0	Byte C Word addressable digital I/O Bits 0, 2, 4, and 6
6	C1	Byte C Word addressable digital I/O Bits 1, 3, 5, and 7	19	C2	
7	C3		20	C4	
8	C5		21	C6	
9	C7		22	D0	Byte D Word addressable digital I/O Bits 0, 2, 4, and 6
10	D1	Byte D Word addressable digital I/O Bits 1, 3, 5, and 7	23	D2	
11	D3		24	D4	
12	D5		25	D6	
13	D7				

Digital I/O



Pin	Name	Description	Pin	Name	Description
1	BA0	Bit Addressable digital I/O Bits 0, 2, 4, and 6	14	BA1	Bit Addressable digital I/O Bits 1, 3, 5, and 7
2	BA2		15	BA3	
3	BA4		16	BA5	
4	BA6		17	BA7	
5	GND	Digital I/O Ground	18	A0	Byte A Word addressable digital I/O Bits 0, 2, 4, and 6
6	A1	Byte A Word addressable digital I/O Bits 1, 3, 5, and 7	19	A2	
7	A3		20	A4	
8	A5		21	A6	
9	A7		22	B0	Byte B Word addressable digital I/O Bits 0, 2, 4, and 6
10	B1	Byte B Word addressable digital I/O Bits 1, 3, 5, and 7	23	B2	
11	B3		24	B4	
12	B5		25	B6	
13	B7				

Part 4: RP Processors

RP2.1 Real-Time Processor

RP2.1 Overview

The RP2 and RP2.1 real-time processors consist of an Analog Devices Sharc floating point DSP with surrounding analog and digital interface circuits to yield a powerful programmable signal-processing device capable of handling a variety of tasks.

Power and Communication

The RP2.1 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using any of the zBus PC interfaces. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

Features

Memory

The RP2 comes with 16MB of memory for data storage and retrieval. The RP2.1 has 32MB of memory for data storage and retrieval.

Digital Input/Output Bits

The digital I/O circuits include eight bits of digital input and eight bits of digital output that are accessed on the 25 pin connector on the front of the RP2. The

eight bits of I/O can be used within the processing chain in a variety of ways including implementing triggers, timing trigger responses, and lighting LEDs. The first four bits of the digital inputs and digital outputs as well as the Trigger/Enable input are mapped to LED indicators on the front panel of the RP2. There is an additional TRIG input BNC on the front panel.

D/A and A/D

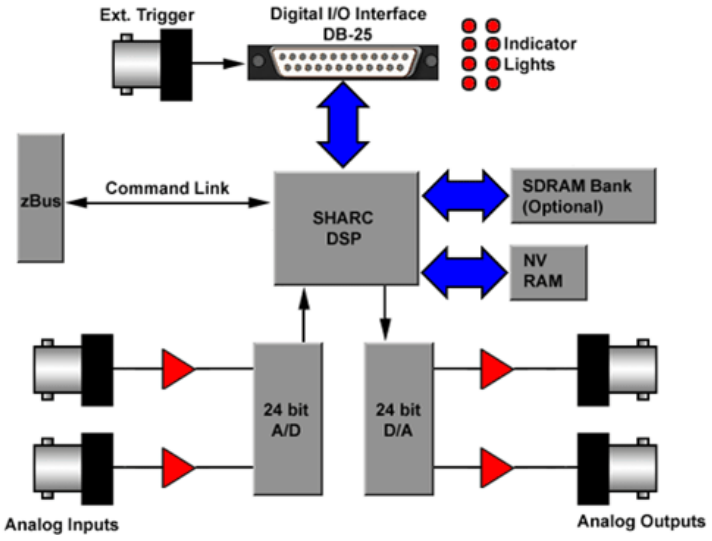
The RP2.1 is equipped with two channels of 24-bit, 200 kHz sigma-delta D/A and two channels of 24-bit, 200 kHz sigma-delta A/D. Sigma-Delta converters provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. See "RP2.1 Technical Specifications" on page 4-5, for the group delay of each device. The original RP2 A/D's run at 100 kHz. An Optional RP2-5 (identifiable by its version number only) is equipped with 24-bit 50 kHz A/D and 50 kHz D/A. The RP2-5 device does not have SDRAM.

Hardware

Up to 32MB of SDRAM can be installed for storage of long waveforms and acquired data. An RP2 comes standard with 16MB of SDRAM while an RP2-5 has no SDRAM. All of the RPvdsEx buffer components, used to build circuits for the RP2, utilize the SDRAM memory and therefore will not work when used on an RP2-5 device.

The RP2 communicates with and is programmed through the zBus link.

The RP2 hardware also contains a powerful digital I/O sub-system, offering eight bits of digital input and eight bits of digital output as well as a dedicated trigger input connected to a BNC on the front panel. The first four bits of both input and output port and the trigger input have LED monitors for a quick indicator of bit state. The bits of these ports can be programmed individually or as a 'digital word' and used in a variety of ways within the RP2 processing circuit.



The RP2 is interfaced to the analog world via a two channel 24-bit analog to digital converter and a two channel 24-bit digital to analog converter. The RP2 system's I/O buffer handles +/- 10 Volt signals with excellent signal to noise performance. The RP2 contains a 100 kHz (50 kHz BW) A/D and a 200 kHz (100 kHz BW) D/

A, while the RP2-5 has a 50 kHz (25 kHz BW) A/D and D/A. Both devices allow for user programmable sampling rates from the specified maximum down to 6.25 kHz. A special calibration program is used to calibrate the RP2's analog I/O offering very small gain and DC offset errors.

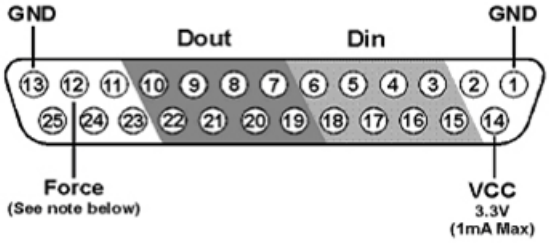
RP2.1 Technical Specifications

This table also includes specification for the RP2 and RP2-5.

DSP	50 MHz Sharc 21065, 150 MFLOPS
Memory	RP2: 16 MB SDRAM RP2.1: 32 MB SDRAM RP2-5 has no SDRAM
A/D	2 channels, 24-bit sigma-delta
Frequency Response	DC - 0.84 * Nyquist (1/2 sample rate) RP2.1: DC - 82 kHz maximum RP2: DC - 41 kHz maximum RP2-5: DC - 21 kHz maximum
S/N (typical)	105 dB (20 Hz to 20 KHz), 95 dB (20 Hz to 50 KHz)
Distortion (typical)	-95 dB for 1 KHz input at 5 Vrms
A/D Sample Rate	RP2.1: 195.312 kHz maximum RP2: 97.656 kHz maximum RP2-5: 48.828 kHz maximum
Sample Delay	RP2.1: 65 samples RP2: 41 samples
D/A	2 channels, 24-bit sigma-delta
Frequency Response	DC - 0.84 * Nyquist (1/2 sample rate) RP2.1: DC - 82 kHz maximum RP2: DC - 41 kHz maximum RP2-5: DC - 21 kHz maximum
S/N (typical)	105 dB (20 Hz to 20 KHz), 95 dB (20 Hz to 50 KHz)
Distortion (typical)	-95 dB for 1 KHz output at 5 Vrms
D/A Sample Rate	RP2.1: 195.312 kHz maximum RP2: 97.656 kHz maximum RP2-5: 48.828 kHz maximum
Sample Delay	RP2.1: 30 samples RP2: 30 samples
Output Current	RP2.1: 175 mA maximum
Digital Inputs	8 bits + 1 TRIG input

Digital Outputs	8 bits
System Reset	Force input (see the section below on how to reset)
Input Impedance	10 kOhm
Output Impedance	10 Ohm

DB25 Connector Pin Out



Pin	Name	Description		Pin	Name	Description
1	GND	Ground		13	GND	Ground
2	NA	Not Used		14	VCC	3.3V (1A Max)
3	DI1	Digital Input Bits		15	DI0	Digital Input Bits
4	DI3			16	DI2	
5	DI5			17	DI4	
6	DI7			18	DI6	
7	DO1	Digital Output Bits		19	DO0	Digital Output Bits
8	DO3			20	DO2	
9	DO5			21	DO4	
10	DO7			22	DO6	
11	NA	Not Used		23	NA	Not Used
12	Force	Used to reset the RP2.1		24		
				25		

Note: TDT recommends the PP16 Patch Panel for accessing digital I/O.

Important!: **Force** is used to reset the RP2.1, including deleting the device's microcode. It has no function in data acquisition or manipulation.

To reset the device:

1. Connect a wire (or paper clip) from pin 12 to pin 13 on the Digital I/O port.
2. With pins 12 and 13 shorted, use the desktop shortcut to run **zBUSmon**.
3. In the zBUSmon utility window, hold down the shift key and right-click the device in the system diagram.
4. Click **Program RP2.1** on the shortcut menu.
5. In the System3 Device Programmer window, select the device type (RP2).
6. Next click the Browse button next to the *uCode File* field and select **RP21.dxe**.

7. Remove the short from pins 12 and 13, and click the **Program Device!** button.

   Do not use your computer until the device reprogramming is complete (approximately five minutes).

RA16BA Medusa Base Station

RA16BA Overview

Recommended for single or dual channel extracellular recordings and low channel count EEG's, EMG's and evoked potential recordings (such as ABRs), the Medusa Base Station is a versatile signal processor designed to acquire, filter, and process data digitized on one of our preamplifiers. The RA16 acquires digitized signals from a Medusa preamplifier over a fiber optic cable, providing loss-less signal acquisition between the amplifier and the base station.

PCM analog outputs can be used for a wide variety of signal production tasks, including control of motors, electrical stimulation, and monitoring analog signals during acquisition.

Power and Communication

The RA16 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using any of the zBus PC interfaces. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RA16BA Features

Status Lights

The four lights on the left-hand side are status lights that relate to the amplifier.

Active — The active light blinks when there is no active connection between the base station and the amplifier. The active light is

	on when there is a connection to an amplifier and the amplifier is on.
Error	The error light blinks when there is a communication error between the base station and the amplifier.
Clip	The clip light is a warning light and flashes when any channel on the connected amplifier produces a voltage approaching the maximum input of the amplifier. The light will flash rapidly to warn that clipping may occur if the signal exceeds the maximum input voltage.
Battery	The battery light flashes when the battery voltage is low. The Li-Ion battery voltage decreases rapidly once this indicator light is on. Data acquisition will suffer if the battery is not charged soon after this warning.

Digital Out Lights

There is one digital out LED for each digital output bit. Each LED will light when a logical high (1) is sent out on the corresponding digital output bit. The digital out lights can be used to indicate clipping or spike detection on a channel.

Trigger

Allows input of an external digital trigger.

Link and Amplifier Ports

The Base Station has two sets of fiber optic ports. The Link port outputs the signals that are input to the amplifier port. This allows multiple base stations to be linked for complex or high channel count processing. The Amplifier port is used to connect the base station to a Medusa preamplifier for the acquisition of analog signals.

Stereo Output

The stereo output samples from the first two channels of the digital-to-analog converters (DACs) so that users can monitor signal properties with headphones or speakers. The left speaker monitors channel one of the DAC and the right speaker monitors channel two.

Use the Ch (channel) parameter on the channel inputs to change which analog channels are being monitored.

Analog and Digital Outputs

Each base station comes with 16 digital output bits and eight analog output channels. See “RA16 Technical Specifications” on page 4-11, for DB25 pinout. Each DAC uses 18-bit sigma-delta parts for high quality signal conversion. Sigma-delta converters provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. For the RA16BA the DAC Delay is 18 samples.

Sampling Rate Considerations

There are no onboard analog-to-digital converters (ADCs) on the Medusa base station. When acquiring data, a preamplifier does this conversion. Since the fiber optic connection from a preamplifier to the base station has a transfer rate limitation of ~25 kHz, circuits utilizing this data acquisition must use a sample rate of ~25 kHz or less. Otherwise (i.e. circuits with digital-to-analog conversion only), the maximum sample rate is ~50 kHz.

Force

Pushing a paper clip in to the pinhole next to the clip light deletes the microcode on the base station. Once the microcode is deleted the RA16 base station will need to be reprogrammed.

USB Transfer Rates

USB transfers are limited to 100,000 samples per second of 32-bit data. 16-channels of ~25 KHz data produce 400,000 samples of data per second. Data reduction techniques such as Compress to 16 and Shuffle to 16 will reduce the data size without significant loss of information. Selective channel analysis and filtering can further reduce the amount of data transferred.

Memory

The RA16BA Medusa comes standard with 32MB of RAM. At 16-channels in 16-bit mode, 32MB would give around 40 seconds of continuous data acquisition. Each additional base station could add an additional 2.5 minutes of continuous data acquisition.

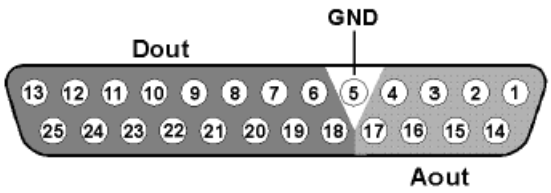
RA16 Technical Specifications

Note: The RA16BA has no onboard AD converters. Technical specifications for the AD converters are found under the preamplifier's technical specifications.

DSP	50 MHz Sharc 21065, 150 MFLOPS
Memory	16 MB SDRAM or 32 MB SDRAM
D/A	8 channels, 18-bit sigma-delta
Sample Rate	48.828 kHz maximum
Frequency Response	3 dB at 3 Hz - Nyquist (~1/2 sample rate)
Voltage Out	+/- 10.0 V (AC coupled)
S/N (typical)	90 dB (20 Hz to 25 KHz)
Distortion (typical)	-70 dB for 1 KHz output at 0.7 Vrms
Sample Delay	18 samples

Fiber Optic Ports	1 16-channel Input and 1 Link Port (24 kHz maximum sample rate)
Digital Inputs	1 bit
Digital Outputs	16 bits
Input Impedance	NA
Output Impedance	20 Ohm

DB25 Analog/Digital I/O Connector Pin Out



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channels		14	A2	Analog Output Channels
2	A3			15	A4	
3	A5			16	A6	
4	A7			17	A8	
5	GND	Ground		18	D0	Digital Output Bits
6	D1	Digital Output Bits		19	D2	
7	D3			20	D4	
8	D5			21	D6	
9	D7			22	D8	
10	D9			23	D10	
11	D11			24	D12	
12	D13			25	D14	
13	D15					

Note: TDT recommends the PP16 patch panel for accessing the Digital I/O.

RV8 Barracuda Processor

Note: This device is no longer available for new purchase.

RV8 Overview

The Barracuda features include nanosecond accurate event-timing, fast DAC's for high frequency stimulus presentation and user control of sample frequencies. In addition the Barracuda gives users precise control over stimulus presentation. The system has 16-digital inputs, 8-digital outputs, and 8 analog outputs.

Power and Communication

The RA16 mounts in a System 3 zBus Powered Device Chassis (ZB1PS) and communicates with the PC using any of the zBus PC interfaces. The ZB1PS is UL compliant, see the *ZB1PS Operations Manual* for power and safety information.

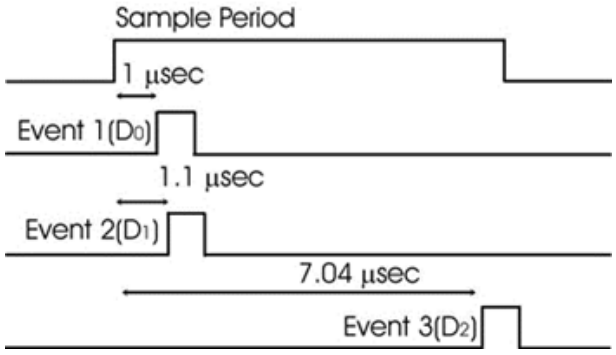
Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

Nanosecond Event-Timing

The Barracuda is a nanosecond accurate event timer. The TimeStamp component uses the high-speed clock on the system to record when a TTL event occurred during a sampling period. This means that event times are independent of sample rate. When an event occurs the TimeStamp sends out the time in microseconds from the start of that sample period. At the end of each sample period the event timer is reset to zero. In the figure below three events occurred during a sample period of

ten microseconds. For each digital input a unique time stamp is recorded for that sample period.



TimeStamp Diagram

Fast Digital-Analog Converters

The Barracuda ships with PCM DAC's with up to 500 kHz sample rate. The fast DAC's can be used for high frequency presentations. In addition the Barracuda's PCM DAC's give users precise control over voltage outputs for microelectrode stimulation.

Variable Sample Frequency

The Barracuda allows users to set the sample period in 40 nanosecond steps. Users can select sample frequency from 10 to 500,000 Hz.

User Control of System Devices

The Barracuda has two control modes: Free-run and Triggered. In Free-run mode the circuit runs continuously and gating functions are required to control the signal outputs and inputs. In Trigger mode the circuit only runs after it has been triggered. It then runs for a set number of samples and then stops. The system can be triggered once or multiple times. The circuit must be reset before it can trigger again. Gating functions are not required for turning on and off stimuli.

Additional Features

To simplify signal synchronization it is possible to send out the sample clock and the system clock (50 MHz) on the digital outputs. Users can also send out the sample clock period.

Barracuda Features

Trigger

Takes an external TTL pulse and triggers components (free run mode) or triggers the circuit (trigger mode).

Status Lights

The status lights indicate the state of the RV8. Armed, Running, DC (DoCount), and FreeRun. Combinations of the status light describe the state of the RV8.

Free Run Mode	Free Run Mode w/ Circuit Running	Trigger Mode	Trigger Mode with System Armed	Trigger Mode with System Running:
				

Digital Input Lights

Lights are on when there is a TTL pulse on the digital input line. Pulse times may be too brief to see in many cases. Only channels 0-7 have indicator lights.

Digital Output Lights

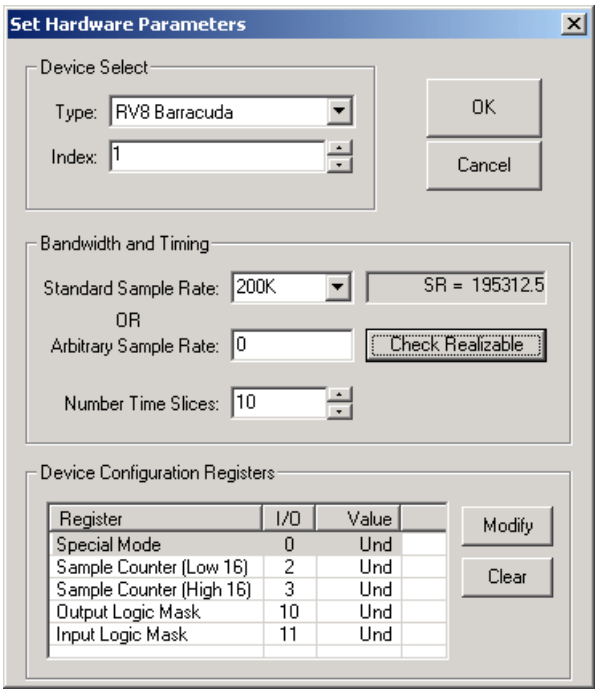
Lights are on when a TTL pulse is sent out of a digital output line. All eight channels (0-7) have a TTL indicator light.

25-pin Connector for Digital Inputs and Outputs

A 25-pin connector gives access to all 24 channels of digital I/O. The pin outs for the connector are shown in "Barracuda Technical Specifications" on page 4-21. TDT provides the PP16 with 24 connectors to give users easy access to all the digital output channels of the Barracuda.

Barracuda Device Setup

The Barracuda has several additional features not found in other RP devices. An expanded dialog box opens after selecting the RV8 option.



Bandwidth and Timing

Standard Sample Rates are in powers of two from 6 kHz to 400 kHz. The actual sample rate is given in the box to the right.

Arbitrary Sample Rate can be from 10 Hz to 500,000 Hz. In the Arbitrary Sample Rate box type a number between 10 Hz and 500,000 Hz. To reset to the Standard Sample Rates type 0 in the Arbitrary Sample Rate box. To determine the true sample rate click **Check Realizable**. The sample rate is based on the system clock (25 MHz) or a sample period of 40 nanoseconds (40 * 10-09). To calculate the true sample rate, take the reciprocal of the required sample period in seconds.

Device Configuration Parameters

The device configuration parameters allow RPvdsEx access to unique features on the RV8. To access a particular parameter either double-click on the parameter name or click on the parameter and click the Modify button. To reset the parameter value to the default mode click Clear.

Special Mode

The Special Mode is a bit-masked value that determines which features of the Barracuda are activated. The default mode for the Special Mode is zero. This makes the system behave like other RP devices. There are seven modes that are accessed through the bit-mask shown below. Special Mode can be accessed with the ActiveX controls SetDevCfg and GetDevCfg.

Bit Number	Enabled Value	Name	Function
0	1	DoCount	Sets up system to run under trigger mode.
1	2	AutoClr	Clears the DAC out buffers after a trigger event.
2	4	TickOut	Sends a pulse at the beginning of each tick period on Digital Out 7. Pulse length is 40 nanoseconds.
3	8	ClkOut	Sends pulses at 1/2 the clock frequency (25 MHz).
4	16	UseZTRGA	Starts the Barracuda when a ZtrgA goes high. Only works in the trigger mode (must also have bit-number 1 enabled).
5	32	UseZTRGB	Starts the Barracuda when a ZtrgB goes high. Only works in the trigger mode (must also have bit-number 0 enabled).
6	64	UseEXTR	Starts the Barracuda using the external trigger. Only works in the trigger mode (must also have bit-number 0 enabled).
7	128	MTRIG	Enables multiple trigger mode. Users can repeatedly trigger the Barracuda without stopping and rerunning the circuit. 0=Very Large Number of Triggers

The Special Modes are set with a bit-masked pattern. For example, to set the trigger mode using a zTRGA the value for the Special Mode would be set to 1 + 16 or "17". To use the Mtrig function the value would be 1 (DoCount) + 16 (UseZTRGA) + 128 (MTRIG) or "145".

DoCount

Enable DoCount to use the trigger mode. If this is not enabled then the device is in free-run mode.

AutoClr

AutoClr works in trigger mode. AutoClr clears the output of the DAC's to zero after the last value is played. Otherwise the output of the DAC is set to the last value converted.

Trigger Mode

In trigger mode the circuit only runs after it has been triggered. After a trigger it runs for set number of samples and then stops.

Using the trigger mode requires three steps:

1. Set the value of the Special Mode parameter.

   This value is a bit-masked value. To calculate the value needed sum the individual bit-masks (see above). The bit-masks include DoCount (1) the trigger mode (16, 32 or 64 depending on what trigger option) and possibly enabling MTRIG (128).

2. Determine the number of samples that the circuit runs. The Barracuda can play out over 4 Gsamples (4*109 samples) on one trigger. Sample Counter (Low 16) sets the sample number between 0 and 65535 Sample Counter (High 16) sets it between 65536 and a large number. For example, to play out 80000 samples the Sample Counter (High 16) would be set to 1 (65,536) and Sample Counter (Low 16) to 14,464.
3. Load and trigger the circuit.

Sample Count Options

Sample count parameters set the number of samples the circuit will run. The Sample Counter (Low 16) values are between 0 and 65536 (lower 16-bits of data). Sample Counter (High 16) values are multiples of 65536. For example, a value of 2 in Sample Counter (High 16) will cause the circuit to run for 131,072 samples. If the system needed to run for 200,000 samples you would set Sample Counter (High 16) = 3 (196,608 samples) and Sample Counter (Low 16) = 3,392.

Sample count is only used when in trigger mode. At all other times the circuit is free running.

Sample Counter (Low 16) = the lower 16bits of the sample counter (0-65535)

Sample Counter (High 16) = the upper 16bits of the counter. A value of 1 in Sample Counter (High 16) = 65536.

Logic

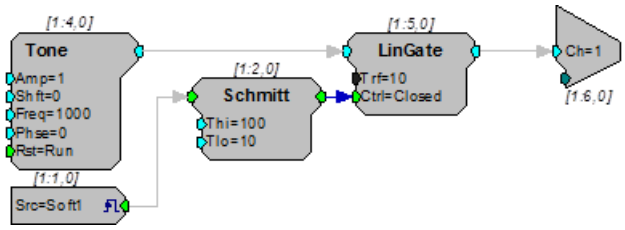
User selects whether a high voltage on a digital line is a logical 1 or logical 0 on the Barracuda.

The default state for a high voltage on a digital line is 1 (high true). Setting InLogic = 1 inverts the logic (low true) and makes a high input voltage produce a 0 and a low input voltage produce a 1. Similarly, when setting OutLogic = 1, a high voltage on a digital output line will produce a 0 and a low voltage will produce a 1.

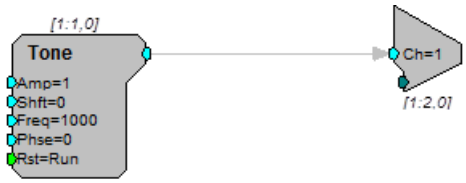
Software Control

The Barracuda has two modes: free-run and trigger. In free-run mode the circuit is always running and signals are constantly generated, acquired, and filtered. In the trigger mode the circuit runs for a set length each time it is triggered. The advantage of the trigger mode is that some circuit design is simplified. The example below shows two circuits that present a tone burst of 100 milliseconds. The first circuit works under the free-run mode and the second with trigger.

Free-Run Mode



Trigger Mode



The first circuit requires three additional components: LinGate gates the output on and off, Schmitt opens and closes the gate and Src (Soft1) starts the Schmitt trigger. The second circuit requires that the Barracuda be controlled from the trigger mode. Trigger mode is accessible within RPvdsEx or from the ActiveX controls.

TimeStamp

The TimeStamp component is unique to the Barracuda and Multifunction Processor (RX6). The event-timer, with its submicrosecond accuracy, is independent of the sample period. This allows users to have separate control of both slow processes, such as button presses, and fast events, such as neural activity, all on one circuit with little or no loss of processing power.

PCM DAC Outs

The PCM DACs have a sample delay of only 2 samples. This makes them ideal for use with time critical presentation of signals. These DACs are excellent for neurophysiological stimulation for examining motor behavior.

Multiple Triggering

Multiple triggers allow users to repeatedly trigger the Barracuda without resetting (Halting and then Running the chain). To use multiple triggering with RPvdsEx add the bit-masked value of 128 to the Special Mode value. For example, to configure the Barracuda for multiple triggering from the zBUSTrigA, you would set the value to 1 (Trigger Enabled) + 16 (ZbusTRIGA) + 128 (multiple triggers). RPvdsEx has no way to control the number of presentations.

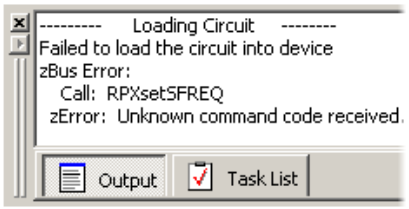
To generate an RPvdsEx circuit for multiple triggering, use the Setup Device command on the Implement menu to open the Set Hardware Parameters dialog box, then modify the Special Mode register. Use the bit-masked values for the Special Mode to make a circuit trigger off either the zBUS or external trigger. In general this will be 1(trigger mode enabled) + (trigger type) + 128 (mTrig enabled).

The multiple trigger does not require the addition of the trigger component. The circuit runs when the trigger pulses high. The RPvdsEx circuit will trigger for a near infinite number of times before stopping.

Arbitrary Sample Rates

The Barracuda is the only System 3 module that has arbitrary sample rates. To set the arbitrary sample, click **Device Setup** on the **Implement** menu, and then set the sample rate in the Arbitrary Sample Rate box. To check the true sample rate, click **Check Realizable**. This will display the true sample rate. Sample periods are in increments of 40 nanoseconds. To calculate the true sample rate determine the

sample period in seconds that you require and then divide by 1/(sample period). These circuits work only with the Barracuda. If the circuit is run on a different RP module it will give the following error:

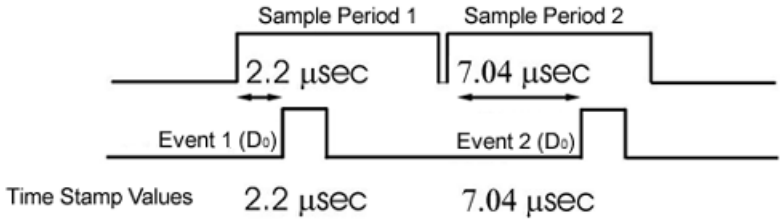


RP Control Object files (RCO) will produce similar problems. If you attempt to run an RCO file (compiled RPvdsEx files for use with ActiveX controls and turn-key software programs) that has an arbitrary sample rate on another RP device the same error will occur.

Using the TimeStamp Component

The TimeStamp component is an event timer with submicrosecond accuracy. With other RP systems the resolution of the TimeStamp is no better than the sample clock period. TimeStamp uses the system clock to determine when, within a sample period, the event occurred. After each sample period the TimeStamp component is reset.

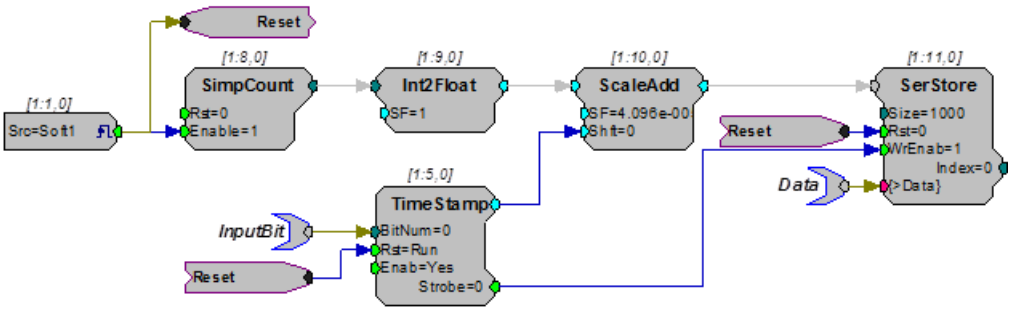
The diagram below shows how TimeStamp works. The first event occurs 2.2 microseconds after the start of the first sample period so a value of 2.2 is generated. The second event occurs 7.04 microseconds after the start of the second sample period so a value of 7.04 is generated.



TimeStamp Diagram

The circuit below saves the event time (in microseconds) to a SerStore buffer. The circuit has two parameter tags: *InputBit* and *data*. The InputBit tag sends the digital input channel number (to which the Event trigger will be sent) to the TimeStamp. This determines which of the Barracuda's digital input lines will be monitored for triggers. The *data* tag reads the stored event-time data to a PC buffer.

A software trigger resets the SimpCount, starting the clock, and will also reset the TimeStamp component and the SerStore buffer. The SimpCount increments the count value at every sample tick. The ScaleAdd divides the SimpCount output by the sample period (40.96 microseconds) to keep track of the time in milliseconds. When an event is detected, the TimeStamp output is added to the SimpCount output to get the event time in microseconds.



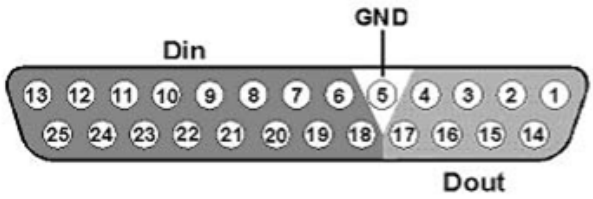
ActiveX

The Barracuda uses two additional ActiveX methods SetDevCfg and GetDevCfg. Detailed information about them is included in the ActiveX help.

Barracuda Technical Specifications

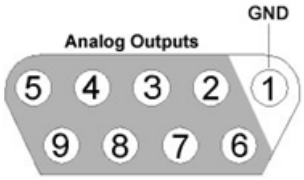
DSP	50 MHz Sharc 21065, 150 MFLOPS
Memory	32MB SDRAM
Digital Inputs	16 bits + 1 TRIG input
Digital Outputs	8 bits
Analog Outputs	8 Channels
Input Impedance	10 kOhm
Output Impedance	10 Ohm

DB25 Connector Pin Out



Pin	Name	Description		Pin	Name	Description
1	Do0	Digital Output Channels		14	Do1	Digital Output Channels
2	Do2			15	Do3	
3	Do4			16	Do5	
4	Do6			17	Do7	
5	GND	Ground		18	Di0	Digital Input Channels
6	Di1	Digital Input Channels		19	Di2	
7	Di3			20	Di4	
8	Di5			21	Di6	
9	Di7			22	Di8	
10	Di9			23	Di10	
11	Di11			24	Di12	
12	Di13			25	Di14	
13	Di15					

Option I/O DB9 Connector Pin Out



Pin	Name	Description
1	AGND	Analog Ground
2	A1	Analog Channels
3	A2	
4	A3	
5	A4	
6	A5	
7	A6	
8	A7	
9	A8	

Part 5: RM Mobile Processors

RM1/RM2 Mobile Processors

RM1 Mobile Processor (RM2 not pictured)

RM1/RM2 Overview

The System 3 platform includes two self-contained real-time processors: the Mini Processor and the Mobile Processor. Designed as an affordable test-bed system for designing and debugging RPvdsEx circuits, each device includes stereo A/D and D/A, an adjustable onboard speaker, and can drive headphones at up to 100 dB SPL. The devices draw power from the USB interface of the computer and work well with laptop computers for maximum portability. These economical mobile systems can also be used for basic psychoacoustics.

For detailed information on each member of the RM family check the technical specifications of the module.

Power Requirements

Power is provided across the USB connection to a host PC. The RM draws approximately 300 mAmps from a 6 Volt input. The draw on a portable PC battery will depend on the power requirements of the portable PC and the properties of the battery. In many cases, the user may see less than 10% decrease of the battery life.

Users can attach an external power supply such as an AC adapter (available on request) or an external pack such as a motorcycle battery (input range of 6-9 Volts).

Software Control

Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx). Circuits are loaded to the processor through TDT run-time applications or custom applications. This manual includes device specific information needed during circuit design. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see the *RPvdsEx Manual*.

RM1/RM2 Processor Hardware

The RM1 Real-time Mini Processor and RM2 Mobile Processor combine a signal processor, a power supply, and a computer interface in one small form factor. The RM consists of an Analog Devices Sharc floating point DSP with surrounding analog and digital interface circuits and 32 MB of memory for data storage and retrieval. The RM2 also includes a fiber optic connection for the RA4/RA16PA Medusa amplifier.

D/A and A/D

The RM is equipped with stereo 24-bit sigma-delta A/D and D/A that can sample at rates up to 97.656 kHz. Sigma-delta converters provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. For the RM1 and RM2, the DAC Delay is 17 samples and the ADC Delay is 16 samples.

Digital Input/Output Bits

The TTL I/O circuits include four bits of digital input and four bits of digital output that are accessed via the 9-pin connector on the back of the RM. Bit0 can also be accessed through a BNC connector on the front panel. The RM's digital I/O can be used to implement triggers, time trigger responses, and light LEDs.

Analog Output

The RM is equipped with an external speaker for use when previewing stimulus during the circuit design process. The RM's stereo analog output can drive a headphone at up to 100 dB SPL.

USB Input Port

An USB Input port allows multiple devices to be connected for increased processing power.

Mobile Processor Front Panel Features

Bit0

The BNC connector for Bit0 allows for a direct input or output to the first bit of the RM device. This allows for a more convenient connection for a typical trigger input. Access to the other digital inputs and outputs are from a 9-pin connector on the back panel.

Status Lights

The status lights indicate the state of the RM.

Power

The power light indicates that the device is connected to a power supply. The power may be supplied by an external power supply or by a computer (powered on) via the USB interface.

Comm (Communication)

The communication light blinks when the device is sending or receiving information to or from the PC. (This requires the system to be connected to a PC.)

Err (Error) or Amp (RM2)

The error light indicates one of the following:

An error communicating with the host PC.

An error communicating with the RA4/RA16PA (RM2 Only)

Status

The status light blinks when a circuit is running. The rate at which the light blinks is a general indicator of cycle usage, with faster blinking indicating a higher cycle usage.

Bits Lights

Bit lights indicate when a bit input is set high. The LED(s) will light if the input signal is set high or if the output bit is set high. Voltage high is 3.3 volts and voltage low is nominal 0 Volts. Access to the digital I/O port is through a 9-pin connector on the back panel. The bit inputs are set logical high by default.

Analog I/O

The analog inputs and outputs use a 3.5 mm stereo plug and deliver or accept a +/- 1 Volt signal with a dynamic range of over 45 dB. The RM uses 24-bit Sigma-delta A/D and D/A converters.

In

The maximum analog input is +/- 1 Volt with a peak sample rate of 97.656 kHz. The input impedance is 10 kOhm. The analog inputs are AC-coupled; the RM cannot receive DC or very low frequency (<1 Hz) signals.

Out

The maximum analog output is +/- 1 volt with a peak sample rate of 97.656 kHz. The low-level output impedance (10 Ohm) of the system allows users to drive earphones at up to 100 dB SPL. The analog outputs are AC-coupled; the RM cannot play out DC or very low frequency (<1 Hz) signals.

Level

The RM has an internal speaker that is driven by channel 1 output. The Level knob controls the volume of the speaker and analog channels 1 and 2 when connected to the 1/8" audio jack labeled OUT. To achieve the full output level specified in your circuit on these two channels, set the Level knob to Max.

RM1/RM2 Processor Back Panel Features

USB In

The USB input on the RM acts as a USB hub. Multiple RM devices can be ganged together to increase signal processor power. A standard USB, A to B, cable is required for setup.

USB Out

The USB output connects either to another RM device, a UB4, or to the host computer's USB interface. The RM can be connected to PCs with either USB 1.1 or USB 2.0 hubs.

Digital I/O

The female DB-9 connector allows direct access to the digital inputs and outputs. Pinout information is provided on the label above the connector. Bits 0 - 3 (which map to pins 5, 9, 4, and 8 on the male DB-9 connector) are inputs and bits 4 - 7 (which map to pins 3, 7, 2, and 6 on the male DB-9 connector) are outputs. Ground is labeled G (which maps to pin 1 on the male DB-9 connector).

Note: The digital lines drive about 25 milliamps.

Amplifier (RM2 only)

A fiber optic connector is found on the RM2 for use with the Medusa RA4/RA16 preamplifier, the Loggerhead RA8GA, and the associated headstage assemblies.

Ext. Pow. (External Power)

An external power supply can be used as an alternative to drawing power from the USB connection. An adapter allowing the device to be powered form an AC power source is available upon request. A battery with an output range of 6-9 volts, such as a motorcycle battery, could also be used to power the device.

TDT recommends separate external power sources when using multiple RM devices.

Mobile Processors Digital Input/Output

The Mobile Processors are equipped with 8 bits of programmable digital input/output, accessed via the Digital I/O 9 pin connector on the back panel. See "RM1/RM2 Processor Technical Specifications" on page 5-9, for a pinout diagram.

Note: The digital lines drive about 25 milliamps.

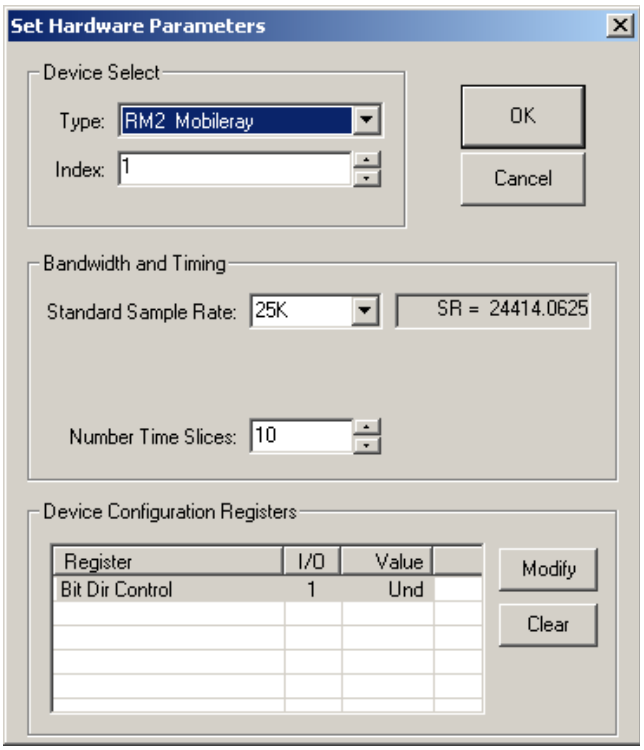
Configuring the Programmable I/O Lines

All 8 digital lines are independently configurable as inputs or outputs. By default, bits 0-3 are configured as inputs and bits 4-7 are configured as outputs. In RPvdsEx, bits 0-7 in the bit configuration register control the configuration of the eight addressable bits as inputs or outputs. Setting a bit to one will configure that bit as an output.

To access the bit configuration register:

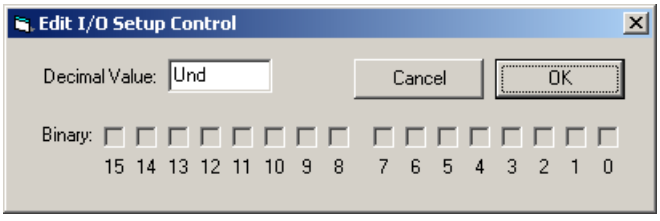
1. Click the **Device Setup** command on the **Implement** menu.
2. In the **Set Hardware Parameters** dialog box, click the **Type** drop-down box and select **RM1** or **RM2** from the list.

   The dialog expands to display the **Device Configuration**.



3. Click **Modify** to display the **Edit Bit Dir Control** dialog box.

   In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.



4. To enable the check boxes, delete **Und** from the **Decimal Value** box.
5. To determine the desired value, select or clear the check boxes. By default, all check boxes are cleared (value = 0). Click the check boxes for desired bits (0 -7) to set the bit to one and configure that bit as an output.

Note: Modifying any of the bits will change the default configuration (by default, bits 0-3 are inputs and bits 4-7 are outputs).

6. When the configuration is complete, click **OK** to return to the **Set Hardware Parameters** dialog box.

Using the RM2 Fiber Optic Port

The RM2 Fiber Optic Port can be used with a Medusa or Loggerhead preamplifier; however, it is unlikely that a single RM2 device can acquire 16 channels of high frequency activity. Instead we recommend that the RM2 be used for low channel count (up to four channels) high sample rate acquisition or for high channel count low sample rate activity (e.g. 16 channels of slow EEG activity). Using the RM2 as part of a Medusa/Loggerhead system effectively provides two channels of high quality A/D inputs and up to 16 channels of signal input running at 25 kHz. The signal input lines accessed via the analog I/O and fiber optic port are mapped as described below to allow for simultaneous use of the high quality A/D and the amplifier input channels.

	RM2 Channel		RM2 Channel
Analog I/O Input Channel 1	Channel 1	Amp Channel 8	Channel 24
Analog I/O Input Channel 2	Channel 2	Amp Channel 9	Channel 25
Amp Channel 1	Channel 17	Amp Channel 10	Channel 26
Amp Channel 2	Channel 18	Amp Channel 11	Channel 27
Amp Channel 3	Channel 19	Amp Channel 12	Channel 28
Amp Channel 4	Channel 20	Amp Channel 13	Channel 29
Amp Channel 5	Channel 21	Amp Channel 14	Channel 30
Amp Channel 6	Channel 22	Amp Channel 15	Channel 31
Amp Channel 7	Channel 23	Amp Channel 16	Channel 32

For more information about the Medusa, see the "RA16PA/RA4PA Medusa PreAmps" on page 7-87.

Software Control for the Mobile Processor

In general, the RM processors can use any circuit that has been designed for the RP2.1. There are a few caveats that relate to the number of digital inputs and outputs, the positioning of the input channels from the fiber optics on the RM2, and the maximum signal voltage.

Digital I/O

The RM has only eight digital I/O channels. Circuits that use more than four TTL outs or four TTL ins will not work with the RM.

RM2 Acquisition Channel Input

The channels from the preamplifier to the RM2 are mapped so that the system can acquire from both the high quality analog inputs and the preamplifier. For acquisition channels across the fiber optic connection, channel numbers are offset by 16. Channel one from the preamp maps to channel 16 of the RM2, channel two maps to 17, and so forth. Users must modify existing circuit designs and OpenEx files by setting an offset value to match the channel organization of the RM2.

There is no fiber optic repeater to allow multiple RM2s to be linked for data acquisition from a single preamplifier. All acquisition from the preamplifier must take place on a single RM2.

Signal Voltage

The maximum signal voltage for acquisition and presentation is +/- 1 volt. Circuits that have components generating signals greater than +/- 1 volt will cause the device to clip either on input or output.

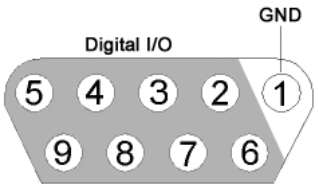
RM1/RM2 Processor Technical Specifications

DSP	50 MHz Sharc 21065, 150 MFLOPS
Memory	32 MB
A/D	2 channels 24-bit sigma-delta A/D
S/N (typical)	85 dB (20 Hz to 20 kHz)
Distortion (typical)	80 dB for 1 kHz input at 630 mV rms
Sample Delay	16 samples
Highpass Filter	1 Hz
D/A	2 channels 24-bit sigma-delta D/A
S/N (typical)	85 dB (20 Hz to 20 kHz)
Distortion (typical)	80 dB for 1 kHz input at 630 mV rms
Sample Delay	17 samples
Highpass Filter	1 Hz
Digital I/O	8 user selectable
System Reset	Front panel next to ERR light
Input Impedance	10 kOhm
Output Impedance	10 Ohm

RM2 Fiber Optic Inputs

Input	up to 16 channels
Sampling Rate	24.414 kHz max

Digital I/O DB9 Female Connector Pin Out



Pin	Name	Description
1	GND	Ground
2	D6	Digital Input/Output Channels
3	D4	
4	D2	
5	D0	
6	D7	
7	D5	
8	D3	
9	D1	

Part 6: Subject Interface

~

SIM Subject Interface Module

SIM Device Overview

The Subject Interface Module (SIM) is a multi-modal stimulator and neurodigitizer suitable for recording a broad range of biological potentials. Multiple banks of high-fidelity stimulation can be combined with the same high-fidelity analog and digital input boards used in the PZ5 amplifier.

The SIM supports up to eight banks that can be configured with stimulation, analog acquisition, or digital headstage acquisition boards.

It connects to a DSP-M card in any RZ processor and is controlled by TDT's Synapse software.

The IZV stimulator boards converts digital waveforms into analog waveforms as part of a computer-controlled neural microstimulator system that delivers user-defined stimuli through up to 128 electrodes. The IZV can output either a voltage-controlled waveform or a current-controlled waveform and provides feedback of the actual voltages delivered to the electrodes.

Each stimulation board has four 'voices' that can supply up to 5mA per channel with 10nA resolution and +/-15V compliance. Voices can be programmatically connected to the same stimulation channel to increase output current to up to 20mA on a single channel per board. Stimulation boards can be harnessed together to increase compliance voltage beyond the +/-15V range for high voltage, single-channel stimulation.

The SIM analog boards can record high and low impedance input signals simultaneously. Analog input boards oversample the signal with very fast instrumentation grade converters. TDT's custom hybrid A/D circuit yields 28 bits of resolution and unparalleled dynamic range. Optional DC coupling offers zero phase distortion across the signal bandwidth. Sampling rate and down-sampling filters can be optimized on each logical amplifier for the intended input type to optimize signal fidelity. The +/-500 mV input range is large enough to accept any biological potential and most stimulus artifacts without saturating.

The analog input and stimulator outputs are organized into 16-channel boards. Each bank is electrically isolated, meaning the ground and reference channels are not inherently shared between banks. Multiple banks can be grouped into a single logical amplifier/stimulator that shares the same settings and ground/reference among each bank in the logical amplifier/stimulator.

For analog recording, there are several different referencing modes; each logical amplifier can use the ground as a reference, use a shared reference, use a unique reference on each bank or implement full per-channel differential referencing.

The SIM may also include digital input boards for inputting signals from an Intan RHD2000 amplifier board and SPI Interface Cables, with up to 128 channels per digital board. Each digital board can be its own logical amplifier, isolated from the other boards, or be grouped with other digital boards in a larger logical amplifier configuration.

A touchscreen interface provides system information and remote arming of the stimulator boards.

SIM devices are available in 2, 4, or 8 bank models. The SIM can support a total of up to 128 analog channels, up to 256 digital channels, up to 128 stimulation channels (32 simultaneously), or up to 256 mixed channel types. The total number of channels is generally reduced to 128 at higher sampling rates, up to 50kHz. See "Sampling Rate and Digital Input Channels" on page 6-7, for more information.

System Hardware

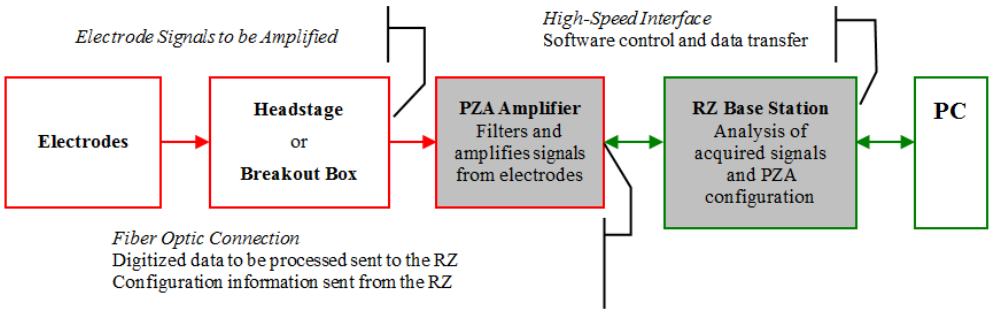
Recording (PZA and PZD)

The Subject Interface accepts inputs from a variety of electrode/headstage combinations via the back-panel. Each analog board (PZA) has a mini-DB26 connector that accepts 16 recording channels (or 8 differential channels) along with ground and reference. Digital boards (PZD) have a 12-pin Omnetics connector for Intan headstages and can accept up to 128 digital channels each. The Subject Interface can return at most 256 recording channels to the RZ base station.

Analog signals are digitized and transmitted to the RZ base station for further processing via a single fiber optic connection. Configuration information is also sent from the RZ to the SI across the fiber optic connection. The Subject Interface connects to the fiber optic port labeled 'To SI' on the back of an RZ base station configured with a DSP-M card.

A standard recording configuration includes electrodes appropriate to the input signals, a breakout box or one or more Z-Series headstages, a Subject Interface and an RZ base station.

The diagram below illustrates this flow of data and control information through the analog system.



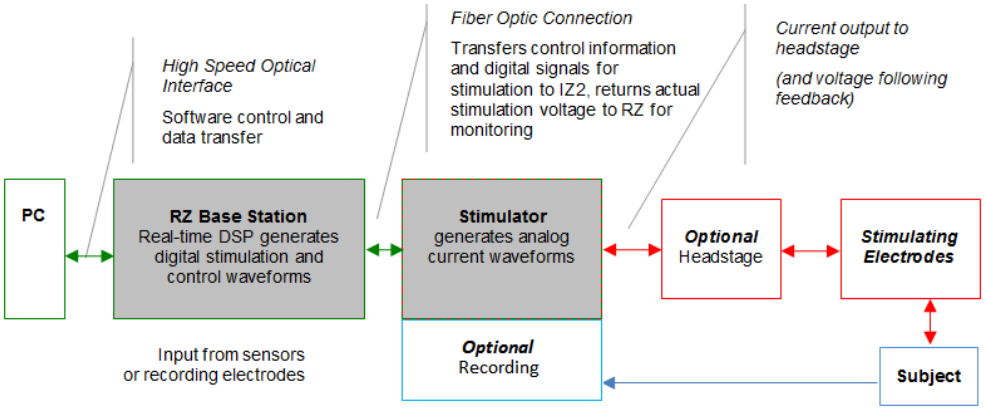
PZA/PZD Data and Control Flow Diagram

Stimulation (IZV)

The Subject Interface accepts 16 channels per bank (mini-DB26 connector) and ground.

A typical system consists of a Subject Interface and an RZ processor equipped with a specialized DSP (RZDSP-M) and additional fiber optic connector on the back panel.

The diagram below illustrates this flow of data and control information through the stimulator system.



IZV Data and Control Flow Diagram

In current controlled mode, the driving voltage is adjusted based on the electrode impedance. Analog-to-digital (A/D) converters read the output voltage on the stimulating channels and send that information back to the RZ for monitoring.

The Stimulator System

The IZV stimulator can deliver arbitrary waveforms of up to 20 kHz bandwidth. Each channel uses PCM D/As to ensure sample delays of only 4 samples.

Special circuitry on the IZV converts low voltage waveforms from the D/A converters to constant voltage or constant current waveforms.

Safety

When Safety Mode is enabled in Synapse, the SIM must be armed by the user before any current can flow. The hardware ensures that maximum output current is not exceeded. The SIM is battery powered and thus isolated from any mains power.

Physical Amplifier

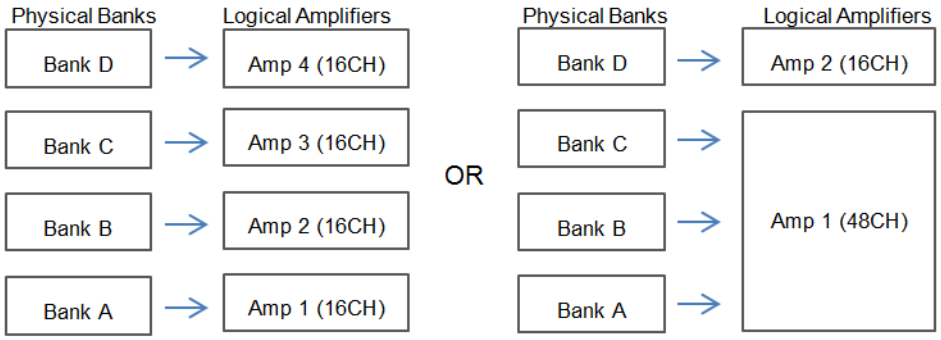
All SIM analog input channels are organized into groups of 16 channel banks, with each bank corresponding to a rear panel headstage connector (labeled alphabetically from bottom to top) and a front panel LED display.

Digital input channels are associated with a digital board corresponding to a rear panel digital input connector (labeled from bottom to top following, alphabetically, any analog input connectors). Each digital board is a bank that can comprise 16, 32, 64, 96, or 128 channels, depending on the connected Intan amplifier board(s).

Each bank is electrically isolated and can be independently configured or grouped with other banks and defined as a logical amplifier. Analog and digital boards cannot be combined.

Logical Amplifiers/Stimulators

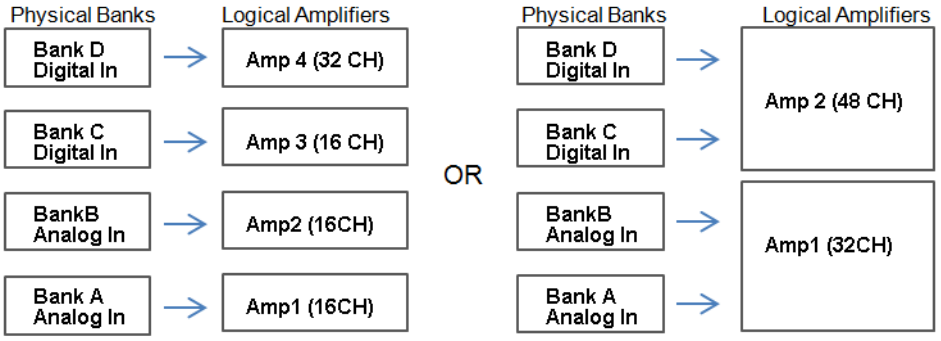
Though each bank has its own ground and reference, a single ground and reference can also be defined and shared across all banks of the logical amplifier. See Reference Modes for analog input banks below.



Two Possible Logical Amplifier Configurations for an SI4 64 Channel NeuroDigitizer (all analog input)

Digital boards can be configured individually or grouped to share a single ground and use common filter settings and sampling rate.

Note: Channel numbering on digital input banks can be non-sequential when sampling at 50 kHz. See "Sampling Rate and Digital Input Channels" on page 6-7.



Two Possible Logical Amplifier Configurations for a SI4 with two analog cards and two digital input cards

Logical amplifier configurations are defined in Synapse software. In the same manner, IZV stimulator banks can also be grouped into logical stimulators and this is controlled in Synapse.

Analog Recording Reference Modes

The SIM PZA boards support four referencing modes for each logical amplifier: Local, Shared, None and Differential. Reference and Ground configurations are defined in Synapse software. See "Pinout Diagrams" on page 6-15.

Local

In Local reference mode, each bank of channels in a logical amplifier uses its own reference input (pin 5) as the reference for that bank.

Shared

In Shared mode, the reference (pin 5) of the first bank of the logical amplifier acts as a reference for all banks in the logical amplifier.

None

In None mode, the references for all banks of a logical amplifier are tied to the Ground (pins 15).

Differential

In Differential mode, the inputs in each bank of the logical amplifier are paired; odd channels serve as recording (+) channels and each even channel is used as an individual reference (-) channel for the preceding odd channel. No connections should be made to pin 5.

Sampling Rate and Onboard Filters

The sampling rate of each logical amplifier is adjustable (max 50 kHz, min 750 Hz) and should be set to a value appropriate for the signal of interest. Reducing the sampling rate when acquiring low-frequency analog signals yields higher bit resolution and improved signal-to-noise. Use the Amp Type presets as a guide for determining what sampling rate to use for each logical amplifier.

The onboard down-sampling filters are used to further reduce the noise from frequencies above the band of interest and can be set to a percentage of the sampling rate (max 45%, min 10%). Adjusting the sampling rate and filter for each logical amplifier to match your desired signal gives you the best possible signal fidelity.

Sampling Rate and Digital Input Channels

When a logical amplifier contains digital inputs, the sampling rate should be set to a value appropriate for the connected Intan amplifier board. Sampling rates at or above 50 kHz reduce the number of channels available on the amplifier boards.

At 50 kHz the 32 channel amplifier board is limited to 20 channels and the 64 and 128 channel boards are limited to 40 channels, at the time of this writing. The maximum aggregate number of channels is 256 channels at up to 25kHz, or 128 channels at up to 50kHz.

At 50 kHz the native channel numbers per board are 1-20 and 33-52. These channel numbers are then offset by the number of channels existing in the lower banks of the SIM. Also see “Input Connectors” on page 6-15.

SIM Software Control

All SIM configuration and control of data acquisition is managed through Synapse. The PZA and PZD objects configure the analog and digital headstage recording inputs, and the IZV object controls the stimulator outputs. Please see the Synapse Manual for more information.

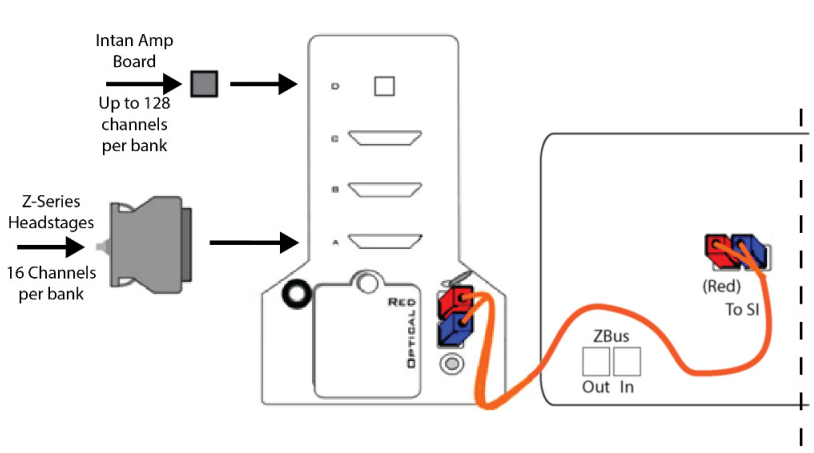
Hardware Setup

TDT recommends fully charging the SIM before use. The SIM battery charger connects to the round female connector located on the back panel.

Important! To avoid introducing EMF noise, DO NOT connect the charger to the SIM while collecting data.

A 5-meter paired fiber optic cable is included to connect the neurodigitizer to the base station. The connectors are color coded and keyed to ensure proper connections.

The diagram below illustrates the connections necessary for PZA or PZD operation.



System Connection Diagram for PZA or PZD with RZ2

Connecting Headstages and Electrodes

Analog signals are input via multiple mini-DB26 connectors on the SIM back panel.

For high impedance recordings, one or more Z-Series headstages can be connected to the input connectors on the PZA back panel. For low impedance recordings, an S-BOX input splitter or LI-CONN low-impedance connector can be used. Alternately, custom connectors and a breakout box with a male mini-DB26 connector can be used. If using custom connectors, see “Pinout Diagrams” on page 6-15.

Digital signals are input via Intan connectors on the SIM back panel.

Powering ON/OFF

To turn the neurodigitizer on, move the toggle switch located on the back panel of the SIM to the ON position.

Using the SIM Front Panel Display

The front display is a touchscreen interface for monitoring the status of SIM banks as well as arming IZV stimulators. Banks are color coded by card type. Blue is a PZA analog recording card, Green is a PZD digital recording card, and Purple is an IZV Stimulator card. Each card box maps, in order, to the right-hand buttons on the front face of the SIM.

Main Configuration Screen

The Main Configuration screen provides a touchscreen interface for monitoring SIM banks. It also provides access to the SIM device settings, such as the screen brightness, as well as tools for viewing system information, such as battery status, and updating the device software.

The main configuration screen includes the following:

Display the System Setup screen. See "System Setup Screen" on page 6-10, for more information.

Screen Off Turns the screen off. This helps reduce electrical interference during MRI recordings.

Battery Status Display battery status information. A lightning bolt through the icon indicates that the SIM is charging.

When the SIM is configured in Synapse, the Phys<->Logic button switches between displaying individual bank information and organizing them by logical amplifier/ stimulator.

Press on the bank (or press the corresponding bank button on the right side of the SIM) to show more information about that bank and how it is configured. For amplifier cards, this includes how the reference is configured. For stimulator cards, this includes the maximum compliance voltage and also an interface to Arm the device, if Remote Arming is enabled in Synapse.

Battery Status

The Battery Status is displayed after touching the  Battery Status icon.

Information displayed includes:

Charging Indicates if the charger is plugged into the SIM (Yes/No).

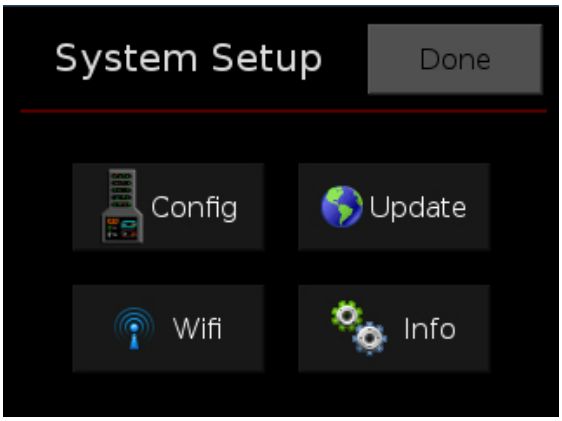
Voltage Current voltage level of the battery pack.

Level % battery life remaining.

Endurance Estimated time of battery life remaining.

System Setup Screen

The System Setup screen is displayed by touching the SIM logo on the top-left of the Main Configuration screen.



Settings include:

Config	Open the System Configure screen.
Update	Update onboard software over the Internet.
Wifi	Connect to a wireless network for system updates.
Info	Open the device System Info screen to view version numbers for various hardware, software and firmware components.

System Configure Screen

The System Configure screen is displayed by touching Config on the System Setup screen.

Settings include:

Brightness	Select High, Medium, or Low to set touchscreen brightness.
Wireless	Enable/disable the wireless connection.

System Info Screen

The System Info screen is displayed by touching Info on the System Setup screen. Use the scroll bar to see all of the version numbers.

Information displayed includes:

Device	SIM model number (e.g. SIM10-4).
Software version	Currently installed version of onboard software.
Firmware version	Currently installed version of firmware.
Hardware version	Version of hardware.
Battery	Date and capacity of last battery calibration (in mAhr).

Advanced Button

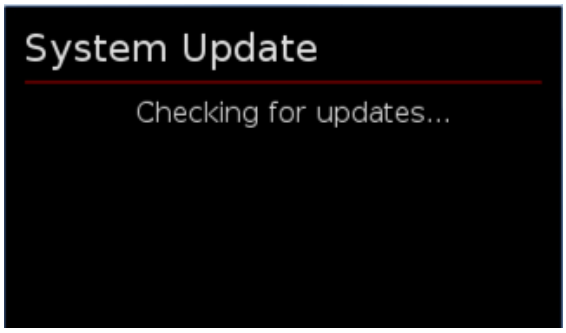
Password protected settings for TDT use only at this time.

System Update Screen

The system updater connects to a TDT server to download the latest SIM software and automatically update the device. This requires an active and configured Internet connection. The SIM provides two options for network connection: WiFi and Ethernet. The WiFi connection can be configured on the Wireless Networks screen, see below. The Ethernet port is located on the back panel.

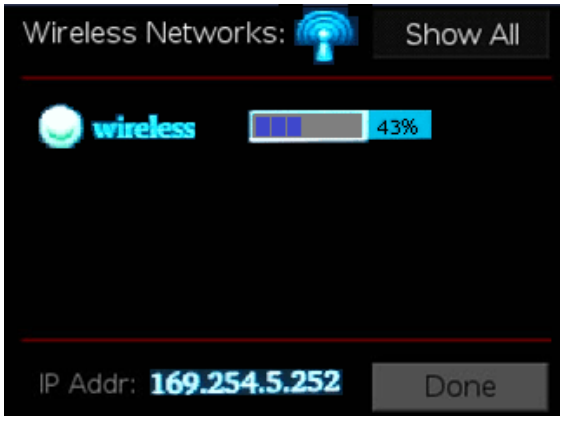
The System Update screen is displayed by touching Update on the System Setup screen.

Important! The update process can take up to an hour to complete. Make sure the SIM battery charger is plugged in during the update.



Wireless Networks Screen

The Wireless Networks screen is displayed by touching WiFi on the System Setup screen. Available networks that have been used or previously configured are displayed in the main area of the screen. Selecting a network from the list displays network information and enables the user to connect to the network, forget the network, or cancel configuration of the network.



The wireless icon  shows if the wireless feature is enabled or disabled. A red 'x' will appear through the icon if wireless is disabled. Enable/disable wireless through the System Configure Screen.

Show All Shows all networks, including networks that have not been previously used or configured.

IP Addr Displays current IP Address when connected to a network.

SIM Features

Clip Warnings and Activity Display

The front panel LEDs can be used to indicate spike activity and/or clip warning for analog input channels. They can be configured under software control using the PZA, PZD, and IZV gizmos in Synapse.

LED Indicators (stimulator)

The stim LEDs are located on the front plate of the SIM and indicate the voltage at the corresponding electrode site. The stim LED will turn green when a channel has greater than +/- 150 mV at the output and will turn red when a channel output is beyond +/- 10 V.

If Safety Mode is enabled, four RED leds indicate a fault state. Four green LEDs indicate it is ready to be armed.

LED Indicators (analog)

LEDs for each channel are lit green to indicate activity or red to indicate a clip warning. The top row indicates the odd channels (left to right). The bottom row indicates the even channels.

Green: Activity

Red: Clip Warning

Clip Warning

Analog clipping occurs when the input signal is too large. When the input to a channel is within 3 dB of the SIM's maximum voltage input range the LED for the corresponding channel is lit red to indicate that clipping may occur.

Activity

When configured to indicate activity, LEDs are lit green whenever a unit (spike) occurs on the corresponding channel. The sensitivity threshold for the green LED is ~200 uV.

LED Indicators (digital)

LEDs that represent digital input boards, indicate the number of input channels with each LED indicating 16 channels. For example, four LEDs indicates 64 input channels have been detected on that connection.

External Ground

The external ground is optional and should only be used in cases where the subject occasionally contacts a metal surface that isn't tied to the animal ground, such as a lever press. When contact is made, a ground loop is formed that temporarily adds extra noise to the system. Grounding this metal surface directly to the TDT hardware removes this ground loop at the cost of raising the overall noise floor a small amount.

A banana jack located on the back of the SIM provides connection to common ground. The PZA or PZD gizmos allow you to float that ground connection on individual logical amplifiers.

A cable kit is also provided to ensure cables used with the external ground are suitable for this use. Each kit includes: one male banana plug to male banana plug pass through and one male banana plug to alligator clip pass through. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

Battery Overview

The SIM neurodigitizer features a 32 Amp-hour Lithium ion battery pack.

Charging the Batteries

Operate the neurodigitizer with the charging cable disconnected. An external battery pack (PZ-BAT) or external charger and extra battery is available to provide longer battery life for extended recording sessions. See "PZ-BAT External Battery Pack for the PZ Amplifiers" on page 7-109 and "PZ5-BAT External Charger" on page 7-105.

SIM Technical Specifications

Stimulator Output	Up to 8 cards
Stim Output Channels	16 per card
Stim Output Voices	4 per card
Stim Compliance Voltage	Up to ± 15V* (user selectable from 15, 10, 7, 5, 3, 1.5, 1.0, and 0.5V) ± 5 mA per voice, up to 3 kOhm load[º]
Stim Output Resolution	Voltage Mode: 100 uV Current Mode: 10 nA
DC Offset Current	Active channel: < 100 nA Open channel: < 1 nA
Sample Rate	Up to 48828.125 Hz
Analog A/D Input	Up to 8 cards (128 channels), hybrid
Maximum Voltage In	± 500 mV
A/D Sample Rate	Up to 48828.125 Hz (adjustable in steps of approximately 750, 1500, 3000, 6000, 12000, 25000, and 50000 Hz)^
Frequency Response	DC coupled: 0 Hz – 0.45×Fs AC coupled: 0.4 Hz – 0.45×Fs
S/N (typical)	104 dB, single unit, Fs = 25 kHz, 300-7000 Hz 116 dB, differential, Fs = 750 Hz, 0.4-300 Hz

Sample Delay	Dependent on SIM and RZ processor sample rates (RZ at 25 kHz)(RZ at 12 kHz) SIM rate — samples — samples 25 kHz — 22 — x 12 kHz — 40 — 23 6 kHz — 76 — 42 3 kHz — 141 — 79 1.5 kHz — 270 — 152 750 Hz — 543 — 295
DC offset	< ± 10 µV
Input Referred Noise	Single Ended: 3.0 µVrms, 300-7000 Hz, 25 kHz Differential: 0.75 µVrms, 0.4-300 Hz, 750 Hz
Distortion (typical)	< 1%
Input Impedance	AC coupled: 100 kOhm DC coupled: 20 MOhm
Battery Capacity	32 Amp-hour
Battery	8-10 hours to charge to 95% capacity, 14 hours to fully charge. Battery life between charges: 2 active boards ~ 50 hrs 4 active boards ~ 35 hrs 6 active boards ~ 27 hrs 8 active boards ~ 22 hrs
Charger	External 12V, 2.5A power supply, center negative
Indicator LEDs	Up to 128 status/clip warning/digital input channel count
Fiber Optic Cable	5 meters standard, cable lengths up to 20 meters. If longer cable lengths are required, contact TDT.
Ethernet Port	100 Mbps

***Note:** Higher compliance voltages can be attained by wiring stimulus banks together

ºNote: Higher current outputs can be attained by targeting the same channel with multiple voices

^Note: If recording at ~50 kHz on 128 channels, see "SIM Software Control" on page 6-7, for more information.

RHD2000 series amplifier boards and SPI interface cables are available from Intan Technologies.

Important! The specifications below are dependent on the amplifier board. See Intan RHD200 series website for latest, full performance specifications.

Digital Headstage Input	Up to 8 cards (256 channels), 1 input per card
Sampling Rates	Up to 25kHz
Frequency Response	0.1 Hz - 10 kHz
Amp Input Range	± 5 mV
Allowable DC Offset	± 0.4 V

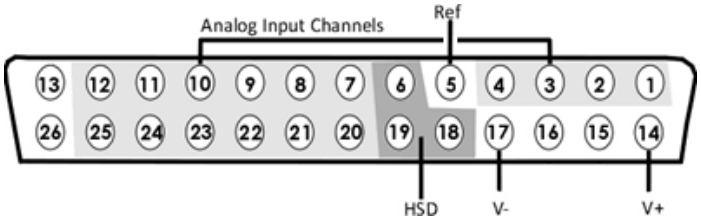
Input Connectors

SIM NeuroDigitizers have up to eight 26-pin headstage connectors (analog) or up to four 12-pin Omnetics nano connectors (digital) on the back of the unit. The connectors are labeled alphabetically from bottom to top. Each connector carries signal for one bank of channels with ground and reference. The corresponding channel numbers depend on 1) the reference mode configurations or number of channels in a connected digital amplifier board and 2) the position of the bank in a logical amplifier.

For simplicity sake, the diagrams below assume channels for that connector begin with channel 1. For example, A1 – A16 represent the 16 channels coming from the connected headstage. The user must increment the channel numbers by 16 (or 8) according to the mode and position of the connector. So, for the connector labeled 'A', A1 is channel 1 while on the connector labeled 'B', A1 may be channel 17.

Pinout Diagrams

Local, None or Shared Reference Mode



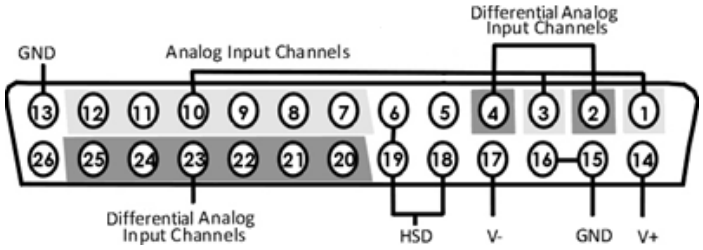
Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		14	V+	Positive Voltage (+2.5V)
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17	V-	Negative Voltage (-2.5V)
5*	Ref*	Reference*		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A5	Analog Input Channels		20	A6	Analog Input Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	^	See notes below		26	NA	Not Used

^Note: In Local reference mode, Pin 13 is AltRef. Otherwise, Pin 13 is Ground.

* In Shared reference mode, only Pin 5 of the first bank of the logical amplifier is connected. It is shared internally among the other banks of the logical amplifier.

* In None reference mode, Pin 5 is not connected.

Differential Reference Mode



Note: There are 8 (+) channels and 8 (-) channels per DB26 connector. Subsequent banks are indexed by an additional 8 channels.

Pin	Name	Description	Pin	Name	Description
1	A1(+)	Analog Input Channel	14	V+	Positive Voltage (+2.5V)
2	A1(-)	Differential Analog Input Channel	15	GND	Ground
3	A2(+)	Analog Input Channel	16	GND	
4	A2(-)	Differential Analog Input Channel	17	V-	Negative Voltage (-2.5V)
5	NA	Not Used	18	HSD	Headstage Detect
6	HSD	Headstage Detect	19	HSD	
7	A3(+)	Analog Input Channels	20	A3(-)	Differential Input Channels
8	A4(+)		21	A4(-)	
9	A5(+)		22	A5(-)	
10	A6(+)		23	A6(-)	
11	A7(+)		24	A7(-)	
12	A8(+)		25	A8(-)	
13	GND	Ground	26	NA	Not Used

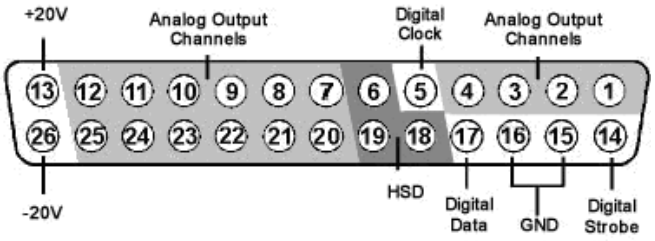
Note: See this tech note before attempting to make any custom connections.

https://www.tdt.com/technotes/#0896.htm

Digital Connectors

The digital input connector is a self-aligning 12-pin Omnetics PZN-12 polarized nano connector that mates directly to an Intan RHD2000 SPI interface cable.

Stimulator Connectors



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channels		14		Digital Strobe
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17		Digital Data
5		Digital Clock		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A5	Analog Output Channels		20	A6	Analog Output Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	V+	+20 V		26	V-	-20 V

Note: See this tech note before attempting to make any custom connections.
https://www.tdt.com/technotes/#0896.htm

Part 7: Preamplifiers

PZ5 NeuroDigitizer

PZ5 Overview

The PZ5 is a multi-modal neurodigitizer suitable for recording a broad range of biological potentials. Its analog input boards combine the functionality of the PZ2 and PZ3 amplifiers in a single device that can be used for both high and low impedance input signals simultaneously. The PZ5 may also include digital input boards for inputting signals from an Intan RHD2000 amplifier board with up to 128 channels.

Analog input boards oversample the signal with very fast instrumentation grade converters. TDT's custom hybrid A/D circuit yields 28 bits of resolution and unparalleled dynamic range. Optional DC coupling offers zero phase distortion across the signal bandwidth. Sampling rate and down-sampling filters can be optimized on each logical amplifier for the intended input type to optimize signal fidelity. The +/-500 mV input range is large enough to accept any biological potential and most stimulus artifacts without saturating.

The neurodigitizer analog inputs are organized into 16-channel banks. Each bank is electrically isolated, meaning the ground and reference channels are not inherently shared between banks. Multiple banks can be grouped into a single logical amplifier that shares the same settings and ground/reference among each bank in the logical amplifier. There are several different referencing modes; each logical amplifier can use the ground as a reference, use a shared reference, use a unique reference on each bank or implement full per-channel differential referencing.

Digital inputs are used exclusively with RHD2000 series amplifier boards and SPI Interface Cables, available from Intan Technologies. Each input serves as a bank of channels and may be up to 128 channels, depending on the connected amplifier board. Each digital board can be its own logical amplifier, isolated from the other boards, or be grouped with other digital boards in a larger logical amplifier configuration.

A touchscreen interface provides immediate preview of inputs, impedance checking and real-time control and configuration options for each amplifier bank.

PZ5 neurodigitizers are available in 32, 64, 96, or 128 analog channel models.The PZ5 is also available with 2 or 4 digital inputs and models that combine 32 or 64 analog input channels with 2 or 4 digital inputs. The PZ5 can support a total of up to 128 analog channels or up to 256 digital channels or up to 256 mixed channel types. the total number of channels is generally reduced to 128 at higher sampling rates, up to 50kHz. See "Sampling Rate and Digital Input Channels" on page 7-7, for more information.

Note: To record at ~50 kHz on 128 or more channels, see "PZ5 Software Control" on page 7-7, for more information.

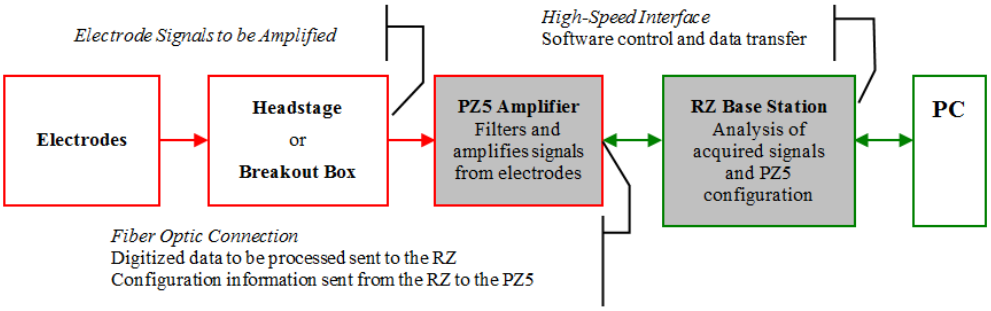
System Hardware

The PZ5 neurodigitizer accepts inputs from a variety of electrode/headstage combinations via the back-panel mini-DB26 connectors. Each mini-DB26 connector inputs 16 recording channels (or 8 differential channels) along with ground and reference. Intan input connectors accept up to 128 digital channels.

Recorded analog signals are amplified and digitized. All channels are transmitted to the RZ base station for further processing via a single fiber optic connection. Configuration information is also sent from the RZ to the PZ5 neurodigitizer across the fiber optic connection. The PZ5 can connect to the 'PZ' fiber optic input on an RZ2 or RZ5D base station, or directly to an RZDSP_P card on any RZ base station.

A standard configuration includes electrodes appropriate to the input signals, a breakout box or one or more Z-Series headstages, a PZ5 neurodigitizer and an RZ base station.

The diagram below illustrates this flow of data and control information through the analog system.



PZ5 Data and Control Flow Diagram

Physical Amplifier

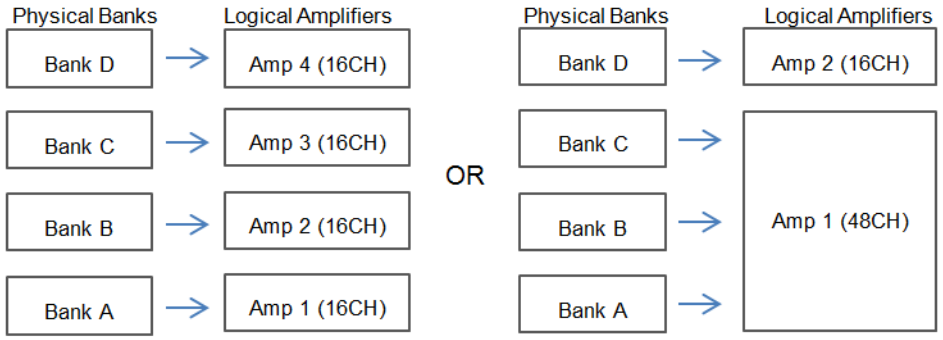
All PZ5 analog input channels are organized into groups of 16 channel banks, with each bank corresponding to a rear panel headstage connector (labeled alphabetically from bottom to top) and a front panel LED display.

Digital input channels are associated with a digital board corresponding to a rear panel digital input connector (labeled from bottom to top following, alphabetically, any analog input connectors). Each digital board is a bank that can comprise 16, 32, 64, 96, or 128 channels, depending on the connected Intan amplifier board(s).

Each bank is electrically isolated and can be independently configured or grouped with other banks and defined as a logical amplifier. Analog and digital boards cannot be combined together.

Logical Amplifiers

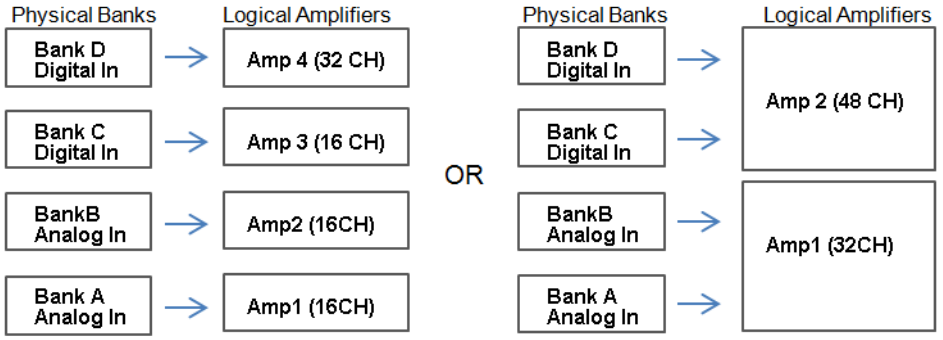
Though each bank has its own ground and reference, a single ground and reference can also be defined and shared across all banks of the logical amplifier. See Reference Modes for analog input banks below.



Two Possible Logical Amplifier Configurations for a PZ5-64 64 Channel NeuroDigitizer (all analog input)

Digital boards can be configured individually or grouped to share a single ground and use common filter settings and sampling rate.

Note: Channel numbering on digital input banks can be non-sequential when sampling at 50 kHz. See "Sampling Rate and Digital Input Channels" on page 7-7.



Two Possible Logical Amplifier Configurations for a PZ5-64-2 (with two digital inputs)

Logical amplifier configurations can be defined using the front panel interface (see "Using the PZ5 Front Panel Display" on page 7-10) or the PZ5_Control macro. The PZ5-32 model can have a maximum of two logical amplifiers configured. All other PZ5s can have a maximum of four logical amplifiers.

Reference Modes

The PZ5 supports four referencing modes for each analog input logical amplifier: Local, Shared, None and Differential. Reference and Ground configurations for each logical amplifier can be defined using the PZ5_Control macro or via the touchscreen interface. See "Pinout Diagrams" on page 7-28.

Local

In Local reference mode, each bank of channels in a logical amplifier uses its own reference input (pin 5) as the reference for that bank.

Shared

In Shared mode, the reference (pin 5) of the first bank of the logical amplifier acts as a reference for all banks in the logical amplifier.

None

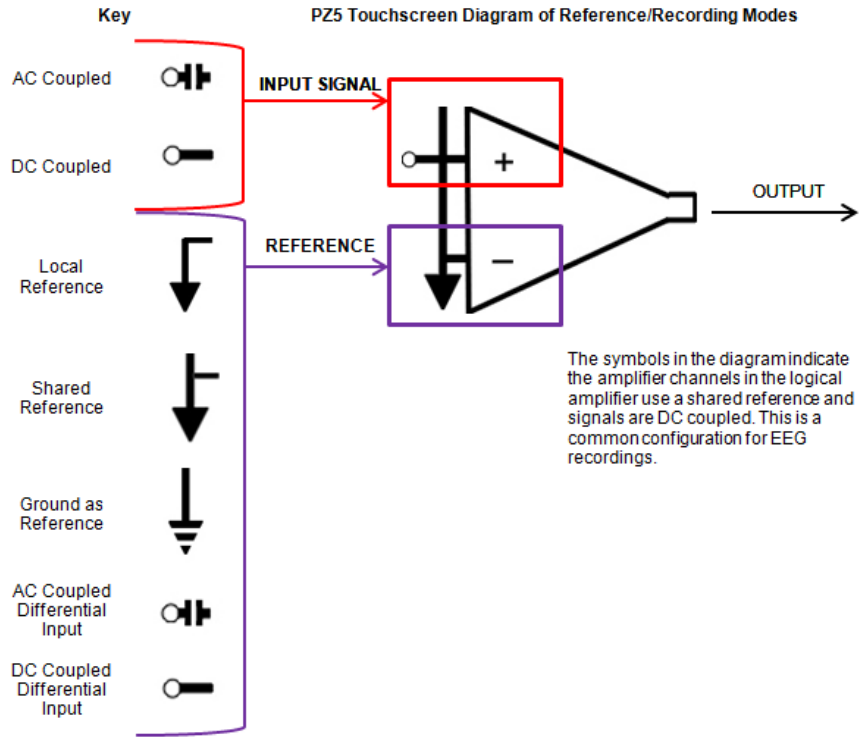
In None mode, the references for all banks of a logical amplifier are tied to the Ground (pins 13, 15, and 16).

Differential

In Differential mode, the inputs in each bank of the logical amplifier are paired; odd channels serve as recording (+) channels and each even channel is used as an individual reference (-) channel for the preceding odd channel. No connections should be made to pin 5.

The Signal/Reference Diagram

The PZ5 touchscreen interface uses representative diagrams to enable users to identify the configuration of the amplifier at a glance. The table below explains the parts of the diagram and what each represents.



Sampling Rate and Onboard Filters

The sampling rate of each logical amplifier is adjustable (max 50 kHz, min 750 Hz) and should be set to a value appropriate for the signal of interest. Reducing the sampling rate when acquiring low-frequency analog signals yields higher bit resolution and improved signal-to-noise. Use the Amp Type presets as a guide for determining what sampling rate to use for each logical amplifier.

The onboard down-sampling filters are used to further reduce the noise from frequencies above the band of interest and can be set to a percentage of the sampling rate (max 45%, min 10%). Adjusting the sampling rate and filter for each logical amplifier to match your desired signal gives you the best possible signal fidelity.

Sampling Rate and Digital Input Channels

When a logical amplifier contains digital inputs, the sampling rate should be set to a value appropriate for the connected Intan amplifier board. Sampling rates at or above 50 kHz reduce the number of channels available on the amplifier boards.

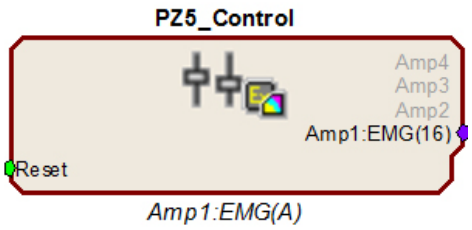
At 50 kHz the 32 channel amplifier board is limited to 20 channels and the 64 and 128 channel boards are limited to 40 channels, at the time of this writing. The maximum aggregate number of channels is 256 channels at up to 25kHz, or 128 channels at up to 50kHz.

It is also important to note that, while the Intan board channel numbers are normally sequential and offset by the number of analog inputs in the amplifier, sampling at or above 50 kHz may also affect channel numbering.

At 50 kHz the native channel numbers per board are 1-20 and 33-52. These channel numbers are then offset by the number of channels existing in the lower banks of the PZ5. Also see “Input Connectors” on page 7-27.

PZ5 Software Control

The PZ5_Control macro provides configuration and control of data acquisition and storage via the RCX control circuit running on the RZ base station. The PZ5_Control macro sets the default logical amplifier configurations when the circuit first runs and retrieves waveforms/impedance values in real-time from each logical amplifier for further processing.



The macro configuration options are available in the macro properties dialog and can be accessed by double-clicking the macro in the RPvdsEx circuit diagram.

The macro outputs a multi-channel signal stream of the acquired signals for each logical amplifier. If the reference mode is Differential, then the 1st channel is Ch1 minus Ch2 and the second channel is

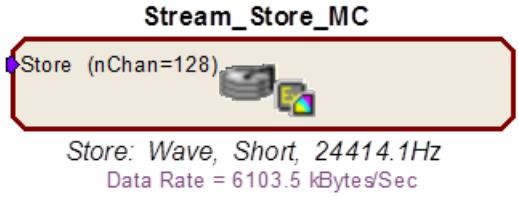
Ch2 minus Ch1 and so on. The output for any logical amplifier in impedance checking mode is the channel impedance, in MΩ.

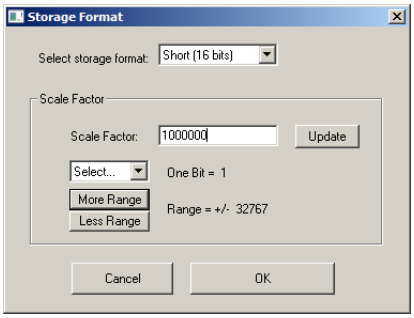
Important! If connecting to an RZDSP_P card, the PZ5_Control macro must be assigned to the DSP slot occupied by the RZDSP_P card. If connecting to an RZ5D the macro must be running on DSP-3.

Recording 128 Channels at 50 kHz

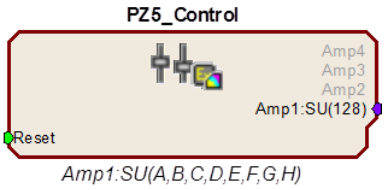
Due to the PZ5's high bit resolution and recording capabilities, data should always be stored as 32-bit floating point. However, when storing 128 channels at 50 kHz sampling rate, you must use the Short (16 bits) format due to bandwidth constraints. This means the data will be scaled and converted into an integer before storage, which narrows the dynamic range of the acquired signals. In this case, all DC offsets must be removed before the data is stored. You can either filter out the DC offset with a NeuroFilter or HP-LP_Filter_MC macro, or use AC coupling on the logical amplifier if you are storing the raw signal direct from the PZ5.

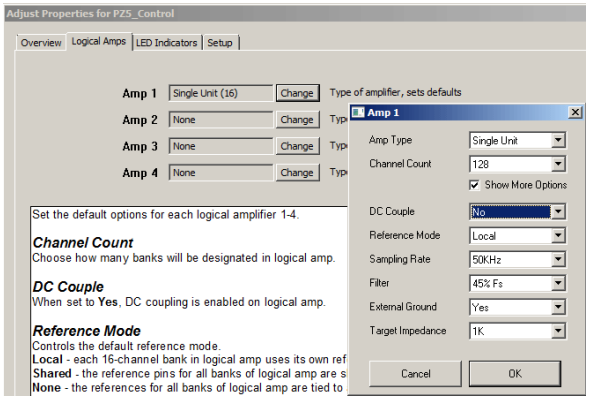
The data storage format is configured via a stream store macro in the RCX control circuit running on the RZ base station, such as Stream_Store_MC and Stream_Store_MC2 if writing into a data tank, and Stream_Server_MC or Stream_Remote_MC if streaming to an RS4 or PO8e. The configuration options are available in the macro properties dialog and can be accessed by double-clicking the macro in the RPvdsEx circuit diagram, then clicking the Store Format button on the Options tab.





AC coupling can be set using the touch screen configuration options or on the Logical Amp tab of the PZ5_Control macro properties dialog.





These changes are required only when recording 128 channels at 50 kHz. In every other case, the Float (32 bits) format should be used to utilize the full bit resolution of the PZ5.

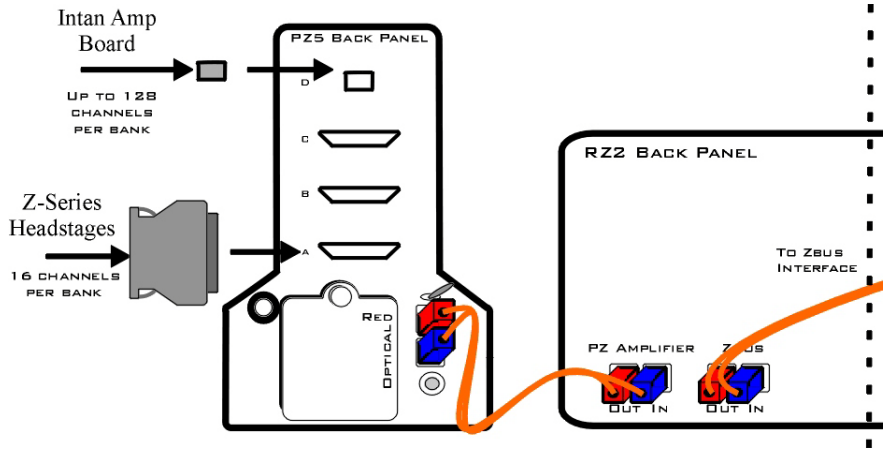
Hardware Setup

TDT recommends fully charging the PZ5 neurodigitizer before use. The PZ5 battery charger connects to the round female connector located on the back panel.

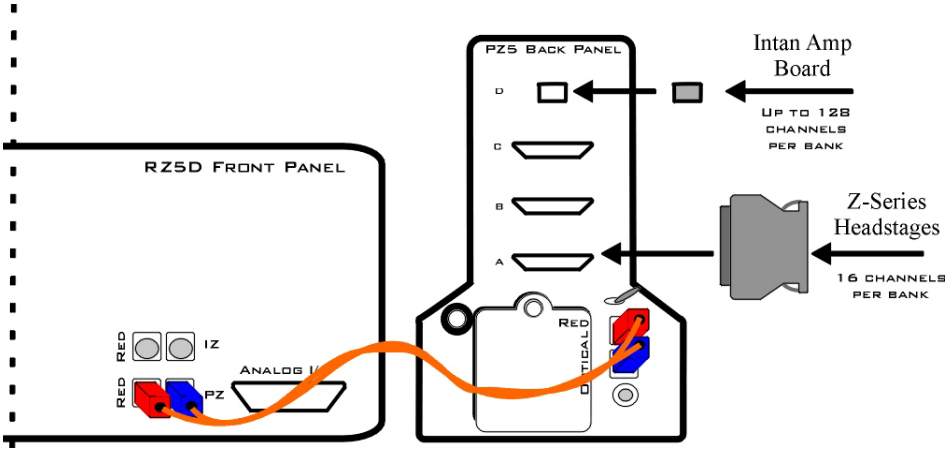
Important! To avoid introducing EMF noise, DO NOT connect the charger to the PZ5 while collecting data.

A 5-meter paired fiber optic cable is included to connect the neurodigitizer to the base station. The connectors are color coded and keyed to ensure proper connections.

The diagram below illustrates the connections necessary for PZ5 neurodigitizer operation.



System Connection Diagram for PZ5 with RZ2



System Connection Diagram for PZ5 with RZ5D

Connecting Headstages and Electrodes

Analog signals are input via multiple mini-DB26 connectors on the PZ5 back panel.

For high impedance recordings, one or more Z-Series headstages can be connected to the input connectors on the PZ5 back panel. For low impedance recordings, an S-BOX input splitter or LI-CONN low-impedance connector can be used. Alternately, custom connectors and a breakout box with a male mini-DB26 connector can be used. If using custom connectors, see “Pinout Diagrams” on page 7-28.

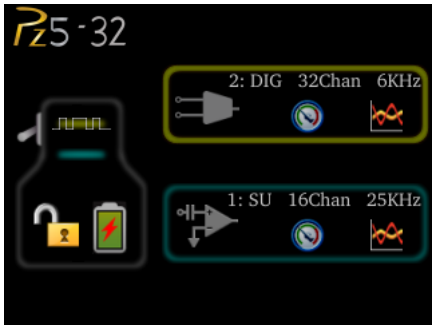
Digital signals are input via Intan connectors on the PZ5 back panel.

Powering ON/OFF

To turn the neurodigitizer on, move the toggle switch located on the back panel of the PZ5 to the ON position.

Using the PZ5 Front Panel Display

The front panel display is a touchscreen interface for impedance checking and waveform preview and can be used for on the fly device configuration. When the PZ5 is powered on, a splash screen is displayed on the touchscreen and a boot-up progress bar is displayed at the bottom of the screen. When the boot sequence is complete, the Main Configuration screen is displayed.



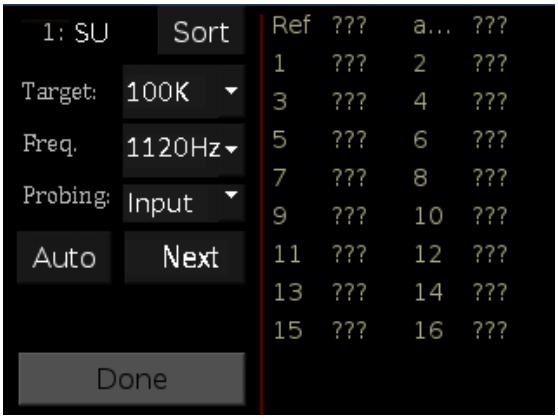
Amplifier boards are represented by horizontal bars in the PZ5 diagram. Digital input boards are overlaid with a digital signal representation. When the RZ device processing circuit runs, the logical amplifier configuration defined in the PZ5_Control is sent to the PZ5 and applied.

To test the impedance of your hardware set-up:

Important!: The impedance checking feature of the PZ5 can and should only be used with a passive headstage or direct connection to the electrodes.

1. Touch the  Test icon on the desired logical amplifier.

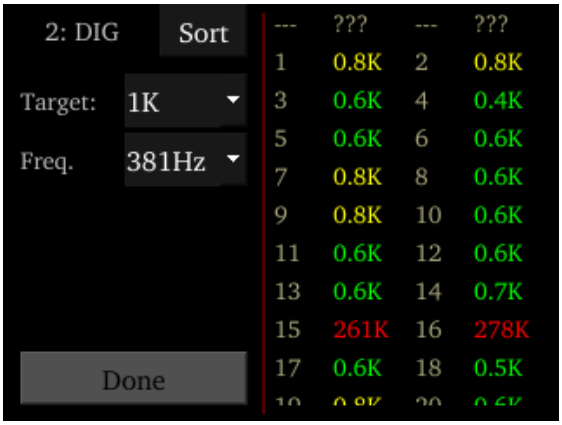
   The Impedance Checking screen will be displayed.



   or

2. In the **Target** field, select a target impedance value.
3. Set the probe signal frequency from the drop-down list.
4. For analog input channels, touch the **Next** button to cycle through each probing option for the selected logical amplifier type. “Probing Options” on page 7-20.

   The impedance values of the currently tested set are updated on the right side of the screen and are color coded for easy identification of problem channels.



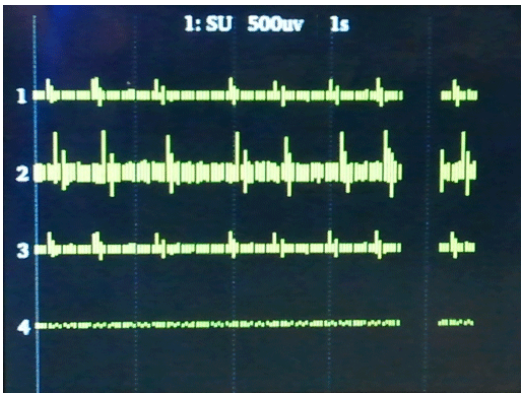
5. A limited set of channels is visible at any one time. Swipe vertically on the interface to scroll the visible channels or touch the Sort button to sort the list by channel number or by impedance value.

When the hardware connections have been made the incoming signals can be previewed on the front display.

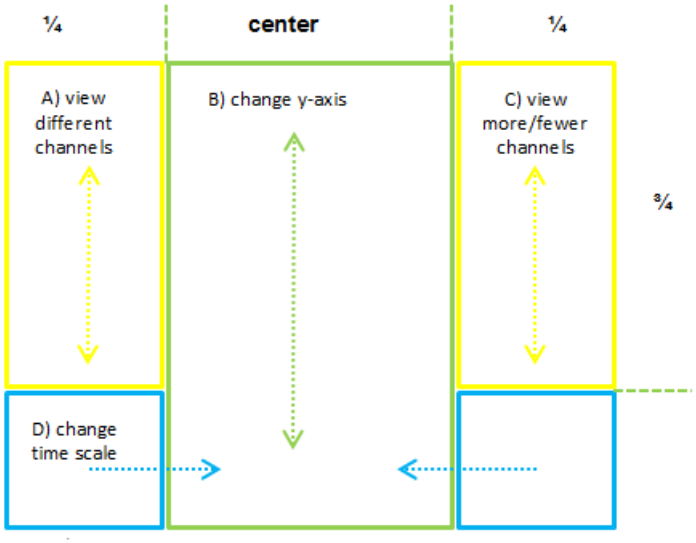
To preview the data:

1. Touch the  **Preview** icon on the desired logical amplifier to enter the Waveform Display screen.
2. To return to the Main Configuration screen from the Waveform Display screen, swipe three fingers across the screen in any direction.

Waveform Display Screen



The Waveform Display screen is displayed by touching the  Preview icon on an existing logical amplifier on the Main Configuration Option screen. The plot label includes the logical amplifier number, amp type, and voltage and time scales. The displayed waveform is decimated for plotting and high pass filtered so all channels can be shown on the same voltage scale. If the logical amplifier is DC Coupled, the DC offset is displayed as a value on the right side of each plot line (in mV). The screen view can be adjusted using touchscreen options.



To view a different subset of channels:

- Swipe up or down on the left side of the screen. (A)

To change the y-axis scale:

- Swipe up or down in the center of the screen. (B)

To view more or fewer channels:

- Swipe down or up on the right side of the screen. (C)

To change the time scale:

- Swipe left or right on the bottom of the screen. (D)

To return to the Main Configuration screen:

- Swipe three fingers across the screen in any direction.

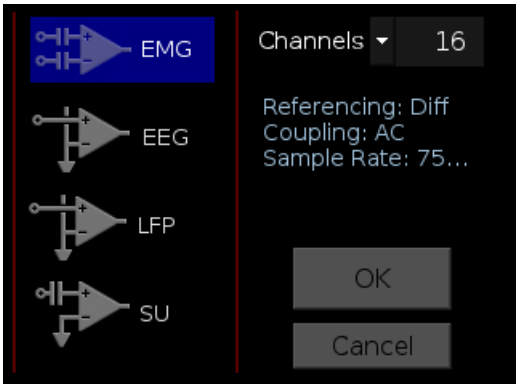
The touchscreen interface can also be used to configure logical amplifiers when the PZ5_Control is not used or for on the fly device configuration.

Typical Steps to Configure a Logical Amplifier Using the Touchscreen

To add a logical amplifier:

1. Touch the  **Plus Sign.**

   The Amp Type Selection screen is displayed.

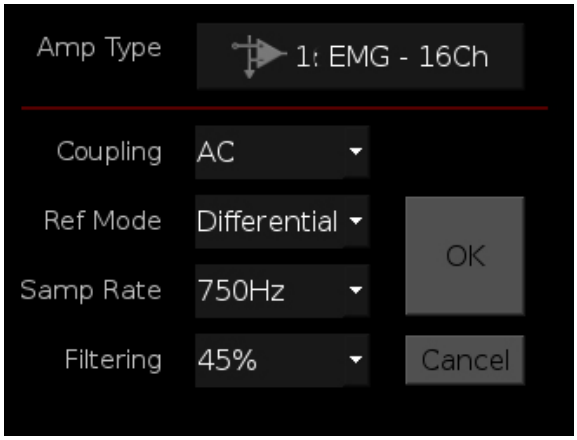


2. Touch the desired **Amp Type** icon  on the left side of the screen.

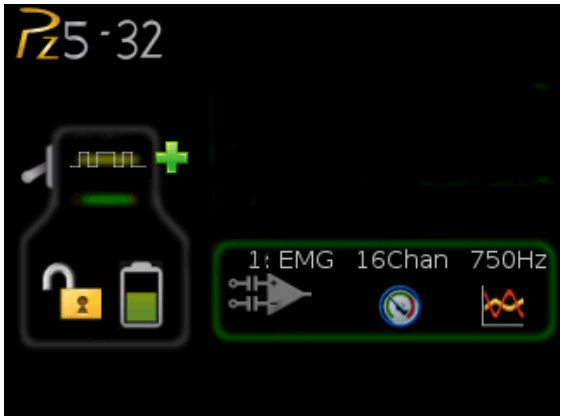
   The text to the center right of the screen displays the default configuration information.

3. Touch the arrow next to **Channels** to display the drop-down list.
4. To configure the number of channels in the logical amplifier, touch the desired number in the list.

5. Touch the **OK** button. The Configuration Options screen is displayed.



6. Make any desired changes to the default settings then touch the **OK** button to save the selections and return to the Main Configuration screen.



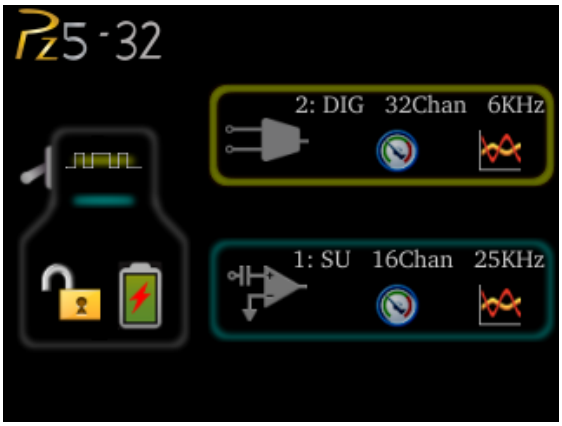
The logical amplifier is configured and a representative diagram is added to the screen.

7. To configure additional logical amplifiers, repeat these steps as needed.

The sections below provide additional information and serve as a reference for each screen.

Main Configuration Screen

The Main Configuration screen provides a touchscreen interface for configuring logical amplifiers and previewing waveforms in real-time. It also provides access to the PZ5 settings, such as the screen auto lock and auto sleep features, as well as tools for viewing system information, such as battery status, and updating the device software.



All logical amplifiers that have been defined are represented on the right side of the screen and labeled in logical order from bottom to top. For example, 2:EMG is the second logical amplifier and is configured for EMG recordings. In the illustration above, this would correspond to the back panel input connector labeled 'B'. Configured digital inputs are displayed above logical amplifiers.

The main configuration screen includes the following:

Display the System Setup screen. See "System Setup Screen" on page 7-21, for more information.

Toggle Toggle LED Indicators on or off. See "Clip Warnings and Activity Display" on page 7-24, for more information.

Battery Status Display battery status information. A lightning bolt through the icon indicates that the PZ5 is charging.

Lock/Unlock Lock to protect configuration settings. Unlock to allow changes to the configuration.

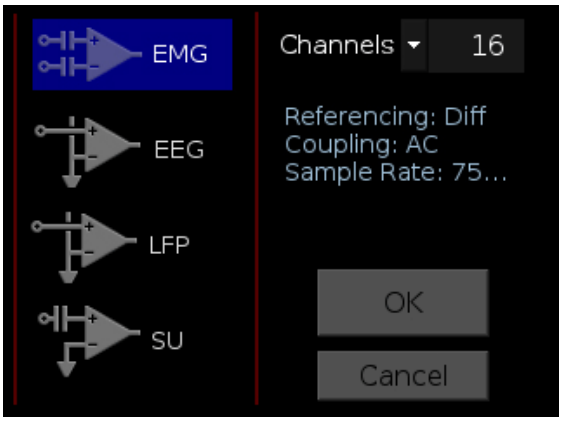
Plus Sign Create a new logical amplifier. As logical amplifiers are added they appear on the Main Configuration screen.

Banks Color coded to indicate current configuration of each bank. A red outline indicates that the bank is configured as part of a logical amplifier but no headstage is currently detected on that bank. A gray bar indicates that the bank is not configured.

Amp Type Selection Screen

The Amp Type Selection screen is displayed by touching the  Plus Sign icon on the Main Configuration screen or by touching the 

Amp Type button on the Configuration Options screen for an existing logical amplifier.



On the Amp Type Selection screen, users can set the number of channels in a logical amplifier or touch a configuration icon on the left side of the screen to select one of four amp types, each with configuration presets displayed to the right. These configuration options can be changed after the Amp Type is selected.

Options include

Select the number of channels in the logical amplifier (by banks of 16 channels).

Amp Types		Defaults
Icon	**Label**	
	**EMG**	Electromyography Referencing: Diff (true differential) Coupling: AC Sample Rate: 750Hz
	**EEG**	Electroencephalography Referencing: Shared Coupling: AC Sample Rate: 750Hz
	**LFP**	Local Field Potentials Referencing: Shared Coupling: AC Sample Rate: 3kHz
	**SU**	Single Unit Referencing: Local Coupling: AC Sample Rate: 25kHz

OK Button

Save selections and open the Configuration Options screen.

Delete Button

Delete the logical amplifier and display a confirmation screen before returning to the Main Configuration screen. **Note:** Only available after a logical amplifier has already been created.

Cancel Button

Return to Main Configuration screen without making changes.

Configuration Options Screen

The Configuration Options screen is displayed after selecting the Amp Type when adding a new logical amplifier or it can be displayed by touching the  configuration icon on an existing logical amplifier on the Main Configuration Option screen. After all analog input banks have been configured, pressing the plus sign displays the configuration screen for digital inputs, when available.

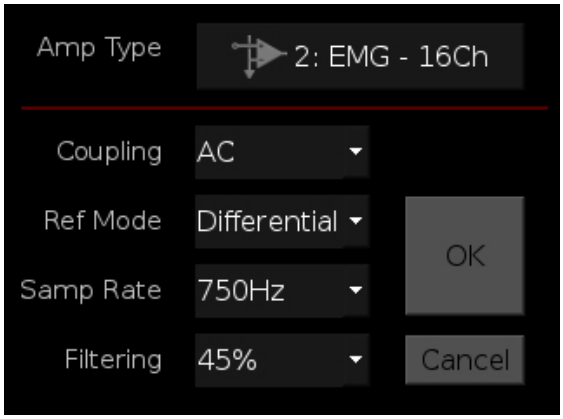
Analog Input Amp Configuration

Amp Type Button

The area at the top of the screen displays the Amp Type for the selected/new logical amplifier and includes the logical amplifier number, configuration type and number of channels.

To return to the Amp Type Selection screen:

- Touch the **Amp Type** button.



Each Amp Type includes preset values for each setting. The Configuration Options screen enables users to modify these settings.

Settings include:

Coupling — Choose AC or DC. AC coupling implements a high pass filter with ~ 0.4 Hz cutoff frequency.

Ref Mode — Choose Local, Shared, None, or Differential Reference Mode. See "Reference Modes" on page 7-5, for more information on reference modes.

Samp Rate — Choose a sampling rate from a list of values: 750 Hz, 1.5 kHz, 3 kHz, 6 kHz, 12 kHz, 25 kHz, 50 kHz.

Filtering — Select a cutoff frequency for the anti-aliasing filter, as a percentage of the sampling rate. Choose from a list of values: 45%, 35%, 25%, 15%, or 10%.

Ext. Ground — Press 'More' button to access this. Set to Yes to connect amplifier ground to external ground plug.

OK Button

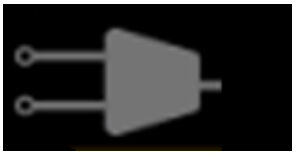
Save amp selections and return to Main Configuration screen.

Cancel Button

Return to Main Configuration screen without making changes.

Digital Input Configuration

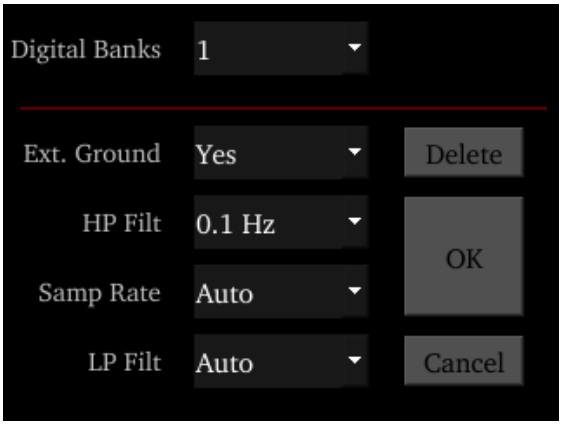
Amp Type Button



The area at the top of the screen displays the Digital Banks drop-down list. Select the desired number of banks (boards) to include in this logical amplifier.

To return to the Main configuration screen:

- Touch the **Cancel** button.



The digital input configuration includes preset values for each setting. The Configuration Options screen enables users to modify these settings.

Settings include:

Ext. Ground Yes to connect amplifier ground to external ground plug.

HP Filt Select a cutoff frequency for the highpass filter.

Samp Rate Choose a sampling rate from a list of values. Auto means it runs at whatever the RZ sampling rate is.

LP Filt Select a cutoff frequency for the lowpass filter. Auto means it is matched to the sampling rate automatically.

PZ5 Sampling Rate	LP Auto Filter
750 Hz	300 Hz
1.5 kHz	750 Hz
3 kHz	1.5 kHz
6 kHz	3 kHz

PZ5 Sampling Rate	LP Auto Filter
12 kHz	5 kHz
25 kHz	10 kHz

Delete Button

Delete amp configuration and return to Main Configuration screen.

OK Button

Save selections and return to Main Configuration screen.

Cancel Button

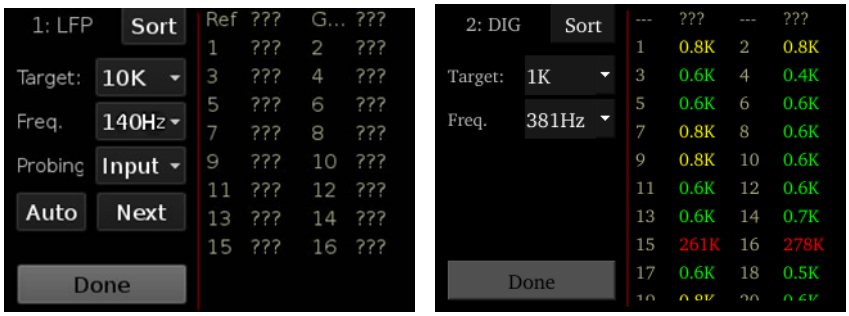
Return to Main Configuration screen without making changes.

Impedance Checking Screen

The Impedance Checking Screen is displayed by touching the  Test icon on an existing logical amplifier on the Main Configuration screen. The logical amplifier number and amp type are displayed in the top-left corner, for example 1:EEG.

Select the type of connections to measure (Probing options) and choose a target impedance value (Target) to color code the measured impedance value text. During impedance checking, all connections in the selected set are tested in parallel and the impedance is measured relative to the user-defined target impedance (1 kOhms – 100 kOhms). The impedance values of the currently tested set are updated on the right side of the screen. Toggle the Sort button to sort the list by channel number or by impedance value.

A limited set of channels are visible at any one time. Swipe vertically on the touchscreen to scroll the visible channels.



Settings include:

Target Select the target impedance from a drop down list (1 kOhms -100 kOhms). This is used to color the impedance value text during/after probing. Impedance values above the target are colored red, values <75% below the target are green and all other values are yellow.

Freq. Set the probe signal frequency from a drop down list. The frequency is adjustable from 35Hz, 70Hz, 140Hz, 280Hz, 560Hz, 1120Hz, and 2240Hz. This feature is only selectable in daughter board firmware v1.3 and above, and PZ5

	software v1.1.1 and above. The frequency is fixed at 140Hz in prior versions.
Probing	(Analog input amps only) Select the set of connections to measure. The available options in this list change depending on the logical amp referencing mode. See Probing Options below.
Sort Button	Toggle button that displays the channels with the largest variation from the target impedance at the top of the screen.
Auto Button	Toggle button that cycles through each probing option every second.
Next Button	Select to advance to the next probing option set.

Done Button

Return to Main Configuration screen.

Probing Options

The referencing mode of the currently selected analog input logical amplifier determines the available Probing options.

Differential Reference Mode

If the reference mode is Differential, the Probing options are *Inp(+)* for the positive input channels and *Inp(-)* for the differential channels. This is the default reference mode for the EMG amp type.

Local Reference Mode

If the reference mode is Local, the options are *Input* for all the input channels, *Ref* to test the reference impedance to ground, or *AltRef* to test the alternative reference (pin 13, see "Pinout Diagrams" on page 7-28). *Ref* and *AltRef* impedance values are displayed on the top row. This is the default reference mode for the Single Unit amp type.

Shared Reference Mode

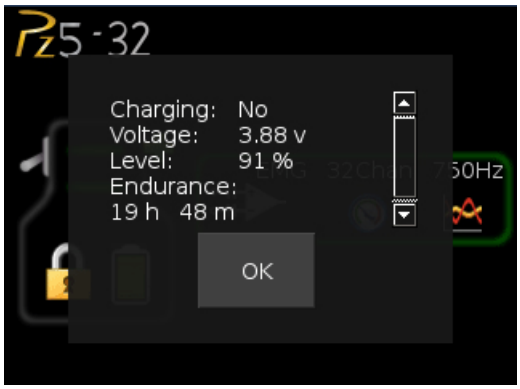
If the reference mode is Shared, the options are *Input* for all the input channels, *Ref* for the reference channel, and *Gnd* to test the ground impedance. *Ref* and *Gnd* impedance values are displayed on the top row. This is the default reference mode for the EEG and LFP amp types.

None

If the reference mode is None, the only option is *Input* for the input channels.

Battery Status

The Battery Status is displayed after touching the  Battery Status icon on the Main Configuration screen.



Information displayed includes:

Charging	Indicates if the charger is plugged into the PZ5 (Yes/No).
Voltage	Current voltage level of the battery pack.
Level	% battery life remaining.
Endurance	Estimated time of battery life remaining.

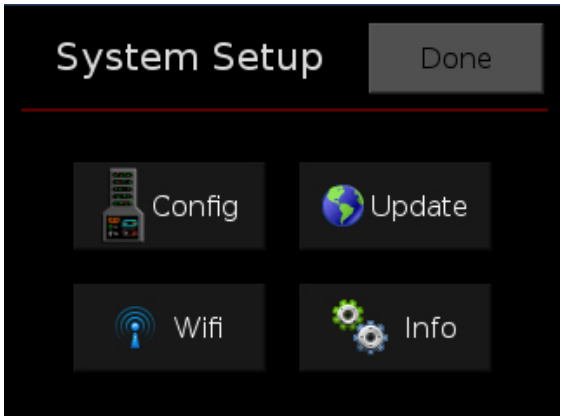
OK Button

Close Battery Status display.

Note: The Battery Level is also mirrored on the RZ2 LCD display.

System Setup Screen

The System Setup screen is displayed by touching the PZ5 logo on the top-left of the Main Configuration screen.



Settings include:

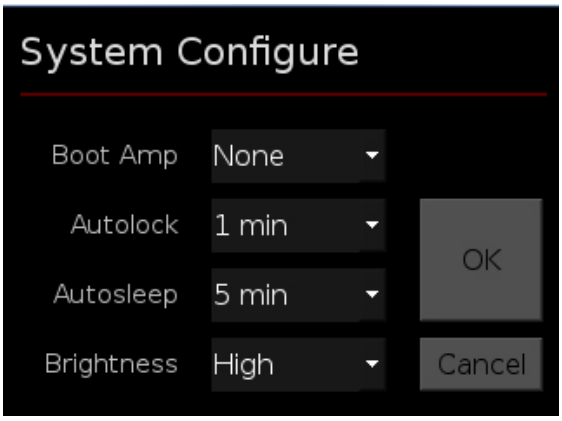
Config	Open the System Configure screen.
Update	Update onboard software over the Internet.
Wifi	Connect to a wireless network for system updates.
Info	Open the device System Info screen to view version numbers for various hardware, software and firmware components.

Done Button

Return to the Main Configuration window.

System Configure Screen

The System Configure screen is displayed by touching Config on the System Setup screen.



Settings include:

Boot Amp Select the default logical amplifier settings when the PZ5 is first powered on.

None – boots with no logical amplifiers specified.

PZ2 – all banks configured as one Single Unit amplifier.

PZ3 – all banks configured as one EEG amplifier.

PZ3 Diff – all channels configured as one EEG amplifier in differential referencing mode.

Last – reboots into the last used configuration.

Smart – Does not overwrite any existing logical amplifier configuration on boot. For example, if you configure the logical amplifiers via the PZ5_Control macro before the PZ5 boots then the PZ5 will NOT overwrite that configuration. If the PZ5 boots and NO logical amplifiers are configured it will behave the same as Last.

Autolock Select an option to lock the configuration screen after 1, 2 or 5 min of screen inactivity or select Never to turn off autolocking.

Autosleep Select an option to turn off the screen after 5, 10 or 30 min of screen inactivity or select Never to turn off autosleep.

Brightness Select High, Medium, or Low to set touchscreen brightness.

Wireless Enable/disable the wireless connection.

OK Button

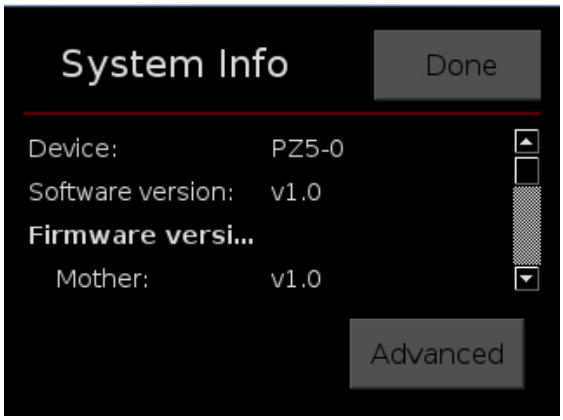
Save changes and return to the System Setup screen.

Cancel Button

Return to the System Setup screen without saving changes.

System Info Screen

The System Info screen is displayed by touching Info on the System Setup screen. Use the scroll bar to see all of the version numbers.



Information displayed includes:

Device PZ5 model number (e.g. PZ5-32).

Software version Currently installed version of onboard software.

Firmware version Currently installed version of firmware.

Hardware version Version of hardware.

Battery Date and capacity of last battery calibration (in mAhr).

Done Button

Return to the Main Configuration screen.

Advanced Button

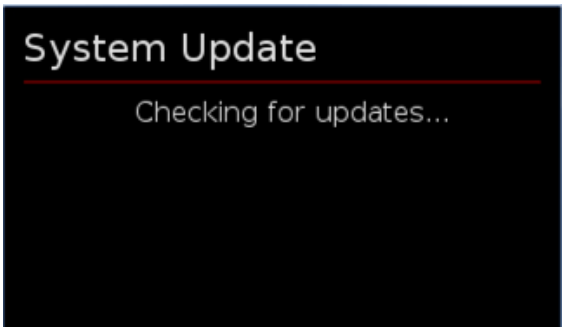
Password protected settings for TDT use only at this time.

System Update Screen

The system updater connects to a TDT server to download the latest PZ5 software and automatically update the device. This requires an active and configured Internet connection. The PZ5 provides two options for network connection: WiFi and Ethernet. The WiFi connection can be configured on the Wireless Networks screen, see below. The Ethernet port is located on the back panel.

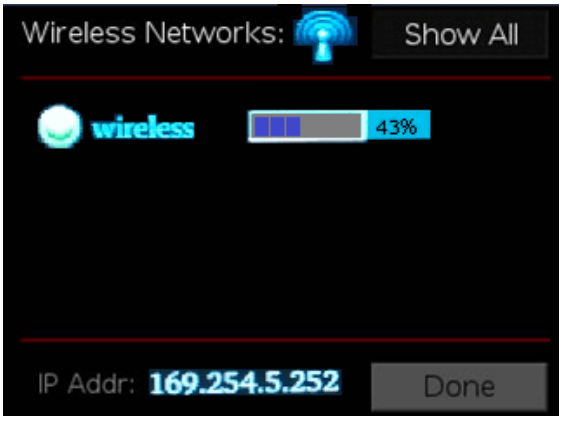
The System Update screen is displayed by touching Update on the System Setup screen.

Important! The update process can take up to an hour to complete. Make sure the PZ5 battery charger is plugged in during the update.



Wireless Networks Screen

The Wireless Networks screen is displayed by touching WiFi on the System Setup screen. Available networks that have been used or previously configured are displayed in the main area of the screen. Selecting a network from the list displays network information and enables the user to connect to the network, forget the network, or cancel configuration of the network.



The wireless icon  shows if the wireless feature is enabled or disabled. A red 'x' will appear through the icon if wireless is disabled. Enable/disable wireless through the System Configure Screen.

Show All Shows all networks, including networks that have not been previously used or configured.

IP Addr Displays current IP Address when connected to a network.

Done Button

Return to the Main Configuration screen.

PZ5 Features

Clip Warnings and Activity Display

The front panel LEDs can be used to indicate spike activity and/or clip warning for analog input channels. They can be configured under software control using the PZ5_Control macro or under manual control, using the touchscreen interface on the front of the PZ5.

LED Indicators (analog)

When enabled, LEDs for each channel are lit green to indicate activity or red to indicate a clip warning. The top row indicates the odd channels (left to right). The bottom row indicates the even channels.

Green: Activity Red: Clip Warning

Note: The LED Indicators are also mirrored on the RZ2 LCD display.

Clip Warning

Analog clipping occurs when the input signal is too large. When the input to a channel is within 3 dB of the PZ5's maximum voltage input range the LED for the corresponding channel is lit red to indicate that clipping may occur.

Activity

When configured to indicate activity, LEDs are lit green whenever a unit (spike) occurs on the corresponding channel. The sensitivity threshold for the green LED is ~200 uV.

LED Indicators (digital)

LEDs that represent digital input boards, indicate the number of input channels with each LED indicating 16 channels. For example, four LEDs indicates 64 input channels have been detected on that connection.

External Ground

The external ground is optional and should only be used in cases where the subject must occasionally make contact with a metal surface that isn't tied to the animal ground, such as a lever press. When contact is made, a ground loop is formed that temporarily adds extra noise to the system. Grounding this metal surface directly to the TDT hardware removes this ground loop at the cost of raising the overall noise floor a small amount.

A banana jack located on the back of the PZ5 provides connection to common ground. Any logical amplifier configured through the PZ5 touchscreen has this shorted by default. The PZ5_Control macro allows you to float that ground connection on individual logical amplifiers.

A cable kit is also provided to ensure cables used with the external ground are suitable for this use. Each kit includes: one male banana plug to male banana plug pass through and one male banana plug to alligator clip pass through. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

Battery Overview

The PZ5 neurodigitizer features a 32 Amp-hour Lithium ion battery pack.

Charging the Batteries

Operate the neurodigitizer with the charging cable disconnected. An external battery pack (PZ-BAT) or external charger and extra battery is available to provide longer battery life for extended recording sessions. See "PZ-BAT External Battery Pack for the PZ Amplifiers" on page 7-109 and "PZ5-BAT External Charger" on page 7-105.

PZ5 Technical Specifications

A/D	Up to 128 channels, hybrid
Maximum Voltage In	+/- 500 mV (+/- 5 mV with Intan RHD2000)
A/D Sample Rate	Up to 48828.125 Hz (adjustable in steps of approximately 750, 1500, 3000, 6000, 12000, 25000, and 50000 Hz)*
Frequency Response	*DC coupled:* 0 Hz – 0.45*Fs *AC coupled:* 0.4 Hz – 0.45*Fs With Intan RHD2000: 0.1 Hz - 10 kHz
S/N (typical)	104 dB, single unit, Fs = 25 kHz, 300-7000 Hz 116 dB, differential, Fs = 750 Hz, 0.4-300 Hz
Sample Delay	Dependent on PZ5 and RZ processor sample rates (RZ at 25 kHz)(RZ at 12 kHz) PZ5 rate — samples — samples 25 kHz — 22 — x 12 kHz — 40 — 23 6 kHz — 76 — 42 3 kHz — 141 — 79 1.5 kHz — 270 — 152 750 Hz — 543 — 295
DC offset	< +/-10 µV
Input Referred Noise	Single Ended: 3.0 µVrms, 300-7000 Hz, 25 kHz Differential: 0.75 µVrms, 0.4-300 Hz, 750 Hz
Distortion (typical)	< 1%
Input Impedance	10^9 Ohms
Battery Capacity	32 Amp-hour
Battery	8-10 hours to charge to 95% capacity, 14 hours to fully charge. Battery life between charges: 2 amp boards ~ 50 hrs 4 amp boards ~ 35 hrs 6 amp boards ~ 27 hrs 8 amp boards ~ 22 hrs
Charger	External 12V, 2.5A power supply, center negative
Indicator LEDs	Up to 128 status/clip warning/digital input channel count

Fiber Optic Cable	5 meters standard, cable lengths up to 20 meters∗∗ If longer cable lengths are required, contact TDT.
Ethernet Port	100 Mbps

∗**Note:** If recording at ~50 kHz on 128 channels, see "PZ5 Software Control" on page 7-7, for more information.

RHD2000 series amplifier boards and SPI interface cables are available from Intan Technologies.

Important! The specifications below are dependent on the amplifier board. See Intan RHD200 series website for latest, full performance specifications.

Supported Sampling Rates	750 Hz, 1.5 3, 6, 12, 25, and 50 kHz
Frequency Response	0.1 Hz - 10 kHz
Amp Input Range	+/- 5 mV
Allowable DC Offset	+/- 0.4 V

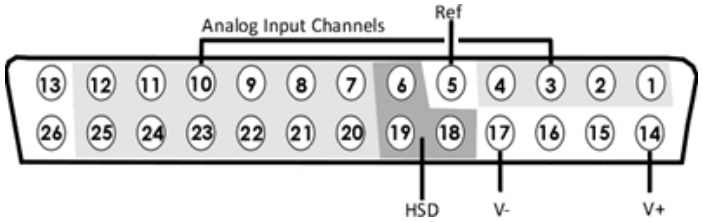
Input Connectors

PZ5 NeuroDigitizers have up to eight 26-pin headstage connectors (analog) or up to four 12-pin Omnetics nano connectors (digital) on the back of the unit. The connectors are labeled alphabetically from bottom to top. Each connector carries signal for one bank of channels with ground and reference. The corresponding channel numbers depend on 1) the reference mode configurations or number of channels in a connected digital amplifier board and 2) the position of the bank in a logical amplifier.

For simplicity sake, the diagrams below assume channels for that connector begin with channel 1. For example, A1 – A16 represent the 16 channels coming from the connected headstage. The user must increment the channel numbers by 16 (or 8) according to the mode and position of the connector. So, for the connector labeled 'A', A1 is channel 1 while on the connector labeled 'B', A1 may be channel 17.

Pinout Diagrams

Local, None or Shared Reference Mode



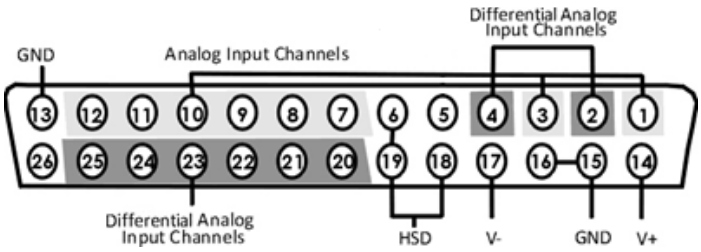
Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		14	V+	Positive Voltage (+2.5V)
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17	V-	Negative Voltage (-2.5V)
5*	Ref*	Reference*		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A5	Analog Input Channels		20	A6	Analog Input Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	^	See notes below		26	NA	Not Used

^Note: In Local reference mode, Pin 13 is AltRef. Otherwise, Pin 13 is Ground.

* In Shared reference mode, only Pin 5 of the first bank of the logical amplifier is connected. It is shared internally among the other banks of the logical amplifier.

* In None reference mode, Pin 5 is not connected.

Differential Reference Mode



Note: There are 8 (+) channels and 8 (-) channels per DB26 connector. Subsequent banks are indexed by an additional 8 channels.

Pin	Name	Description	Pin	Name	Description
1	A1 (+)	Analog Input Channel	14	V+	Positive Voltage (+2.5V)
2	A1 (-)	Differential Analog Input Channel	15	GND	Ground
3	A2 (+)	Analog Input Channel	16	GND	
4	A2 (-)	Differential Analog Input Channel	17	V-	Negative Voltage (-2.5V)
5	NA	Not Used	18	HSD	Headstage Detect
6	HSD	Headstage Detect	19	HSD	
7	A3 (+)	Analog Input Channels	20	A3 (-)	Differential Input Channels
8	A4 (+)		21	A4 (-)	
9	A5 (+)		22	A5 (-)	
10	A6 (+)		23	A6 (-)	
11	A7 (+)		24	A7 (-)	
12	A8 (+)		25	A8 (-)	
13	GND	Ground	26	NA	Not Used

Note: Contact TDT technical support (386-462-9622 or support@tdt.com) before attempting to make any custom connections.

Digital Connectors

The digital input connector is a self-aligning 12-pin Omnetics PZN-12 polarized nano connector that mates directly to an Intan RHD2000 SPI interface cable.

PZ5M Medically Isolated NeuroDigitizer

PZ5M Overview

The PZ5M is a multi-modal neurodigitizer, suitable for recording a broad range of biological potentials, combining the functionality of high and low impedance amplifiers in a single device. The device is battery operated with alternative Mains power, used primarily for charging, with full biomedical isolation for subject safety. The rack-mountable PZ5M-512 can be used for simultaneous input of EEG, EMG, LFP and Single Unit signals. It is available with 256 channels (PZ5M-256) or 512 channels (PZ5M-512).

By oversampling the signal with very fast instrumentation grade converters, TDT's custom hybrid A/D circuit yields 28 bits of resolution and unparalleled dynamic range. Optional DC coupling offers zero phase distortion across the signal bandwidth. Sampling rate and down-sampling filters can be optimized on each logical amplifier, ensuring the best possible signal fidelity for the intended input type. The +/-500 mV input range is large enough to accept any biological potential and most stimulus artifacts without saturating.

The neurodigitizer inputs are organized into multiple banks of 64 channels. Each bank is electrically isolated, meaning the ground and reference channels are not inherently shared between banks. Multiple banks can be grouped into a single logical amplifier that shares the same settings and ground/reference across each bank in the logical amplifier. There are several different referencing modes, optimizing ground and reference for different types of recording. Each logical amplifier can use the ground as a reference, use a shared reference, use a unique reference on each bank or implement full per-channel differential referencing.

A touchscreen interface provides immediate preview of inputs, impedance checking and real-time control and configuration options for each amplifier bank.

System Hardware

The PZ5M neurodigitizer accepts inputs from a variety of electrode/headstage combinations via the back-panel connectors. It includes up to eight DB80 connectors, each inputting 64 recording channels (or 32 differential channels) along with ground and reference.

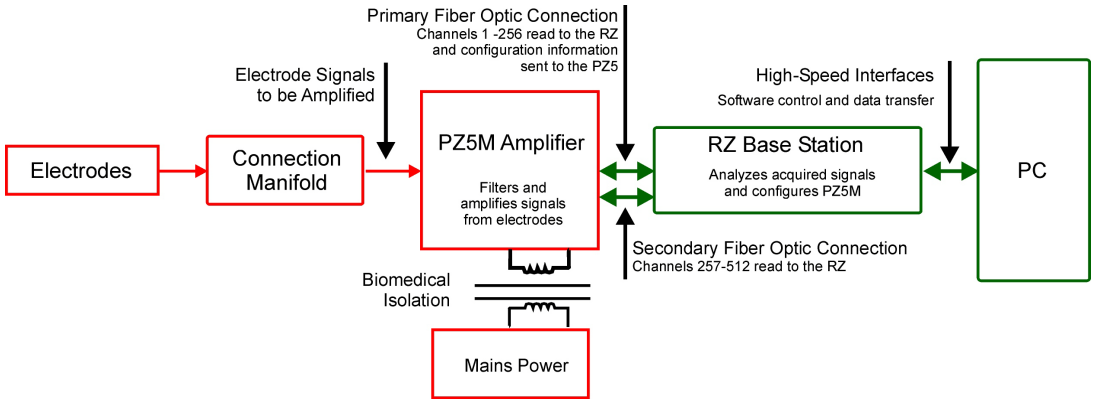
Recorded signals are amplified, digitized, and then transmitted via fiber optic connection to the RZ base station for further processing. Configuration information is also sent from the RZ to the PZ5M neurodigitizer across the same fiber optic connection. The PZ5M-512 uses two of these connections, each transferring data for up to 256 channels.

The PZ5M can connect to:

- The 'PZ' fiber optic input on an RZ2.
- Any RZDSP_P card installed in an RZ processor (includes the 'PZ' fiber optic input on an RZ5D).

A standard system configuration includes electrodes appropriate to the input signals, a connection manifold, PZ5M neurodigitizer and an RZ base station.

The diagram below illustrates this flow of data and control information through the system.



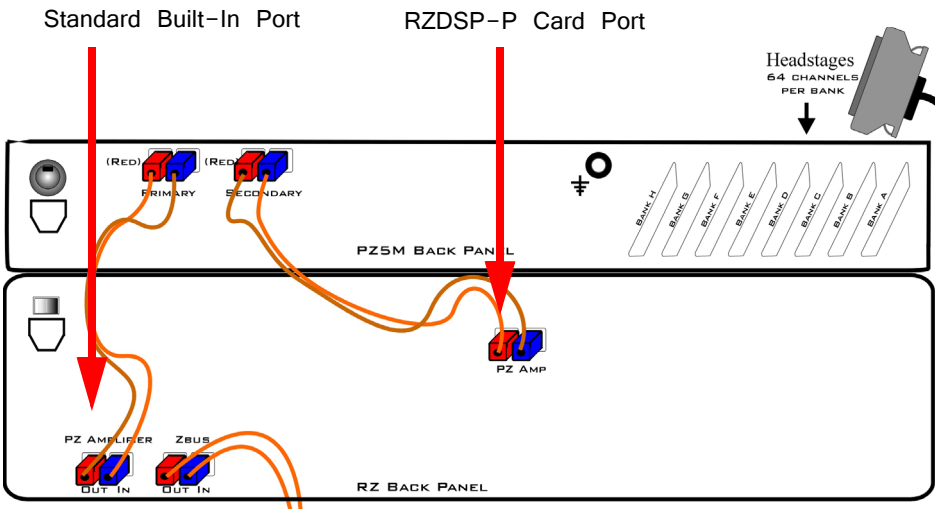
PZ5M Data and Control Flow Diagram

Hardware Setup

Up to two 5-meter paired fiber optic cables (up to 256 channels per duplex cable) are included to connect the neurodigitizer to the base station. The connectors are color coded and keyed to ensure proper connections.

The diagrams below illustrate the connections necessary for PZ5M neurodigitizer operation.

The Medically Isolated NeuroDigitizer is available with up to 512 channels. Two fiber optic ports are available on the back panel for transferring digitized channels to the RZ device. The first 256 channels are handled by the primary fiber optic port and the second 256 channels (257-512) are handled by the secondary fiber optic port. The connection to the processor can be made in a number of ways, including using the standard PZ Amp Port for the device (RZ2 shown below) and a RZDSP-P port mounted in the back panel of an RZ device. Note: The front panel optic port on the RZ5D is an RZDSP-P port.



System Connection Diagram for PZ5M-512 with RZ2

Connecting Headstages and Electrodes

Signals are input via multiple mini-DB80 connectors on the PZ5M back panel. For high impedance recordings, most users will connect to the input connectors on the PZ5M back panel using a DB80-DB26 adapter (shown below) or a connection manifold. The adapter provides direct headstage connections for up to four headstages.

DB80-DB26 adapter

For low impedance recordings, users will likely use custom cables. If using custom connectors, see "Pinout Diagrams" on page 7-53.

Powering ON/OFF

The neurodigitizer has both an onboard battery and a connection to mains power. The device can remain plugged in at all times, but the mains power on the back panel must be switched to the off position for battery operation. Regular operation is controlled by the small square power button on the face of the device.

To power on the neurodigitizer using the onboard battery:

1. Switch back panel mains power to off.
2. Press and hold the front panel power button. After one second, release the button.

   The neurodigitizer is powered on for battery for operation.

To power off onboard battery operation:

- Press and release the front panel power button.

  It may take a minute for the lights to go out.

The neurodigitizer uses mains power for charging.

To charge the neurodigitizer:

1. Ensure the power connector on the neurodigitizer back panel is connected to a mains power outlet, using the provided AC power cable.
2. Set the switch on the back panel adjacent to the power connector to the on position for charging.

   Battery lights are on when charging.

Important: If the power circuit doesn't detect the power (from power cord) when set to charge, charging is not engaged. Be sure the device is plugged in before you switch to charging.

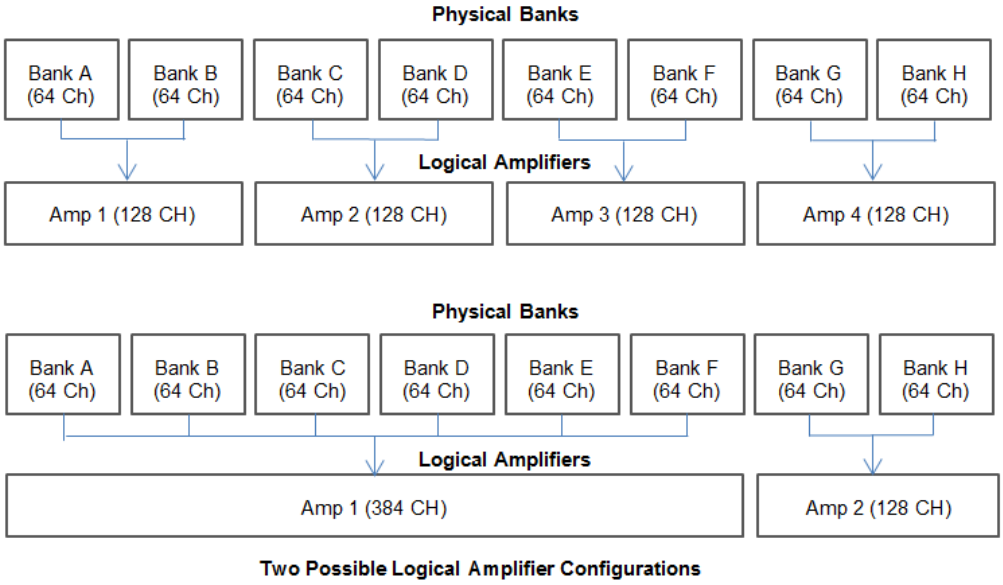
See "Power Status LEDs" on page 7-51, for more information.

Physical Amplifier

All PZ5M channels are organized into banks, with each bank corresponding to a group of 64 channels, a rear panel headstage connector (labeled alphabetically), and a front panel LED displays. Each bank is electrically isolated and can be independently configured or grouped with other banks and defined as a *logical amplifier*.

Logical Amplifiers

The PZ5M can have a maximum of four logical amplifiers. Though each bank has its own ground and reference, a single ground and reference can also be defined and shared across all banks of the logical amplifier. See "Reference Modes" below. The diagrams below show possible logical amplifier configurations.



Two Possible Logical Amplifier Configurations

Logical amplifier configurations can be defined using the PZ5M_Control macro (recommended) (see "PZ5M Software Control" on page 7-36) or the front panel interface (see "Using the PZ5M Front Panel Display" on page 7-37). If using the PZ5M_Control macro, the front panel configuration will be overwritten by information in the macro when the circuit is run.

Reference Modes

The PZ5M supports four referencing modes for each logical amplifier: Local, Shared, None and Differential. Reference and Ground configurations for each logical amplifier can be defined using the PZ5M_Control macro or via the touchscreen interface. See "Pinout Diagrams" on page 7-53, for pinout information.

Local

In Local reference mode, each group of 32 channels in a logical amplifier uses its own reference input as the reference for that bank.

Shared

In Shared mode, the reference connection of the first bank of the logical amplifier acts as a reference for all banks in the logical amplifier.

None

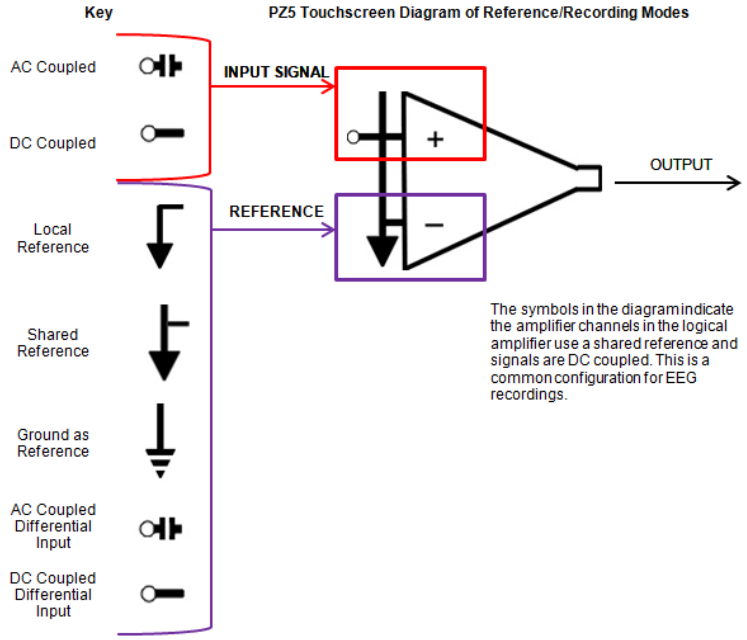
In None mode, the Ground connection is used as the reference for all banks of a logical amplifier.

Differential

In Differential mode, the inputs in each bank of the logical amplifier are paired; odd channels serve as recording (+) channels and each even channel is used as an individual reference (-) channel for the preceding odd channel.

The Signal/Reference Diagram

The PZ5M touchscreen interface uses representative diagrams to enable users to identify the configuration of the amplifier at a glance. The table below explains the parts of the diagram and what each represents.



Sampling Rate and Onboard Filters

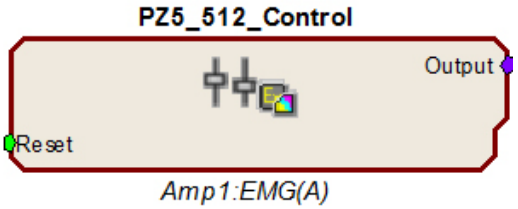
The sampling rate of each logical amplifier is adjustable (max 50 kHz, min 750 Hz) and should be set to a value appropriate for the signal of interest and the number of channels. Use the Amp Type presets as a guide for determining what sampling rate to use for each logical amplifier.

The onboard down-sampling filters are used to further reduce the noise from frequencies above the band of interest and can be set to a percentage of the sampling rate (max 45%, min 10%). Adjusting the sampling rate and filter for each logical amplifier to match your desired signal gives you the best possible signal fidelity.

Note: If recording at ~50 kHz on 128 or more channels, see "PZ5-512 Software Control", below, for additional configuration information.

PZ5M Software Control

The PZ5M_Control macro provides configuration and control of data acquisition and storage via the RCX control circuit running on the RZ base station. The PZ5M_Control macro sets the default logical amplifier configurations when the circuit first runs and retrieves waveforms/impedance values in real-time from each logical amplifier for further processing.

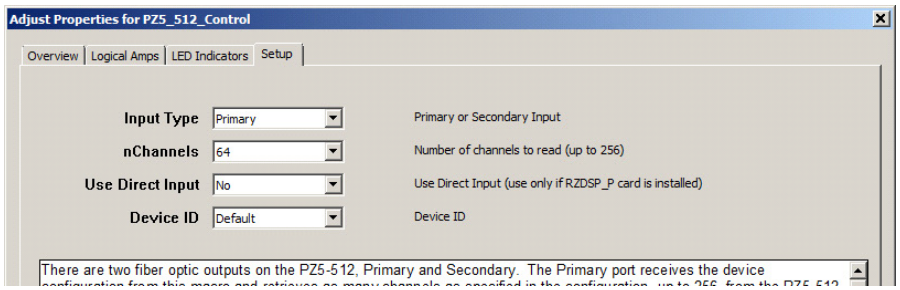


The macro configuration options are available in the macro properties dialog and can be accessed by double-clicking the macro in the RPvdsEx circuit diagram.

The macro outputs a multi-channel signal stream of the acquired signals. If the reference mode is Differential, then the 1st channel is Ch1 minus Ch2 and the second channel is Ch2 minus Ch1 and so on. The output for any logical amplifier in impedance checking mode is the channel impedance, in MΩ.

Macro Setup

The Setup tab in the macro properties dialog box must be used to provide the PZ5M with device configuration information.



Input Type. There are two fiber optic outputs on the PZ5M-512, Primary and Secondary. If recording from more than 256 channels, two PZ5M_control macros must be used. One macro must be selected as the Primary Input Type. The primary fiber optic port (channels 1 - 256) receives the logical amplifier configuration from the macro and retrieves as many channels as specified in the nChannels input, up to 256, from the PZ5M-512. The secondary port retrieves data from channels 257-512. The user must set the number of channels (nChannels) retrieved from the secondary port.

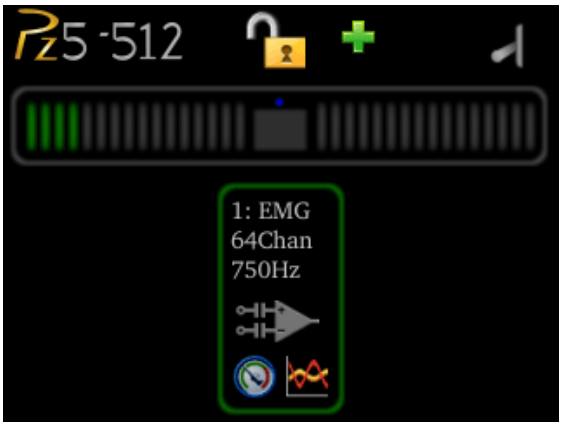
Note: Only the logical amplifier configuration specified by the Primary input is sent to the PZ5M-512.

Use Direct Input. If connecting to the back panel PZ input port on an RZ2, Use Direct Input must be set to No. In all other cases Use Direct Input must be set to Yes. If connecting to an RZDSP_P card, the PZ5M_Control macro must be assigned to the DSP occupied by the RZDSP_P card.

Using the PZ5M Front Panel Display

The front panel display is a touchscreen interface for impedance checking and waveform preview and can be used for on the fly device configuration. When the PZ5M is powered on, a splash screen is displayed on the touchscreen and a boot-up progress bar is displayed at the bottom of the screen. When the boot sequence

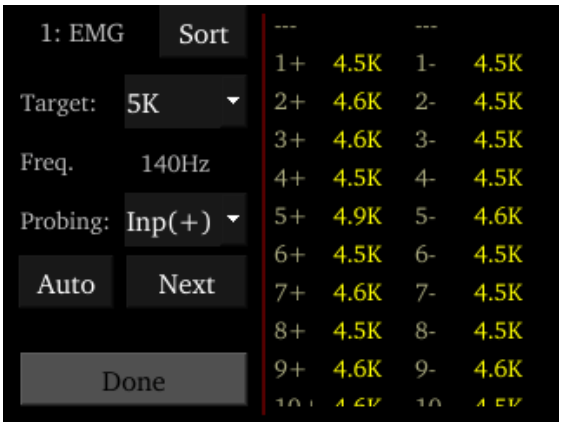
is complete, the Main Configuration screen is displayed. When the processing circuit is run on the controlling RZ device, the logical amplifier configuration defined in the PZ5M_Control macro is applied.



To test the impedance of your hardware set-up:

3. Touch the  Test icon on the desired logical amplifier.

   The Impedance Checking screen will be displayed.



4. In the **Target** field, select a target impedance value.
5. Touch the **Next** button to cycle through each probing option for the selected logical amplifier type. See “Probing Options” on page 7-46.

   The impedance values of the currently tested set are updated on the right side of the screen and are color coded for easy identification of problem channels.

   A limited set of channels is visible at any one time. Swipe vertically on the interface to scroll the visible channels or touch the Sort button to sort the list by channel number or by impedance value.

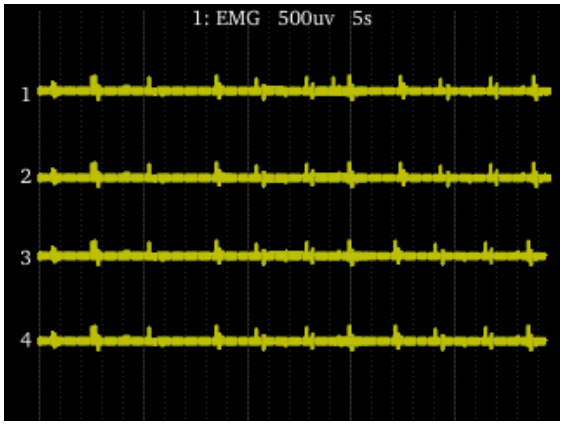
When the hardware connections have been made the incoming signals can be previewed on the front display.

To preview the data:

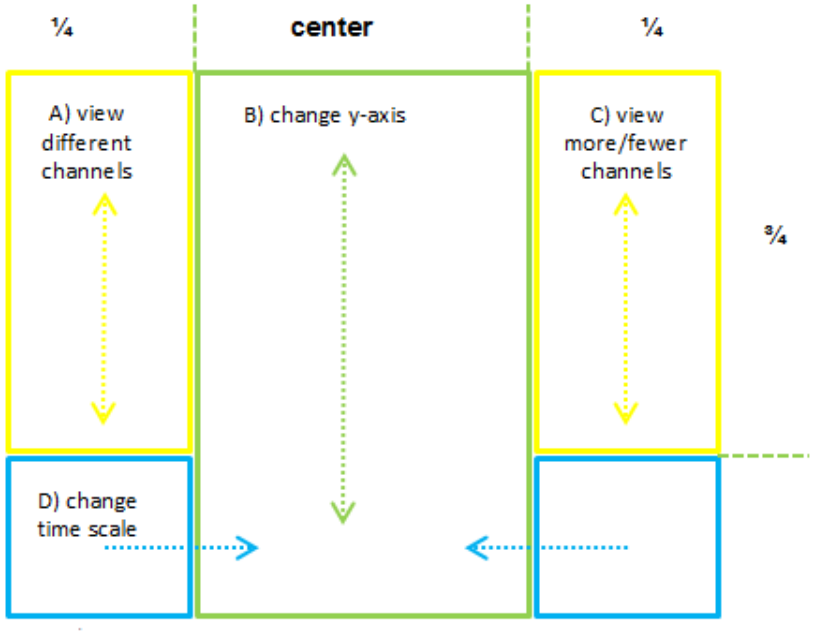
1. Touch the  **Preview** icon on the desired logical amplifier to enter the Waveform Display screen.

2. To return to the Main Configuration screen from the Waveform Display screen, swipe three fingers across the screen in any direction.

Waveform Display Screen



The Waveform Display screen is displayed by touching the  **Preview icon** on an existing logical amplifier on the Main Configuration Option screen. The plot label includes the logical amplifier number, amp type, and voltage and time scales. The displayed waveform is decimated for plotting and high pass filtered so all channels can be shown on the same scale. If the logical amplifier is DC Coupled, the DC offset is displayed as a value on the right side of each plot line (in mV). The screen view can be adjusted using touchscreen options.



To view a different subset of channels:

- Swipe up or down on the left side of the screen. (A)

To change the y-axis scale:

- Swipe up or down in the center of the screen. (B)

To view more or fewer channels:

- Swipe down or up on the right side of the screen. (C)

To change the time scale:

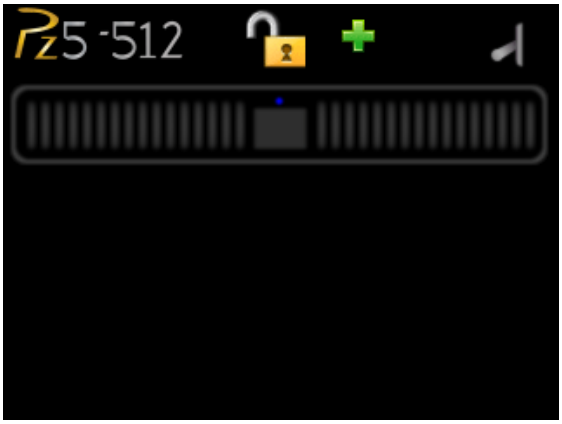
- Swipe left or right on the bottom of the screen. (D)

To return to the Main Configuration screen:

- Swipe three fingers across the screen in any direction.

The touchscreen interface can also be used to configure logical amplifiers when the PZ5M_Control is not used or for on-the-fly device configuration.

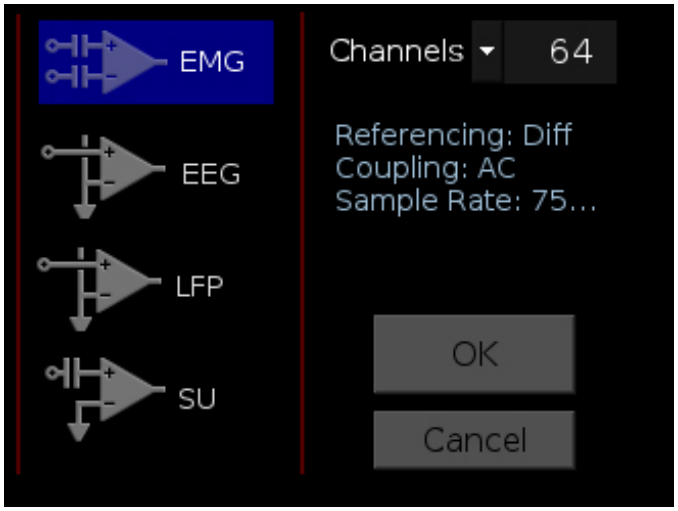
Typical Steps to Configure a Logical Amplifier Using the Touchscreen



To add a logical amplifier:

1. Touch the  **Plus Sign.**

   The Amp Type Selection screen is displayed.



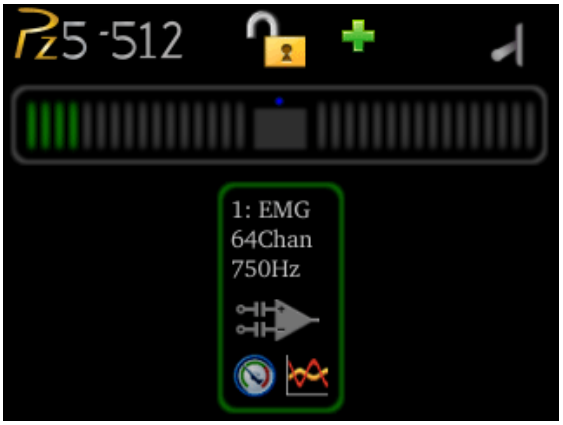
2. Touch the desired **Amp Type** icon  on the left side of the screen.

The text to the center right of the screen displays the default configuration information.

3. Touch the arrow next to **Channels** to display the drop-down list.
4. To configure the number of channels in the logical amplifier, touch the desired number in the list.
5. Touch the **OK** button.

   The Configuration Options screen is displayed.

6. Make any desired changes to the default settings then touch the **OK** button to save the selections and return to the Main Configuration screen.



   The logical amplifier is configured and a representative diagram is added to the screen.

To configure additional logical amplifiers, repeat these steps as needed.

The sections below provide additional information and serve as a reference for each screen.

Main Configuration Screen

The Main Configuration screen provides a touchscreen interface for configuring logical amplifiers and previewing waveforms in real-time. It also provides access to the PZ5M settings, such as the screen auto lock and auto sleep features, as well as tools for viewing system information, such as LED indicators, and updating the device software.

All logical amplifiers that have been defined are represented on the right side of the screen and labeled in logical order from bottom to top. For example, 2:EEG is the second logical amplifier and is configured for EEG recordings. In the illustration above, this would correspond to the back panel input connector labeled 'B'.

The main configuration screen includes the following:

Display the System Setup screen. See "System Setup Screen" on page 7-47, for more information.

ToggleToggle. LED Indicators on or off. See "Clip Warnings and Activity Display" on page 7-51, for more information.

Lock/Unlock. Lock to protect configuration settings. Unlock to allow changes to the configuration.

Plus Sign. Create a new logical amplifier. As logical amplifiers are added they appear on the Main Configuration screen.

Banks color coded to indicate current configuration of each bank.

Configuration	Color Codes
EMG	Green
EEG	Brown
LFP	Purple

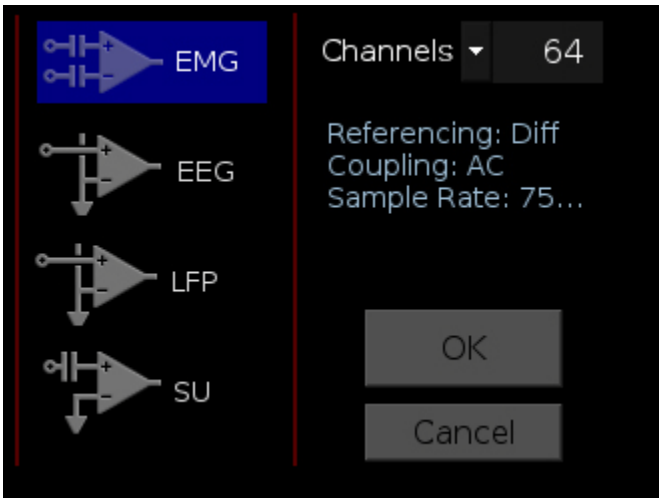
SU	Teal
Not configured	Gray

Warning: A red outline indicates the bank is configured as part of a logical amplifier but no headstage is currently detected on that bank.

Amp Type Selection Screen

The Amp Type Selection screen is displayed by touching the  Plus Sign icon on the Main Configuration screen or by touching the 

Amp Type button on the Configuration Options screen for an existing logical amplifier.



On the Amp Type Selection screen, users can set the number of channels in a logical amplifier or touch a configuration icon on the left side of the screen to select one of four amp types, each with configuration presets displayed to the right. These configuration options can be changed after the Amp Type is selected.

Options include:

Channels Drop-Down List	Select the number of channels in the logical amplifier (by banks of 16 channels).
Amp Types	

Icon	*Label*	*Defaults*
	**EMG**	Electromyography Referencing: Diff (true differential) Coupling: AC **Sample Rate: 750Hz**
	**EEG**	Electroencephalography Referencing: Shared Coupling: AC **Sample Rate: 750Hz**
	**LFP**	Local Field Potentials Referencing: Shared Coupling: AC **Sample Rate: 3kHz**
	**SU**	Single Unit Referencing: Local Coupling: AC **Sample Rate: 25kHz**

OK Button

Save selections and open the Configuration Options screen.

Delete Button

Delete the logical amplifier and display a confirmation screen before returning to the Main Configuration screen.

Note: Only available after a logical amplifier has already been created.

Cancel Button

Return to Main Configuration screen without making changes.

Configuration Options Screen

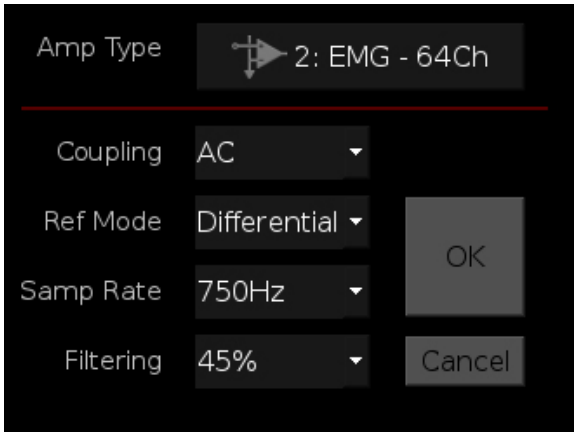
The Configuration Options screen is displayed after selecting the Amp Type when adding a new logical amplifier or it can be displayed by touching the  configuration icon on an existing logical amplifier on the Main Configuration Option screen.

Amp Type Button

The area at the top of the screen displays the Amp Type for the selected/new logical amplifier and includes the logical amplifier number, configuration type and number of channels.

To return to the Amp Type Selection screen:

- Touch the **Amp Type** button.



Each Amp Type includes preset values for each setting. The Configuration Options screen enables users to modify these settings.

Settings include:

Coupling Choose AC or DC. AC coupling implements a high pass filter with ~ 0.4 Hz cutoff frequency.

Ref Mode (Reference Mode) Choose Local, Shared, None, or Differential (Individual). See "Reference Modes" on page 7-35, for more information on reference modes.

Samp Rate (Sampling Rate) Choose a sampling rate from a list of values: 750 Hz, 1.5 kHz, 3 kHz, 6 kHz, 12 kHz, 25 kHz, 50 kHz.

Filtering Select a cutoff frequency for the anti-aliasing filter, as a percentage of the sampling rate. Choose from a list of values: 45%, 35%, 25%, 15%, or 10%.

OK Button

Save selections and return to Main Configuration screen.

Cancel Button

Return to Main Configuration screen without making changes.

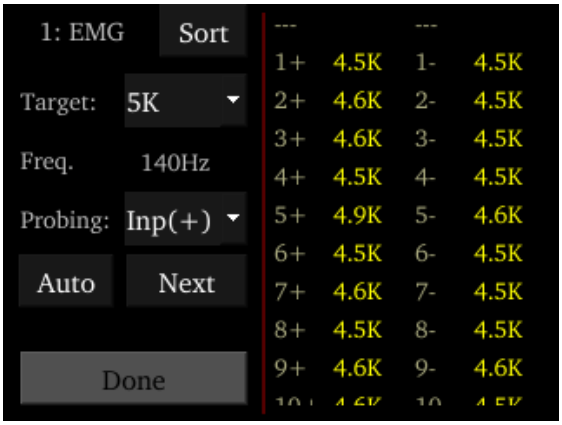
Impedance Checking Screen

The Impedance Checking Screen is displayed by touching the **Test** icon on an existing logical amplifier on the Main Configuration screen. The logical amplifier number and amp type are displayed in the top-left corner, for example 1:EEG.

Select the type of connections to measure (Probing options) and choose a target impedance value (Target) to color code the measured impedance value text. During impedance checking, all connections in the selected set are tested in parallel and the impedance is measured relative to the user-defined target impedance (1 kΩ – 100 kΩ). The impedance values of the currently tested set are updated on the right side of the screen. Toggle the Sort button to sort the list by channel number or by impedance value.

A limited set of channels are visible at any one time. Swipe vertically on the touchscreen to scroll the visible channels.

Important!: The impedance checking feature of the PZ5M can and should only be used with a passive headstage or direct connection to the electrodes.



Settings include:

Target — Select the target impedance from a drop down list (1 kΩ-100 kΩ). This is used to color the impedance value text during/after probing. Impedance values above the target are colored red, values <75% below the target are green and all other values are yellow.

Freq. — Set the probe signal frequency from a drop down list. The frequency is adjustable from 35Hz, 70Hz, 140Hz, 280Hz, 560Hz, 1120Hz, and 2240Hz.

Probing — Select the set of connections to measure. The available options in this list change depending on the logical amp referencing mode. See "Probing Options" below.

Sort Button — Toggle button that displays the channels with the largest variation from the target impedance at the top of the screen.

Auto Button — Toggle button to cycle through each probing option every second.

Next Button — Select to advance to the next probing option set.

Done Button

Return to Main Configuration screen.

Probing Options

The referencing mode of the currently selected logical amplifier determines the available Probing options.

Differential Reference Mode

If the reference mode is Differential, the Probing options are *Inp(+)* for the positive input channels and *Inp(-)* for the differential channels. This is the default reference mode for the EMG amp type.

Local Reference Mode

If the reference mode is Local, the options are *Input* for all the input channels, *Ref* to test the reference impedance to ground, or *AltRef* to test the alternative reference (see "Pinout Diagrams" on page 7-53. Ref and AltRef impedance values are displayed on the top row. This is the default reference mode for the SU amp type.

Shared Reference Mode

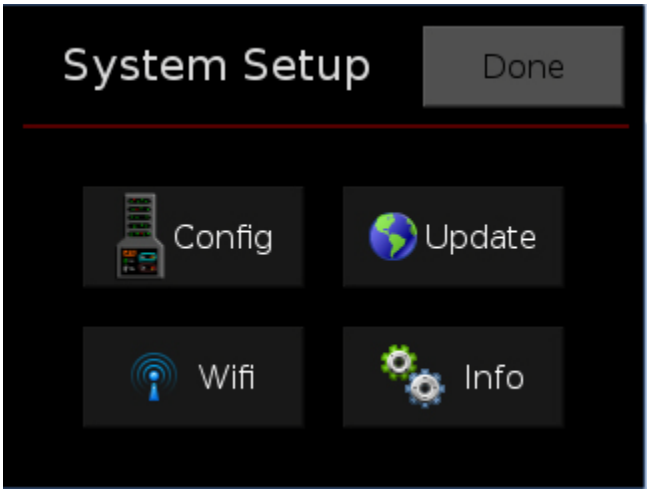
If the reference mode is Shared, the options are *Input* for all the input channels, *Ref* for the reference channel, and *Gnd* to test the ground impedance. *Ref* and *Gnd* impedance values are displayed on the top row. This is the default reference mode for the EEG and LFP amp types.

None

If the reference mode is *None*, the only option is Input for the input channels.

System Setup Screen

The System Setup screen is displayed by touching the PZ5M logo on the top-left of the Main Configuration screen.



Options include:

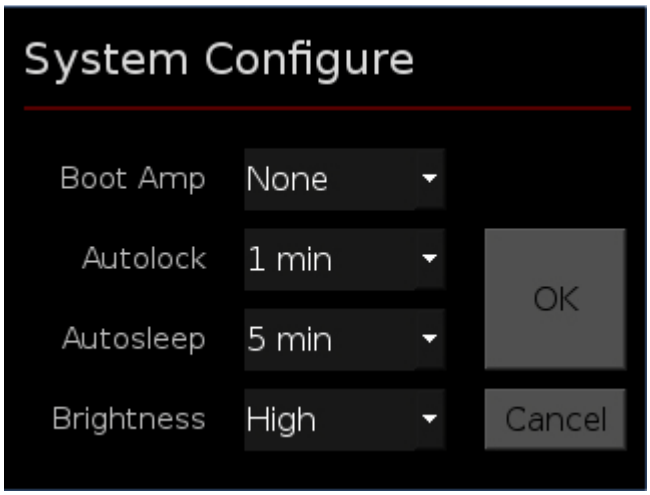
Config	Open the System Configure screen.
Update	Update onboard software over the Internet.
Wifi	Connect to a wireless network for system updates.
Info	Open the device System Info screen to view version numbers for various hardware, software and firmware components.

Done Button

Return to the Main Configuration window.

System Configure Screen

The System Configure screen is displayed by touching Config on the System Setup screen.



Settings include:

Boot Amp Select the default logical amplifier settings when the PZ5M is first powered on.

None – boots with no logical amplifiers specified.

PZ2 – all banks configured as one Single Unit amplifier.

PZ3 – all banks configured as one EEG amplifier.

PZ3 Diff – all channels configured as one EEG amplifier in differential referencing mode.

Last – reboots into the last used configuration.

Smart – Does not overwrite any existing logical amplifier configuration on boot. For example, if you configure the logical amplifiers via the PZ5M_Control macro before the PZ5M boots then the PZ5M will NOT overwrite that configuration. If the PZ5M boots and NO logical amplifiers are configured it will behave the same as Last.

Autolock Select an option to lock the configuration screen after 1, 2 or 5 min of screen inactivity or select Never to turn off autolocking.

Autosleep Select an option to turn off the screen after 5, 10 or 30 min of screen inactivity or select Never to turn off autosleep.

Brightness Select High, Medium, or Low to set touchscreen brightness.

Wireless Enable/disable the wireless connection.

OK Button

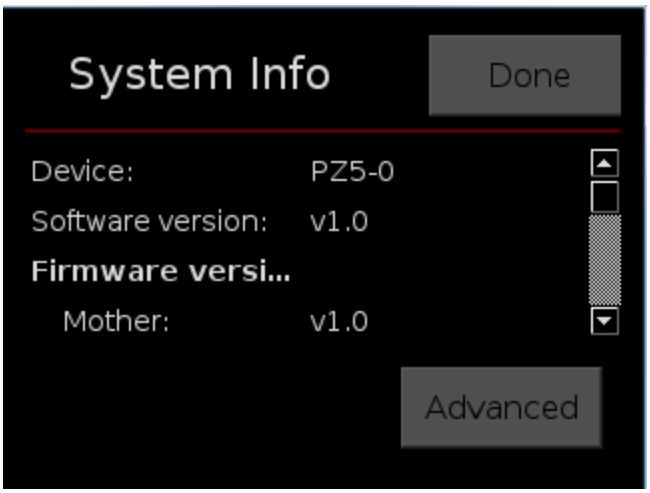
Save changes and return to the System Setup screen.

Cancel Button

Return to the System Setup screen without saving changes.

System Info Screen

The System Info screen is displayed by touching Info on the System Setup screen. Use the scroll bar to see all of the version numbers.



Information displayed includes:

Device	PZ5M model number.
Software version	Currently installed version of onboard software.
Firmware version	Currently installed version of firmware.
Hardware version	Version of hardware.
Battery	Not used.

Done Button

Return to the Main Configuration screen.

Advanced Button

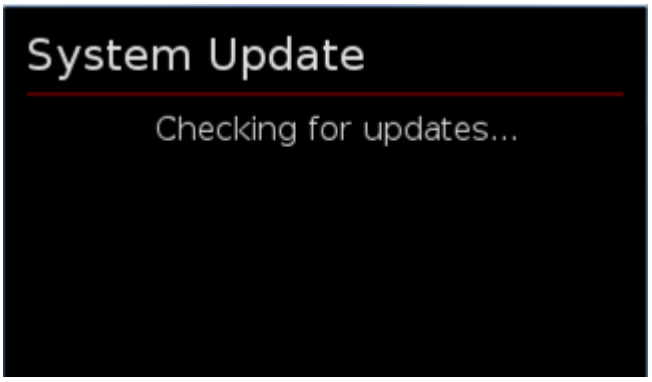
Password protected settings for TDT use only at this time.

System Update Screen

The system updater connects to a TDT server to download the latest PZ5M software and automatically update the device. This requires an active and configured Internet connection. The PZ5M provides two options for network connection: Wifi and Ethernet. The Wifi connection can be configured on the Wireless Networks screen, see below. The Ethernet port is located on the back panel.

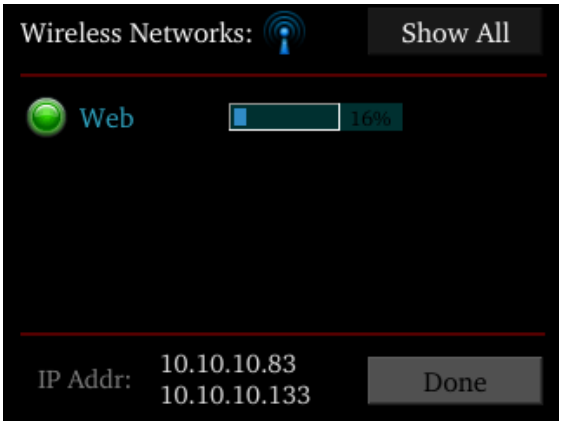
The System Update screen is displayed by touching Update on the System Setup screen.

Note: The update process can take up to an hour to complete.



Wireless Networks Screen

The Wireless Networks screen is displayed by touching Wifi on the System Setup screen. Available networks that have been used or previously configured are displayed in the main area of the screen. Selecting a network from the list displays network information and enables the user to connect to the network, forget the network, or cancel configuration of the network.



The wireless icon  shows if the wireless feature is enabled or disabled. A red 'x' will appear through the icon if wireless is disabled. Enable/disable wireless through the System Configure Screen.

Show All

Shows all networks, including networks that have not been previously used or configured.

IP Addr

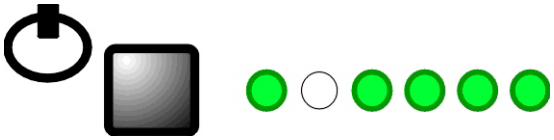
Displays current IP Address when connected to a network.

Done Button

Return to the Main Configuration screen.

PZ5M Features

Power Status LEDs



A battery power button located above the front panel touchscreen interface turns on/off battery power and the adjacent row of small LEDs reports power type and level. The first LED (from left) indicates whether the devices is being powered from mains or batter power.

LED Color	Status
Green	the device is using mains power and the battery is charging.
Red	the device is using battery power.

To use battery power, turn off Mains power using the switch on the back panel.

The four LEDs on the right end of the row indicate the power level of the battery.

# of LED's Lit	Battery Power Level
4	Fully charged
3-2	Not fully charged
1	Critically low, charge immediately

The LED between the Power Mode LED and the Power Level LEDs is not used at this time.

Battery Operation and Charging

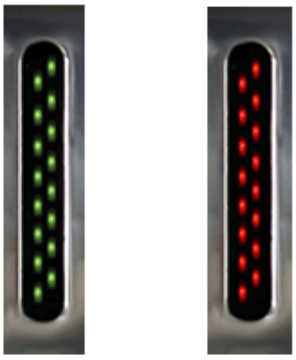
The digitizer has an onboard, 240 Wh battery for device operation. The battery charges whenever the Mains power is connected and the Mains power switch is in the on position. The battery power button may be on or off.

Clip Warnings and Activity Display

The front panel LEDs can be used to indicate spike activity and/or clip warning. They can be configured under software control using the PZ5M_Control macro or under manual control, using the touchscreen interface on the front of the PZ5M.

LED Indicators

When enabled, LEDs for each channel are lit green to indicate activity or red to indicate a clip warning. The left row indicates the odd channels bottom to top. The right row indicates the even channels.



Green: Activity Red: Clip Warning

Clip Warning

Analog clipping occurs when the input signal is too large. When the input to a channel is within 3 dB of the PZ5M's maximum input range the LED for the corresponding channel is lit red to indicate that clipping may occur.

Activity

When configured to indicate activity, LEDs are lit green whenever a unit (spike) occurs on the corresponding channel. The sensitivity threshold for the green LED is ~200 uV.

Note: The LED Indicators are also mirrored on the RZ2 LCD display.

External Ground

The external ground is optional and should only be used in cases where the subject must occasionally make contact with a metal surface that isn't tied to the animal ground, such as a lever press. When contact is made, a ground loop is formed that temporarily adds extra noise to the system. Grounding this metal surface directly to the TDT hardware removes this ground loop at the cost of raising the overall noise floor a small amount.

A banana jack located on the back of the PZ5M provides connection to common ground. Any logical amplifier configured through the PZ5M touchscreen has this shorted by default. The PZ5M_Control macro allows you to float that ground connection on individual logical amplifiers.

A cable kit is also provided to ensure cables used with the external ground are suitable for this use. Each kit includes: one male banana plug to male banana plug pass through and one male banana plug to alligator clip pass through. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

PZ5M Technical Specifications

A/D	Up to 512 channels, hybrid
Maximum Voltage In	+/- 500 mV
A/D Sample Rate	Up to 48828.125 Hz (adjustable in steps of approximately 750, 1500, 3000, 6000, 12000, 25000, and 50000 Hz)*
Frequency Response	DC coupled: 0 Hz – 0.45*Fs AC coupled: 0.4 Hz – 0.45*Fs
S/N (typical)	104 dB, single unit, Fs = 25 kHz, 300-7000 Hz 116 dB, differential, Fs = 750 Hz, 0.4-300 Hz
DC offset	< +/-10 µV
Input Referred Noise	Single Unit: 3.0 µVrms, 300-7000 Hz, 25 kHz Differential: 0.75 µVrms, 0.4-300 Hz, 750 Hz
Distortion (typical)	< 1%
Input Impedance	10^9 Ohms
Indicator LEDs	Up to 512 status/clip warning
Fiber Optic Cable	5 meters standard (2), cable lengths up to 20 meters **Note:** If longer cable lengths are required, contact TDT.
Ethernet Port	100 Mbps
Battery	240 Wh 20 hours to fully charge 16-18 hours to charge to 95% capacity 5.5 hours between charges (with every bank active)

*Note: If recording at ~50 kHz on 128 channels, see "PZ5M Software Control" on page 7-36, for more information.

Input Connectors

PZ5M NeuroDigitizers has up to eight headstage connectors on the back of the unit. Each connector carries input signals and some combination of ground(s) and reference(s).

Pinout Diagrams

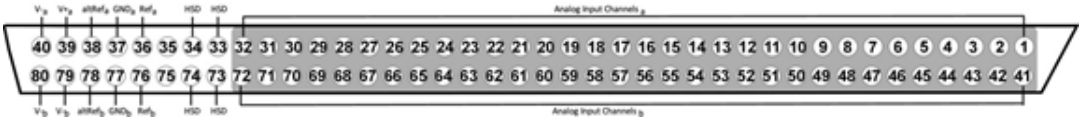
The PZ5M connectors are labeled alphabetically from right to left. The corresponding channel numbers depend on 1) the reference mode configuration and 2) the position of the bank in a logical amplifier.

For simplicity sake, the diagrams below assume channels for that connector begin with channel 1. For example, in the first pinout below A1 – A32 represent the first

32 channels coming from the headstage connected to the mini-DB80. Channels numbers should be incremented according to connection position.

The left and right row on each connector is electrically separate, but represents a single block of channels that can be defined as a logical amplifier or as part of a larger logical amplifier. As a result, ground and references are duplicated for left(a) and right(b) rows.

Local, None or Shared Reference Mode



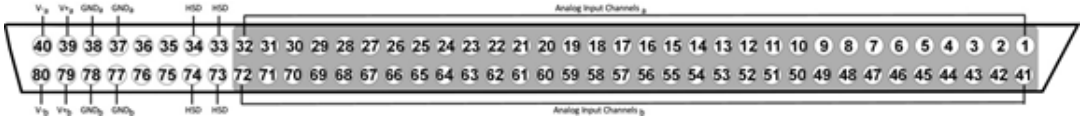
Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels (1-32)		41	A33	Analog Input Channels (33-64)
2	A2			42	A34	
. . .	. . .			. . .	. . .	
31	A31			71	A63	
32	A32			72	A64	
33	HSD	Headstage Detect		73	HSD	Headstage Detect
34	HSD	Headstage Detect		74	HSD	Headstage Detect
35	NA	Not Used		75	NA	Not Used
36	Refa	Reference for ch1-32		76	Refb	Reference for ch33-64
37	GNDa	Ground for ch1-32		77	GNDb	Ground for ch33-64
38	^	See notes below		78	^	See notes below
39	V+a	Positive Voltage		79	V+b	Positive Voltage
40	V-a	Negative Voltage		80	V-b	Negative Voltage

^Note: In Local reference mode, Pin 38 is AltRefa and Pin 78 is AltRefB. Otherwise, Pin 38 is GNDa and Pin 78 is GNDb.

* In Shared reference mode, only Pin 36 of the first bank of the logical amplifier is connected. It is shared internally among the other banks of the logical amplifier.

* In None reference mode, Pin 36 and Pin 76 are not connected.

Differential Reference Mode



Note: There are 32 (+) channels and 32 (-) channels per mini-DB80 connector. Subsequent banks are indexed by an additional 32 channels.

Pin	Name	Description		Pin	Name	Description
1	A1(+)	Analog Input Channels (1-16)		41	A17(+)	Analog Input Channels (17-32)
2	A1(-)			42	A17(-)	
3	A2(+)			43	A18(+)	
4	A2(-)			44	A18(-)	
. . .	. . .			. . .	. . .	
29	A15(+)			69	A31(+)	
30	A15(-)			70	A31(-)	
31	A16(+)			71	A32(+)	
32	A16(-)			72	A32(-)	
33	HSD	Headstage Detect		73	HSD	Headstage Detect
34	HSD	Headstage Detect		74	HSD	Headstage Detect
35	NA	Not Used		75	NA	Not Used
36	NA	Not Used		76	NA	Not Used
37	GNDa	Ground for ch1-32		77	GNDb	Ground for ch33-64
38	GNDa	Ground for ch1-32		78	GNDb	Ground for ch33-64
39	V+a	Positive Voltage		79	V+b	Positive Voltage
40	V-a	Negative Voltage		80	V-b	Negative Voltage

Note: Contact TDT technical support (+1 386-462-9622 or support@tdt.com) before attempting to make any custom connections.

Special Note: ***Recording 128 Channels or more at 50 kHz (rare)***

Due to the PZ5M's high bit resolution and DC recording capabilities, data should always be stored as 32-bit floating point. However, the bandwidth of the system is limited by the optical interface when streaming high channel counts at high speed. As a result high channel count, high speed data must be stored in Short format.

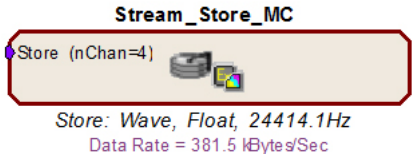
The limits for each optical interface (to PC, to DSP-S, to DSP-U) are:

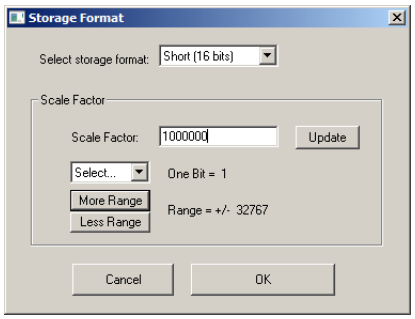
256 channels or more at 25 kHz = data storage limited to 16 bit (short) format

128 channels or more 50 kHz = data storage limited to 16 bit (short) format

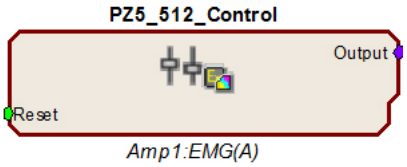
When using Short format, the data will be scaled and converted into an integer before storage. This narrows the dynamic range of the acquired signals and all DC offsets must be removed before the data is stored. You can either filter out the DC offset with a NeuroFilter or HP-LP_Filter_MC macro, or use AC coupling on the logical amplifier if you are storing the raw signal direct from the PZ5M.

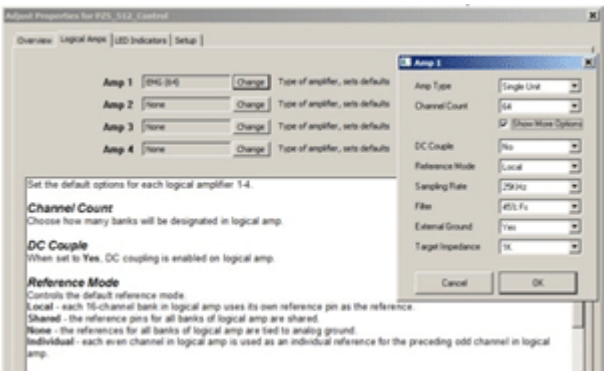
The data storage format is configured via a stream store macro in the RCX control circuit running on the RZ base station, such as Stream_Store_MC and Stream_Store_MC2 if writing into a data tank, and Stream_Server_MC or Stream_Remote_MC if streaming to an RS4 or PO8e. The configuration options are available in the macro properties dialog and can be accessed by double-clicking the macro in the RPvdsEx circuit diagram, then clicking the Store Format button on the Options tab.





AC coupling can be set using the touch screen configuration options or on the Logical Amp tab of the PZ5M_Control macro properties dialog.





These changes are required only when recording 128 channels at 50 kHz. In every other case, the Float (32 bits) format should be used to utilize the full bit resolution of the PZ5M.

PZ2 PreAmp

PZ2 Overview

The PZ2 is a high channel count preamplifier suitable for extracellular recordings. The PZ2 preamplifier features a custom 18-bit hybrid A/D architecture that offers the advantages of Sigma-Delta converters at significantly lower power and a fast fiber optic connection capable of simultaneously transferring up to 256 channels. The extended bandwidth offered by this connection supports sampling rates up to ~50 kHz and improves signal fidelity, spike discrimination, sorting, and analysis. Used exclusively with Z-Series base stations, PZ2 preamplifiers are available in 32, 64, 96, 128, or 256-channel models.

Note: When sampling at a rate of ~50 kHz only the first 128 amplifier channels will be available.

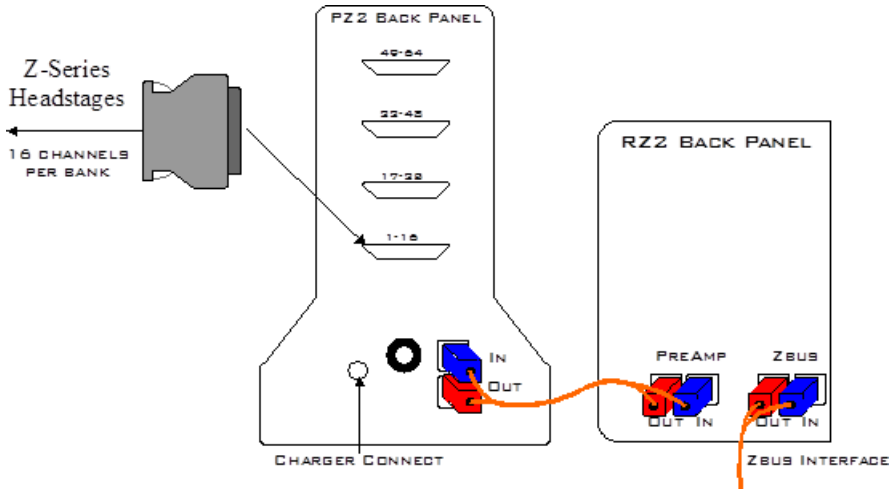
System Hardware

All PZ2 channels are organized into groups of 16 channel **banks** with each bank corresponding to a rear panel headstage connector and front panel LED display. Recorded signals are digitized, amplified, and transmitted to the RZ2 base station via a single fiber optic connection for further processing. In addition, configuration information is sent from the RZ2 to the PZ2 preamplifier across the fiber optic connection.

A standard configuration for neurophysiology recordings includes electrodes (chronic or acute), one or more Z-Series high impedance headstages, a PZ2 preamplifier, and an RZ2 base station.

Hardware Set-up

The diagram below illustrates the connections necessary for PZ2 preamplifier operation.



One or more Z-Series headstages can be connected to the input connectors on the PZ2 back panel. A 5-meter paired fiber optic cable is included to connect the preamplifier to the base station. The connectors are color coded and keyed to ensure proper connections. The PZ2 battery charger connects to the round female connector located on the back panel of the PZ2 preamplifier.

Important! To avoid introducing EMF noise, DO NOT connect the charger to the PZ2 while collecting data.

Powering ON

To turn the preamplifier on, move the three position battery switch located on the front panel of the PZ2, to either the Bat-A or Bat-B position.

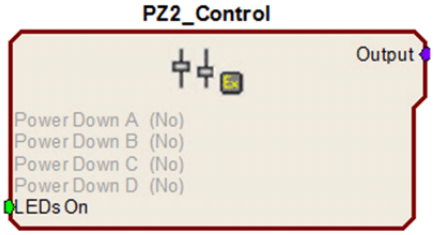
Powering OFF

To turn the preamplifier off, move the three position battery switch located on the front panel of the PZ2, to the OFF position.

Important! Channels are grouped by 16-channel banks and each bank will only power up when a headstage is connected. This design helps to increase battery life.

PZ2 Software Control

The preamplifier's hardware operation (power options and indicator LEDs) can be configured using the PZ2_Control macro within the RPvdsEx control circuits running on the RZ2 base station.



Double-clicking the macro in RPvdsEx displays the macro properties and allows users to easily configure the macro. Additional information on using the macro is available in the macro properties dialog box.

This macro is not required for preamplifier operation but is recommended if the user requires more control over the amplifier power/up or power/down status or front panel LEDs. See the relevant sections below for more information about these features.

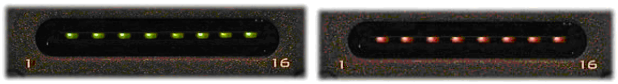
PZ2 Features

Clip Warnings and Activity Display

256 front panel LEDs can be used to indicate spike activity and/or clip warning depending on display mode and configuration. See "Display Button" and "Status LED" below for more information.

Recording Channel LEDs

When enabled, LEDs for each channel may be lit green to indicate activity or red to indicate a clip warning.



Green: Activity | Red: Clip Warning

Clip Warning	When the input to a channel is greater than -3dB from the preamplifier's maximum voltage input the LED for the corresponding channel is lit red indicating clipping may occur.
Activity	Whenever a unit (spike) occurs (the sensitivity threshold can be configured with the PZ2_Control macro) the LED for the corresponding channel is lit green.

Note: The LED Indicators are also mirrored on the RZ2 LCD display.

Display Button

The Display button located on the front panel of the PZ2 toggles the clip warning and activity display LEDs between software control and standard operation.

To toggle between display modes:

- Press the **Display** button.

Status LED

When recording, the status LED located below the Display button indicates the current display mode of the LED Indicators.

Green	Software Control of LEDs Use the PZ2_Control macro to configure LED Indicators. LEDs are turned off until enabled through software control.
Orange	LEDs enabled for standard operation

In this mode, LEDs are automatically enabled for default activity and clip warning display as described above.

External Ground

The external ground is optional and should only be used in cases where the subject must occasionally make contact with a metal surface that isn't tied to the animal ground, such as a lever press. When contact is made, a ground loop is formed that temporarily adds extra noise to the system. Grounding this metal surface directly to the TDT hardware removes this ground loop at the cost of raising the overall noise floor a small amount.

A banana jack located on the back of the PZ2 (directly to the right of the charger input) provides connections to common ground for the first bank of channels (1-16). A cable kit is also provided to ensure cables used with the external ground are suitable for this use. Each kit includes: one male banana plug to male banana plug pass through and one male banana plug to alligator clip pass through. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

Battery Overview

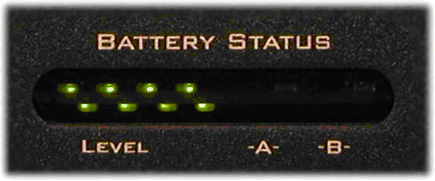
The PZ2 preamplifier features two Lithium ion batteries to allow for longer record times. A three-position switch selects the active battery between Bank-A, Bank-B, or both banks off.

Maximizing Battery Life

To increase battery life, individual banks of channels will only power up when a headstage is connected to the corresponding input.

The PZ2_Control macro can also be added to the circuit running on the RZ2 to further specify how PZ2 channel banks are powered. When a headstage is connected, banks may be powered on or off statically through the **Power Control** options within the macro or dynamically by using the **PZ2_Control** macro inputs. See the internal macro help for more information.

Battery Status LEDs



Battery Level: Eight LEDs indicate the voltage level of the selected battery. These LEDs can be found on the front of the PZ2 preamplifier by the heading Level. When the battery is fully charged, all eight LEDs will light green. When the battery voltage is low, only one green LED will be lit. If the voltage is allowed to drop further, the

last LED will flash red. TDT recommends charging the battery before this flashing low-voltage indicator comes on. While charging, the Level LEDs will flash green.

Status	Description
8 Green	Fully Charged
1 Green, 7 Unlit	Low Voltage
1 Flashing Red	Low Voltage - Charge Immediately!
8 Green Flashing	Charging in Progress

Charging the Batteries

Operate the preamplifier with the charging cable disconnected. Connecting the PZ2 charger will simultaneously charge both batteries. TDT recommends putting the three-position switch in the **OFF** (middle) position while charging the PZ2.

Charging Indicators

When powered on, the PZ2 battery status LEDs are also used for each battery to indicate which battery, if any, is charging. These LEDs are found next to the Level LEDs by the headings -A- and -B-. A green indicator denotes the battery bank is fully charged while a red indicator designates the battery is currently charging. When the device is in operation (charger is not connected) the -A- and -B- LEDs are not lit.

Status	Description
Red	Charging
Green	Fully Charged
Unlit	Operation Mode (charger not connected)

An external battery pack is also available to provide longer battery life for extended recording sessions. See "PZ-BAT External Battery Pack for the PZ Amplifiers" on page 7-109.

PZ2 Technical Specifications

A/D	Up to 256 channels, 18-bit hybrid
Maximum Voltage In	+/- 10 mV
Frequency Response	3 dB: 0.35 Hz – 7.5 kHz 6 dB: 0.2 Hz – 8.5 kHz
Anti-Aliasing Filter	4th order Lowpass (24 dB per octave)
S/N (typical)	73 dB

Distortion (typical)	< 1%
A/D Sample Rate	Up to 48828.125 Hz*
Sample Delay	Dependent on Sample Rate and RPvdsEx input method **Rate** / **Pipe Input** / **MC Input** 6 kHz / 16 samples / 15 samples 12 kHz / 17 samples / 16 samples 25 kHz / 20 samples / 19 samples 50 kHz / 26 samples / 25 samples
Input Impedance	10^5 Ohms
Power Requirements	2 Lithium Ion cells at 10 AmpHours each
Battery	Eight hours to charge both cells Battery life between charges, per cell: 32 ch ~ 13 hrs 64 ch ~ 11 hrs 96 ch ~ 9.5 hrs 128 ch ~ 8 hrs 256 ch ~ 5 hrs
Charger	External 6 V, 3 A power supply
Indicator LEDs	Up to 256 status or clip warning, battery life, active battery bank
Input referred noise	2 µV rms typical 300- 7000 Hz, 8 µV peak typical
Fiber Optic Cable	5 meters standard, cable lengths up to 20 meters**

*Note: When sampling at a rate of 48.828 kHz the PZ2 preamplifier is limited to a maximum of 128 channels.

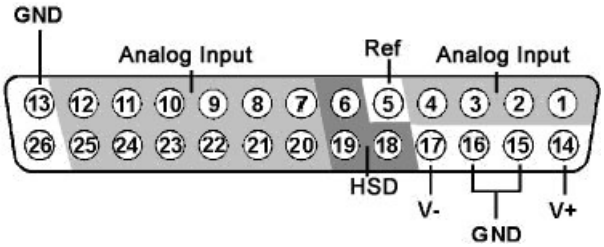
**Note: If longer cable lengths are required, contact TDT.

Input Connectors

PZ2 Preamplifiers have up to 16, 26-pin headstage connectors on the back of the unit. A1 – A16 represent the 16 channels coming from each connected headstage. The PZ2 channels are marked next to the respective connector on the preamplifier. So, for the connector for channel 1 – 16, A1 is channel 1 while on the connector for channels 17 – 32, A1 is channel 17.

Important! Each input connector uses its own unique ground and reference. When using multiple headstages, ground pins on all headstages should be connected together to form a single common ground. See "Headstage Connection Guide" on page 7-97.

Pinout Diagram



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		14	V+	Positive Voltage (+1.5V)
2	A2			15	GND	Ground
3	A3			16	GND	
4	A4			17	V-	Negative Voltage (-1.5V)
5	Ref	Reference		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A5	Analog Input Channels		20	A6	Analog Input Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	GND	Ground		26	NA	Not Used

Note: TDT technical support (386-462-9622 or support@tdt.com) before attempting to make any custom connections to pins 6, 18, or 19.

PZ3 Low Impedance Amplifier

PZ3 Overview

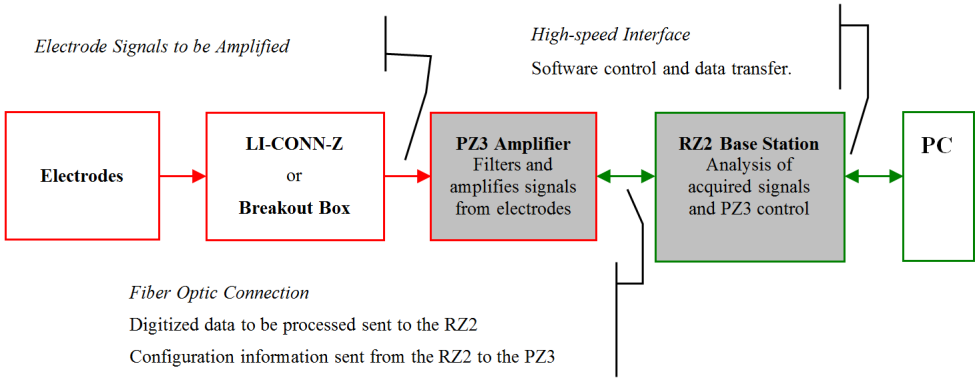
The PZ3 is a high channel count, low impedance amplifier well suited for ECOG, Evoked Potentials, EEGs, LFP's, EMGs, and other similar recording applications. Available in 32, 64, and 128 channel models, the PZ3 amplifier offers shared or true differential operation, low input referred noise, impedance checking, and an optional high input range mode.

System Hardware

A standard configuration for low sample rate, low impedance recordings includes 1.5 mm TouchProof connectors for electrodes, a PZ3 amplifier, and an RZ2 base station.

The battery powered PZ3 digitizes and amplifies signals recorded from each of the electrode channels. All digitized signals are sent via a single fiber optic connection to the RZ2 base station for further processing. The RZ2 also sends amplifier configuration information to the PZ3 across the fiber optics.

The diagram below illustrates this flow of data and control information through the system.

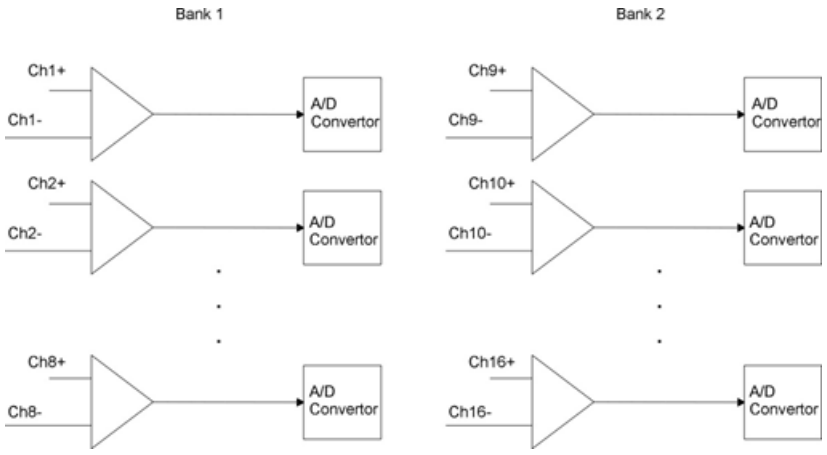


PZ3 Data and Control Flow Diagram

Recording Modes

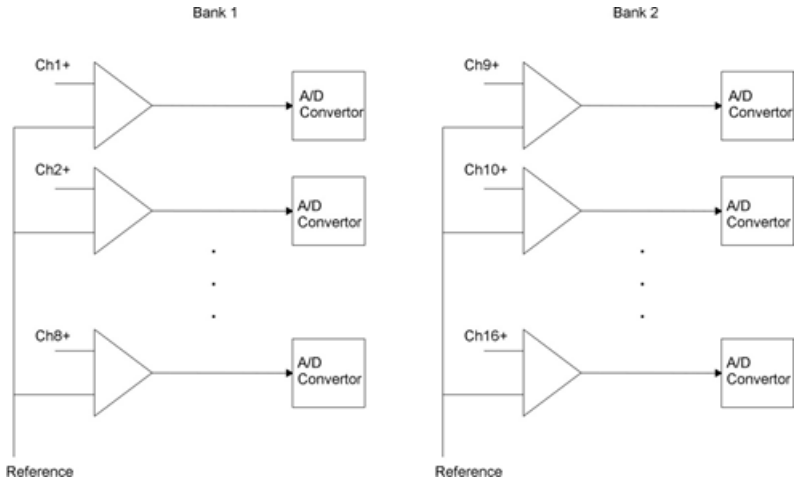
The PZ3 supports two recording modes: Individual Differential and Shared Differential.

For **Individual Differential** (true differential) operation, the amplifier inputs are grouped into banks of eight recording (+) channels, each with a paired alternate indifferent (-) channel (inverting channel).



Individual (True) Differential, Bank 1 and 2 Functional Diagram

For **Shared Differential** operation, each bank of channels uses a separate shared reference.



Shared Differential, Bank 1 and 2 Functional Diagram

The PZ3's impedance checking and a high voltage range features can be used in both true and shared differential modes.

It is also important to note that in the various modes of operation, the RZ2 processor may use the alternate channels to report information such as impedance values or RMS. This occurs at the software level on the RZ2. For example, in Shared Differential mode the RZ2 maps RMS levels for each channel to the alternate channels.

Electrode Connectors

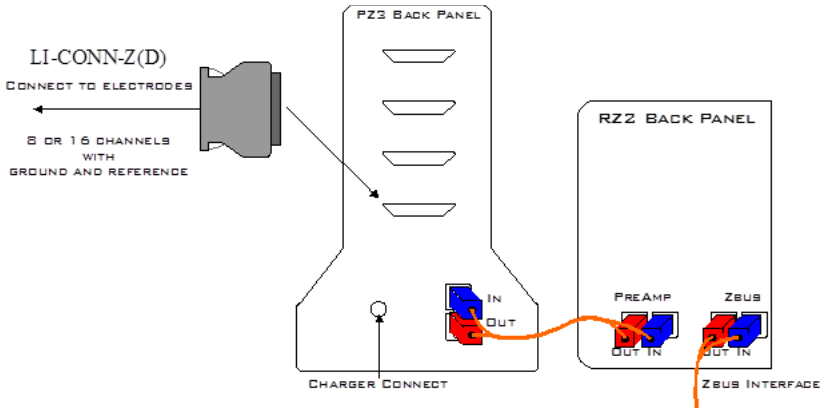
The PZ3 is designed to record from low impedance electrodes and electrode caps with input impedance less than 20 kOhm. Signals are input via multiple DB26

connectors on the PZ3 back panel. A break out box or connector(s) are required for electrode connection.

TDT provides a version of our LI-CONN connector for the PZ3: the LI-CONN-Z for Shared Differential mode. It features standard 1.5 mm safety connectors and provides easy connections between electrodes and the amplifier.

Hardware Set-up

The diagram below illustrates the connections necessary for PZ3 amplifier operation.



One or more male connectors (such as the LI-CONN-Z) can be connected to the input connectors on the PZ3 back panel. Alternately, custom connectors and a breakout box can be used. If using custom connectors, see “Input Connectors” on page 7-76 for pinout.

Note: In Shared Differential mode no connection should be made to the indifferent (-) channels.

A 5 meter paired fiber optic cable is included to connect the preamp to the base station. The connectors are color coded and keyed to ensure proper connections.

The PZ3 battery charger connects to the round female connector located on the back panel of the PZ3 amplifier.

Important! To avoid introducing EMF noise, DO NOT connect the charger to the PZ3 while collecting data.

PZ3 Software Control

The amplifier's mode of operation (shared or individual differential), other options, and channel mapping tasks are handled using PZ3 specific macros within the RPvdsEx control circuits running on the RZ2 Signal Processor.

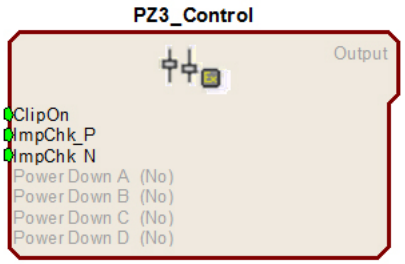
RPvdsEx includes two PZ3 specific macros:

PZ3_Control macro

PZ3_ChanMap macro

PZ3_Control Macro

The PZ3 Control macro should be added to your RPvdsEx circuit to configure all hardware features of the PZ3 amplifier.



Inputs are available on the macro for enabling/disabling the LED clip status lights, enabling Impedance mode for electrode (+) channels, enabling Impedance mode for alternate indifferent (-) channels, and dynamic power control for channel banks.

Macro Options

Double-clicking the macro in RPvdsEx, displays the macro properties dialog box and allows users to easily modify macro properties.

On the Options tab, in the properties dialog box:

Setting the **Clip LEDs On** to Yes or No enables or disables the LED clip warning indicators.

Differential Mode allows the user to select from Shared Differential) or Individual (True-Differential) modes.

Input Range may be set to either 3mV or 20mV input ranges.

The **Target Impedance** option allows the user to specify the impedance threshold for the status LEDs for each channel bank. Three inputs are available on the macro for enabling/disabling the LED clip status lights, enabling Impedance mode for electrode (+) channels, and enabling Impedance mode for indifferent (-) channels.

Under the **Power Contro**l tab are additional options that specify how the PZ3 channel banks are powered.

Powering Down the Channel Banks

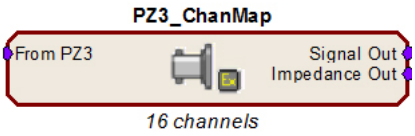
Channel banks may be powered down through the macro. As long as the *Power Control Mode* under the Power Control tab is set to *Static*, channel banks may only be powered up or down through the Power Control Mode options within the macro. Dynamic mode will allow channel banks to be powered on or off either through both the Power Control Mode options or by inputs on the macro through RPvdsEx components. Each of the letter indexed channel banks in the macro correspond to 32 channels of the PZ3. Selecting *No* will enable a bank of channels while selecting *Yes* will power down and disable that bank of channels.

For Example:

If you are using a PZ3 with 128 channels, powering down Bank A (Select **Yes**) would power down the first four blocks of 8 channels of the PZ3, disabling channels 1 – 32.

PZ3_ChanMap Macro

In the data stream on the RZ2, the odd numbered channels are the recording channels and the even numbered channels can report impedance measurements or RMS values. The PZ3_ChanMap should be added to your RPvdsEx circuit along with the RZ2_Input_MC macro to remap the data stream. The channel mapping macro selects the appropriate channels from the PZ3 input stream and builds two separate, sequential multichannel outputs containing either the amplified waveforms or alternate data (impedance or RMS values).



Macro Options

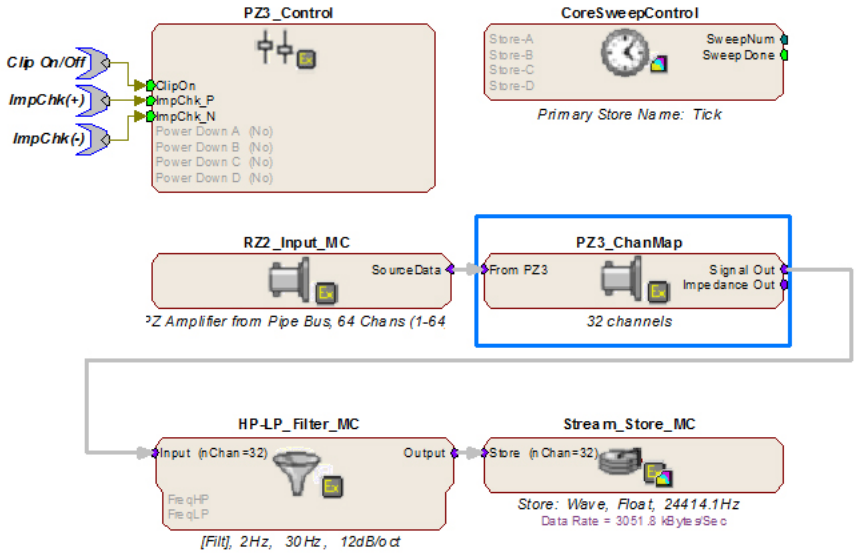
The user can set several different options under the Options tab.

The designated number of channels to map and output.

The ability to enable/disable the impedance measurement output.

PZ3 Circuit Example

The following illustration shows how macros can be used to create a simple OpenEx acquisition and control circuit for the PZ3.



The RZ2_Input_MC macro feeds the circuit with each digitally amplified signal acquired using the PZ3 amplifier. The data is fed first through the PZ3_ChanMap macro which separates the signals from their impedance (or RMS) values and builds the appropriate multi-channel data stream for further processing. In this case the signals are filtered and stored for post processing.

A CoreSweepControl macro is included to handle the required timing functions used by programs such as OpenEx and a PZ3_Control macro configures the operation mode of the PZ3 as well as any additional options that may be necessary. Three

parameter inputs allow toggling of clipping LEDs and toggling (+) or (-) channel impedance measurements.

PZ3 Operation

RCX control circuits running on the base station must include PZ3 specific macros to configure the amplifier's mode of operation; Shared Differential or Individual Differential and other configuration options such as input range and clip warning display. "PZ3 Software Control" on page 7-67, for more information. Impedance checking is also available from the front panel.

Powering ON

To turn the amplifier on, move the three position battery switch to either the Bat-A or Bat-B position.

Powering OFF

To turn the amplifier off, move the three position battery switch to the OFF position.

Operation Modes

Recorded signals are acquired in Shared or Individual differential mode.

Shared Differential

In shared differential mode a single shared reference and a ground are used for each bank of eight recording channels.

Note: In this mode no connection should be made to the alternate indifferent (-) channels. Use the LI-CONN-Z connector to ensure proper connections.

Enabling Shared Differential Operation

To enable shared differential mode, use the PZ3 control macro and under the Options tab set the value of Differential Mode to Shared.

Individual Differential

When the PZ3 is operating in individual differential mode, each of the 8 (+) channels of an individual bank has a paired (-) differential reference.

Note: While operating in this mode no connections should be made to the Shared Reference (pin 5.)

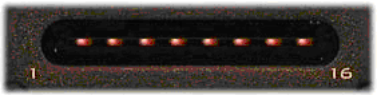
Enabling Individual Differential Mode

To enable individual differential mode, use the PZ3 control macro and under the Options tab set the value of Differential Mode to Individual.

Clip Warnings

Analog clipping occurs when the input signal is too large. If analog clipping occurs, TDT recommends switching the PZ3 into high input range mode. For more information see “Modifying the Input Voltage Range on the PZ3 ” on page 7-71.

While the amplifier is recording, the front panel LEDs can act as clip warning indicators (according to configuration settings set using the PZ3_Control macro). If an analog signal approaches the PZ3s clipping range, the PZ3 LEDs for the corresponding channel are lit red.



Note: The LED Indicators are also mirrored on the RZ2 LCD display.

When recording, the status LED located below the Display Mode button indicates the status of the Clip Indicators. Solid green indicates that clip warning is disabled and orange indicates the clip warning is enabled.

To enable clip warning, press the **Display Mode** button on the PZ3 front panel.

Alternatively the PZ3_Control macro can be used to enable or disable the clip warning indicators. For more information on the PZ3_Control macro see“PZ3 Software Control” on page 7-67.

External Ground

The external ground is optional and should only be used in cases where the subject must occasionally make contact with a metal surface that isn’t tied to the animal ground, such as a lever press. When contact is made, a ground loop is formed that temporarily adds extra noise to the system. Grounding this metal surface directly to the TDT hardware removes this ground loop at the cost of raising the overall noise floor a small amount.

A banana jack located on the back of the PZ3 (directly to the right of the charger input) provides connections to common ground for the first bank of channels (1-16). A cable kit is also provided to ensure cables used with the external ground are suitable for this use. Each kit includes: one male banana plug to male banana plug pass through and one male banana plug to alligator clip pass through. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

Modifying the Input Voltage Range on the PZ3

In the default mode, the PZ3 has an effective differential input range of +/- 3mV, which TDT recommends for EEG, LFP, and ECOG. If recordings demand a higher input range such as EMGs, the alternate High Input Range mode allows the input range to increase to +/- 20 mV.

Important! The PZ3 automatically detects the gain setting and voltage range and scales the signal output accordingly.

Note: The signal to noise performance is better while operating in the +/- 3mV input range.

Enabling the High Input Range Mode

The high input range mode can be enabled through the PZ3_Control macro.

To enable the high range input mode, select **20 mV** from the **Input Range** option on the **Options** tab.

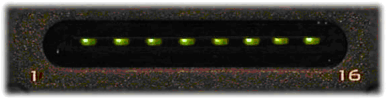
Testing your Electrode Impedance

Impedance measurement may be enabled programmatically or using the *Display Mode* button.

Enabling Impedance Mode

To enable impedance mode manually, push and hold down the Display Mode button on the PZ3 front panel.

During impedance checking all channels are tested in parallel using a ~375 Hz test signal and the impedance is measured relative to a target impedance (1kW – 15kW) specified by the user (set using the PZ3_Control macro). The LEDs on the PZ3 (and in the PZ3 display on the RZ2 LCD) will light green when the electrode impedance is less than or equal to the target impedance or red when electrode impedance is greater than the target impedance value.



Green: Less than or equal target impedance

Red: Greater than target impedance

Impedance Checking For True Differential Mode

Impedance values of either recording (+) or alternate indifferent (-) channels can be tested.

To toggle between (+) and (-) channel impedance measurements, press the **Display Mode** button on the PZ3 front panel.

The status LED located below the *Display* button of the PZ3 will flash green while electrode (+) channel impedance is being tested or red while alternate indifferent (-) channel impedance are being tested.

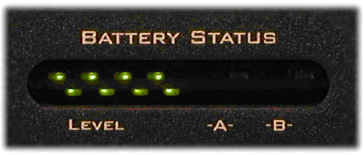
Returning to Signal Acquisition Modes

To leave Impedance mode, simply hold down the **Display Mode** button on the PZ3 front panel after enabling impedance mode.

Battery Overview

The PZ3 amplifier features two Lithium ion batteries to allow for longer record times. A three-position switch selects the active battery between Bank-A, Bank-B, or both banks off.

Battery Status LEDs



Battery Level: Eight LEDs indicate the voltage level of the selected battery bank. These LEDs can be found on the front of the PZ3 amplifier by the heading Level. When the battery is fully charged, all eight LEDs will be lit. When the battery voltage is low, only one green LED will be lit. If the voltage is allowed to drop further, the last LED will flash red. TDT recommends charging the battery before this flashing low-voltage indicator comes on. While charging, the Level LEDs will flash green.

Status	Description
8 Green	Fully Charged
1 Green, 7 Unlit	Low Voltage
1 Flashing Red	Low Voltage - Charge Immediately!
8 Green Flashing	Charging in Progress

Charging the Batteries

Operate the amplifier with the charging cable disconnected. Connecting the PZ3 charger will simultaneously charge both batteries. Ensure that the three-position switch is in the OFF (middle) position while charging the PZ3.

Charging Indicators

LEDs are also used for each bank to indicate which bank, if any, is charging. These LEDs are found next to the Level LEDs by the headings -A- and -B-. A green indicator denotes the battery bank is fully charged while a red indicator designates the bank is currently charging. When the device is in operation (charger is not connected) the A and B LEDs are not lit.

Status	Description
Red	Charging
Green	Fully Charged
Unlit	Operation Mode (charger not connected)

An external battery pack is also available to provide longer battery life for extended recording sessions. See "PZ-BAT External Battery Pack for the PZ Amplifiers" on page 7-109.

PZ3-RZ2 Channel Data Charts

The following charts show what data the user can expect to be available on the RZ2 for each channel depending on whether the amplifier is in a recording mode or in

impedance checking mode. Please note that this does not necessarily reflect how the hardware channels are used on the PZ3. The RZ2 interprets input from the PZ3 then makes the data available as described below. To further simplify circuit design, the PZ3_ChanMap macro can be used to build separate multichannel data streams for waveform data and impedance values.

Unmapped Channel Index	Recording Mode	
	Shared Differential	Individual Differential (True Differential)
Channel 1	Analog Input Channel 1	Analog Input Channel 1(+)
Channel 2	RMS of Channel 1	Reference Channel 1(-)
. .	. .	. .
Channel 15	Analog Input Channel 8	Analog Input Channel 8(+)
Channel 16	RMS of Channel 8	Reference Channel 8(-)

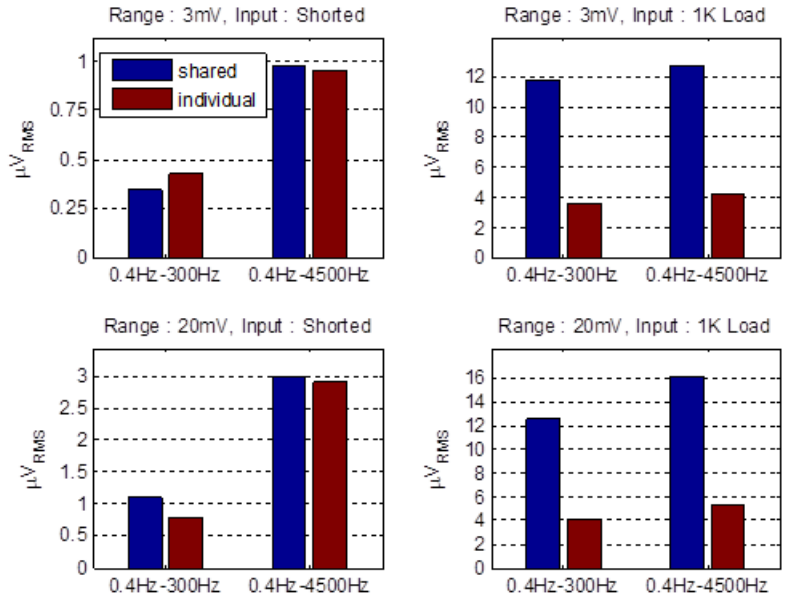
Unmapped Channel Index	Impedance Checking	
	Shared Differential	Individual Differential (True Differential)
Channel 1	NA	NA
Channel 2	Impedance of Channel 1	Impedance of Channel 1 (+) or (-)
. .	. .	. .
Channel 15	NA	NA
Channel 16	Impedance of Channel 8	Impedance of Channel 8 (+) or (-)

PZ3 Technical Specifications

A/D	Up to 128 channels 18-bit hybrid
Maximum Voltage In	+/- 3 mV - Default input range mode +/- 20 mV - High input range mode
Frequency Response	3 dB: 0.1 Hz – 5 kHz
S/N (typical)	72 dB – 3mV input range 79 dB – 20mV input range
Distortion (typical)	< 1%
A/D Sample Rate	Up to 48828.125 Hz
Input Impedance	10^6 Ohms

Power Requirements	2 Lithium Ion cells at 10 AmpHours each
Battery	Eight hours to charge both cells Battery life between charges, per cell: 32 ch ~ 11 hrs 64 ch ~ 8 hrs 128 ch ~ 5 hrs
Charger	External 6 V, 3 A power supply
Indicator LEDs	Up to 128 status or clip warning, battery life, active battery bank
Input referred noise	See figures below
Fiber Optic Cable	5 meters standard, cable lengths up to 20 meters*

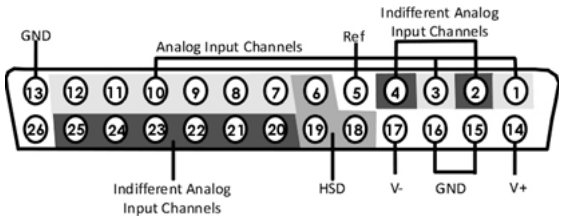
*Note: If longer cable lengths are required, contact TDT.



Input Connectors

PZ3 amplifiers have up to 16 26-pin headstage connectors on the back of the unit. The PZ3 channels are marked next to the respective connector on the amplifier.

Pinout Diagram



Note: There are 8 (+) channels and 8 (-) channels per DB26 connector. Subsequent banks are indexed by an additional 8 channels.

Pin	Name	Description		Pin	Name	Description
1	A1(+)	Analog Input Channel		14	V+	Positive Voltage (+1.5V)
2	A1(-)	Indifferent Analog Input Channel		15	GND	Ground
3	A2(+)	Analog Input Channel		16	GND	
4	A2(-)	Indifferent Analog Input Channel		17	V-	Negative Voltage (-1.5V)
5*	Ref*	Shared Reference*		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A3(+)	Analog Input Channels		20	A3(-)	Indifferent Analog Input Channels
8	A4(+)			21	A4(-)	
9	A5(+)			22	A5(-)	
10	A6(+)			23	A6(-)	
11	A7(+)			24	A7(-)	
12	A8(+)			25	A8(-)	
13	GND	Ground		26	NA	Not Used

***Note:** No connections should be made to pin 5 while operating in True Differential mode.

PZ4 Digital Headstage Manifold

PZ4 Overview

The PZ4 is a high channel count manifold for transmitting extracellular recordings acquired with TDT's ZCD digital headstages to an RZ base station for processing.

This device supports sampling rates up to ~25 kHz. The PZ4 manifold is available with 1, 2 or 4 digital headstage connections for a variety of channel counts.

The PZ4-4 has four DB26 connections and can support up to 256 channels. The PZ4-2 has two DB26 connections and can support up to 128 channels. The PZ4-1 has a single DB26 connection and can support up to 32 channels.

PZ4 System Hardware

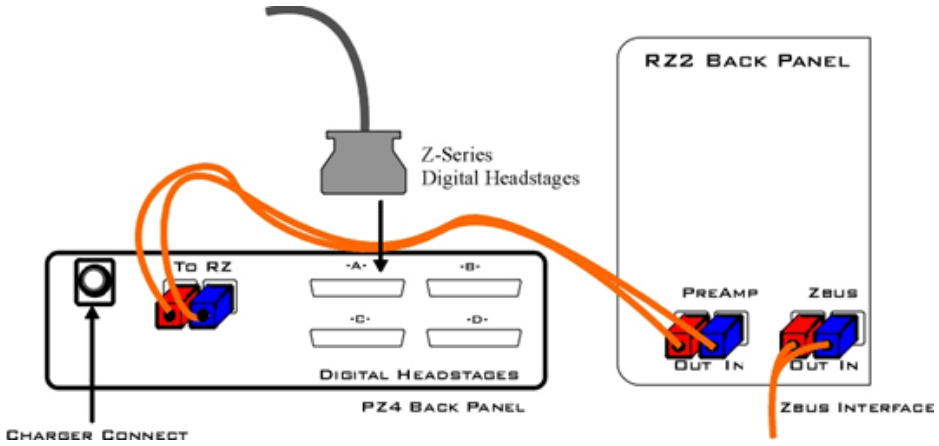
Analog signals from the electrodes are digitized on the ZCD headstage and transmitted to the PZ4. They are then organized and streamed to the RZ base station over a fiber optic connection for further processing and data storage.

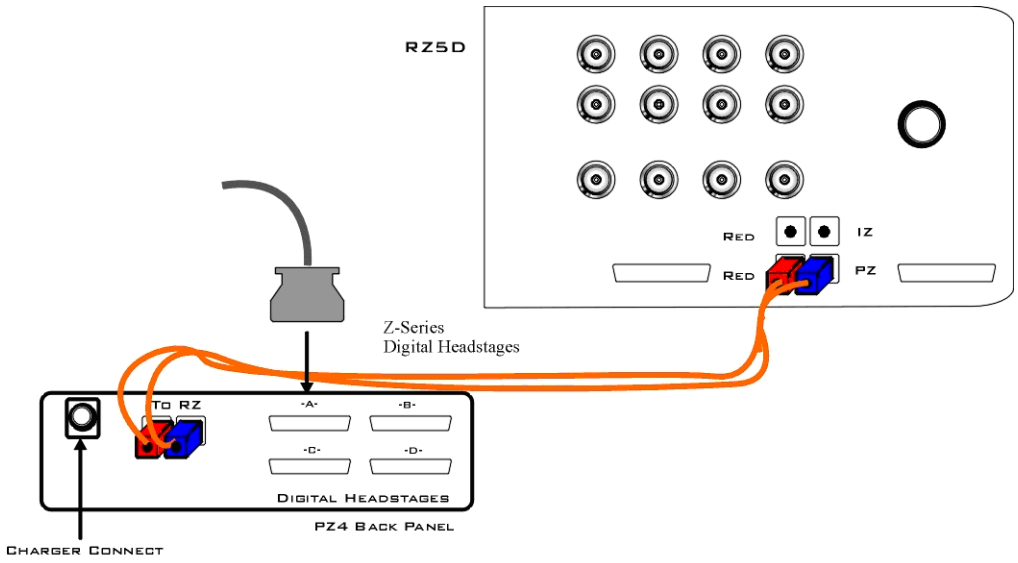
The PZ4 Manifold has up to four 26-pin headstage connectors (DB26) on the back of the unit. Because the PZ4 accepts digital inputs, the channel count for each DB26 connection is not fixed. Each DB26 connection can support any headstage channel count up to the limit for the entire PZ4 device. For example, the DB26 port on a PZ4-1 can accept either a 16 channel (ZCD-16) or 32 channel headstage (ZCD-32). A PZ4-2 might have a 32ch headstage (ZCD-32) connected to Bank A and a 96 channel headstage (ZCD-96) connected to Bank B for a total of 128 channels.

The PZ4 will automatically detect the number of channels in the headstage on each DB26. All channels will be concatenated together, starting with connector "-A-", to create the output signal to the RZ base station.

Hardware Set-up

The PZ4 can connect to any RZ with a PZ port. This includes an RZ2, any RZ with an RZDSP-P card or any RZ5D. The diagram below illustrates the connections necessary for PZ4 manifold operation for an RZ2 and an RZ5D.





One or more ZCD headstage can be connected to the input connectors on the PZ4 back panel.

Only TDT digital headstages can be connected to the PZ4. No other connections should be attempted.

A 5-meter paired fiber optic cable is included to connect the preamplifier to the base station. The connectors are color coded and keyed to ensure proper connections.

The PZ4 battery charger connects to the round female connector located on the back panel of the PZ4 preamplifier. The battery will only charge when the power switch is in the CHG position.

Power Switch

To turn the PZ4 on, move the two-position battery switch located on the front panel to the ON position. To turn the PZ4 manifold off, or to charge the battery, move the two-position battery switch to the CHG position.

PZ4 Features

Headstage LEDs

An LED for each headstage (labeled -A-, -B-, -C-, -D-) indicates whether or not a digital headstage is detected. Each LED turns green when a headstage is detected on the corresponding port. If the headstage configuration changes while the PZ4 is under power, all headstage LEDs affected by the change will turn red. For example, if a headstage connected to bank A is swapped with a headstage connected to bank B, the -A- and -B- LEDs that were previously green will turn red. This is an alert to the user that the PZ4 has reconfigured the channels. The red LEDs can be cleared by cycling the power on the PZ4.

Status LED

The Status LED indicates if the PZ4 is synchronized to the RZ base station. It will turn green when synchronized and red otherwise.

External Ground

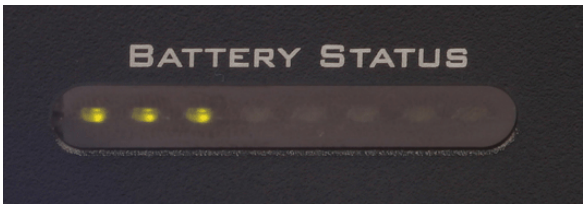
The external ground is optional and should only be used in cases where the subject must occasionally make contact with a metal surface that isn't tied to the animal ground, such as a lever press. When contact is made, a ground loop is formed that temporarily adds extra noise to the system. Grounding this metal surface directly to the TDT hardware removes this ground loop at the cost of raising the overall noise floor a small amount.

A banana jack located on the back of the PZ4 (directly below the fiber optic port) provides connections to common ground for all channels. A cable kit is also provided to ensure cables used with the external ground are suitable for this use. Each kit includes: one male banana plug to male banana plug pass through and one male banana plug to alligator clip pass through. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

Battery Overview

The PZ4 manifold contains a Lithium ion battery pack.

Battery Status LEDs



Eight LEDs on the front panel indicate the voltage level of the PZ4 battery. When the battery is fully charged, all eight LEDs will light green. When the battery voltage is low, only one green LED will be lit. If the voltage is allowed to drop further, the last LED will flash red. TDT recommends charging the battery before this flashing low-voltage indicator comes on. While charging, the Battery Status LEDs will flash red and green.

Status	Description
8 Green	Fully Charged
1 Green, 7 Unlit	Low Voltage
1 Flashing Red	Low Voltage - Charge Immediately!
Green/Red Flashing	Charging in Progress

Charging the Batteries

The PZ4 power switch should be in the CHG position while charging, otherwise 50/60Hz noise will bleed into the recordings.

An external battery pack (PZ-BAT) is also available to provide longer battery life for extended recording sessions. See "PZ-BAT External Battery Pack for the PZ Amplifiers" on page 7-109.

PZ4 Technical Specifications

Sample Rate	Up to 24414.0625 Hz
Power Requirements	One Lithium Ion cell at 12.75 AmpHours
Battery	5 hours to charge the battery 8-10 hrs battery life between charges
Charger	External 6 V, 3 A power supply
Indicator LEDs	Headstage status, battery life, sync status
Fiber Optic Cable	5 meters standard, cable lengths up to 20 meters*

***Note:** If longer cable lengths are required, contact TDT.

Medusa4Z BioAmp

Medusa4Z Overview

The Medusa4Z is a four-channel, referential, low-noise digital bioamp targeted for use in low-channel-count, low-impedance neurophysiology recordings, such as ABR, EEG, EMG, or EKG signals. The bioamp digitizes one or four channels at acquisition rates of approximately 3kHz, 6kHz, 12kHz, or 25kHz, and the amplified digital signal is sent to the base station via a noiseless fiber optic connector.

Connections to the subject (four channels, reference, and ground) are made with six standard 1.5 mm touchproof safety connectors.

- It is powered by a 5 AmpHr Li-Poly battery that provides up to 30 hours of continuous data acquisition in single-channel mode and up to 24 hours in four-channel mode.
- It includes impedance testing functionality for each of the four recording channels as well as the reference electrode.
- The user interface has 8 buttons and a 16 x 2 character LCD display screen. It lets you select performance characteristics of the preamplifier and shows battery and signal level.
- A complete charge from a dead battery can be achieved in under 8 hours with the included charger.

Medusa4Z Features

The Medusa4Z has the option to be run in single-channel mode or four-channel mode. When in single channel mode, channels 2-4 are powered down and isolated from the reference line. Running in single-channel mode will provide slightly better performance and longer battery life.

There are selectable Sampling Frequency options of approximately 3 kHz, 6 kHz, 12 kHz, or system rate (maximum 25 kHz). Users will find that using the lowest practical rate improves noise performance.

When testing the impedance of the probes, users can select frequencies of 100 Hz, 300 Hz, 500 Hz, or 1 kHz.

A user-selectable digital highpass filter has adjustable options that are: Off, 1 Hz, and 3 Hz. The hardware has a fixed analog highpass at 0.3Hz.

An Auto Shutdown feature has three modes: Never, 1 hour, 3 hours, or 5 hours. If no buttons are pressed after this interval, then the device will automatically power down. If no optics are detected, the Medusa4Z will also shutdown. Before shutting down, the blue POWER LED will blink fast to indicate that time has expired. Pressing any key will reset the counter.

Analog Input Channels

The Medusa4Z Preamplifier acquires signals with 16-bit PCM ADCs. The signals are oversampled before conversion to remove aliasing of high frequency RF signals. This allows users to acquire at lower sampling rates (down to 3 kHz) with improved signal-to-noise quality in that range and no aliasing. The Medusa4Z can also acquire data in High-Resolution mode which uses 24-bit PCM ADCs. This is controlled by the base station (RZ, RX) to which the Medusa4Z is connected. The change occurs by modifying the underlying circuit running on the base station in Synapse or BioSigRZ. This is the handled by default in BioSigRZ v5.7.5 and above, and in TDT Drivers v92 and above there is a RPvdsEx circuit macro available in: C:\TDT\RPvdsEx\Macros\Device\Medusa4Z_Bioamp.

Electrode Connectors

Plug the electrodes directly into the standard 1.5mm touchproof connectors on the side of the Medusa4Z.

Impedance Checking

The Impedance checker on the Medusa4Z provides a simple check of the channel impedance relative to ground. To check the impedance level, press the button next to the channel indicator (e.g. CHAN-1). The impedance between channel and ground will be shown on the screen. The REF impedance button checks the impedance between the reference and the ground. Impedance checking frequency options are 100 Hz, 300 Hz, 500 Hz, and 1kHz. These are settable on the user interface.

LCD Screen

The LCD screen shows the current sampling rate, battery level, and signal level indication on the active channels.

Use the SETUP button to cycle through available settings and use the OPTION button to change the currently selected setting. Settings include:

Active Channels: Single or Four Channel

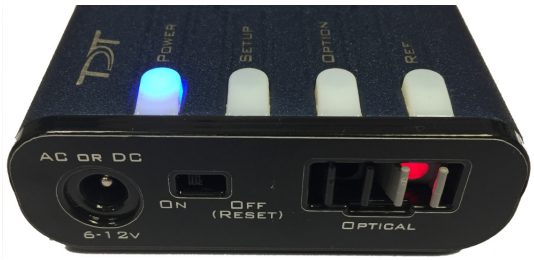
Sample Frequency: ~3kHz, ~6kHz, ~12kHz, System Rate (up to ~25kHz). Match this to the desired frequency range of your acquired signal (maximum frequency captured will be ~45% of selected sample frequency). Note that lower sampling rates will have improved signal-to-noise, but they will also have longer sample delays. Please refer to the "Medusa4Z PreAmp Technical Specifications" on page 7-85 for more information.

Probe Frequency: 100 Hz, 300 Hz, 500 Hz, 1 kHz. Choose the default frequency used for the impedance checker.

Highpass Filt: Off, 1 Hz, 3 Hz. Set the highpass filter cutoff frequency on the input signals. 'Off' is a 0.1 Hz filter. Note that there is a fixed 0.3 Hz highpass analog filter on the inputs.

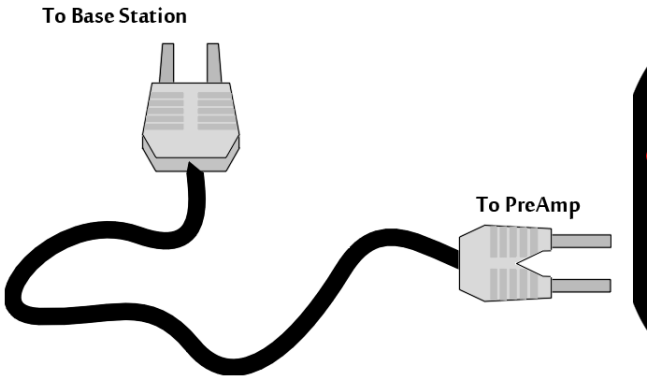
Auto Shutdown: Never, 1 hr, 3 hr, 5 hr. After a period of inactivity the Medusa4Z will shut itself down to preserve power. This prevents dead batteries from accidentally leaving the unit on overnight.

Base Station Connector - Optical



Use the provided fiber optic pair (black cable, white connectors) to connect the OPTICAL port on the preamplifier to the optical input port on the base station.

The duplex fiber optic cable has identical one-piece connectors at each end. There is a V-shaped groove on one side of the connector and a raised rectangle on the other. As shown in the image below, plug the connector into the RZ6 port with the raised rectangle side up. Plug the connector into the preamplifier with the V-shaped groove up.



Medusa4Z Connection Diagram

Power

The POWER button on the face of the Medusa4Z powers it on. Press and hold the button to power it off. Press the power button momentarily to go to the home screen from anywhere or to reset the power down timer.

Do not use the recessed slide power switch (ON OFF (RESET)) on the side of the device unless you need to reset all settings to factory default, or if you are storing the Medusa4Z for an extended period of time and want to completely disconnect the battery. The OPTICAL fiber connector at the right will be illuminated when the amplifier is on.

Power Requirements

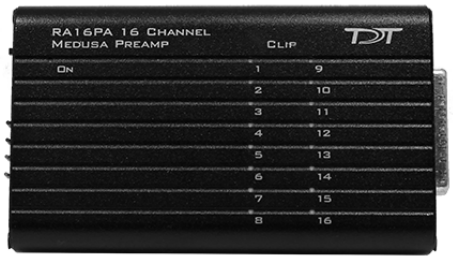
The lithium battery charges in four hours. Keeping the battery charger connected to the amplifier does not affect the battery life. However, the charger will significantly increase the noise of the system if it is plugged in while an experiment is running. A 12 Volt battery charger is included with the amplifier. The supplied charger tip is center negative. However, tip polarity can be positive or negative if the charger needs to be replaced.

The lithium battery supplied with the system cannot be removed. If battery life longer than 30 hours is required, an external battery pack can be connected to the voltage inputs of the charger. TDT recommends a 6 (minimum) to 16 Volt (maximum) battery, such as lead acid batteries used for motorized wheel chairs. Contact TDT for more information.

Medusa4Z PreAmp Technical Specifications

A/D	Up to 4 channels Standard Mode: 16-bit PCM High-Resolution Mode: 24-bit PCM
Sample Rate	~3 kHz, ~6 kHz, ~12 kHz, or ~25 kHz
Maximum Voltage In	+/- 10 mV
Gain	100x
Frequency Response	3 dB 0.3 Hz - 0.45*Fs (with no additional high-pass filter selected)
Highpass Filter	0.3 Hz, 1 Hz, or 3 Hz
Anti-Aliasing Filtering	45% sampling rate
S/N (typical)	80 dB
Input Referred Noise (µVrms)	Depends on Med4Z sample rate and electrode impedance Medusa4Z rate shorted 3kOhm 10kOhm 3 kHz 0.15 0.3 0.5 6 kHz 0.25 0.4 0.7 12 kHz 0.3 0.6 1.0 25 kHz 0.4 0.9 1.4
Sample Delay	Dependent on Medusa4Z and RZ processor sample rates (RZ at 25 kHz)(RZ at 12 kHz)(RZ at 6kHz) Medusa4Z rate samples samples samples 25 kHz 24 N/A N/A 12 kHz 42 24 N/A 6 kHz 76 42 24 3 kHz 146 76 42
Input Impedance	100 kOhm
Battery	Li-Poly Battery 5000 mAh single-channel mode: 30 hours between charges four-channel mode: 24 hours between charges. 1000 cycles of charging, not removable by user
Charger	6-16 V DC, > 1 A, center-positive or center-negative.
Fiber Optic Cable	5 meters standard, maximum cable length 12 meters

RA16PA/RA4PA Medusa PreAmps



Medusa Overview

The Medusa Preamplifiers are low noise digital bioamplifiers and are available with either PCM or Sigma-Delta ADCs. The system amplifies and digitizes up to 16-channels of analog signal at a 24.414 kHz sampling rate. The amplified digital signal is sent to the base station via a noiseless fiber optic connector.

- Digitizes either four or 16 channels at acquisition rates of approximately 6, 12, or 25 kHz.
- Connects to the headstage via a DB25 connector.
- Powered by a Lithium-ion battery that provides 20 hours of continuous data acquisition in 16-channel mode and 30 hours of operation in 4-channel mode.
- Clip warning lights indicate when any signal is -3db from the preamplifier's maximum voltage input.

Medusa Features

Analog Acquisition Channels

The RA16PA and RA4PA standard Medusa Preamplifiers acquire signals using 16-bit PCM ADCs, which provide quality acquisition with minimal delay. The RA16SD and RA4SD use Sigma-Delta ADCs, which have several characteristics that improve signal quality. Oversampling of the signal before conversion removes aliasing of high frequency RF signals.

RA16SD testing indicates that signals greater than 150% of the Nyquist frequency are removed from the signal. This allows users to acquire at lower sampling rates (6 kHz) without worry of significant aliasing. In addition, each converter also has a two pole anti-aliasing filter (12 dB per Octave) at 7.5 kHz. However, the sigma-delta ADC's have a fixed group delay of 20 samples (compared to four samples for the RA16PA). When using the RA16SD this group delay must be taken into account

when the data is displayed or acquired (for example, adding a SampDelay to the RPvdsEx circuit).

Clip Warning Lights

When the input to a channel is greater than -3db from the preamplifier's maximum voltage input, a light on the top of the amplifier is illuminated. The first column of lights corresponds to channels 1-8 and the second column corresponds to channels 9-16. The clip warning light indicator can be turned off by flipping a switch on the end of the amplifier.

Power Light

The power light is in the top corner of the amplifier. It is illuminated when the device is on. It flashes quickly if the battery is low. It flashes slowly while the battery is charging. Note: The flashing LED indicator is only available when the amplifier is powered on and connected to a powered base station.

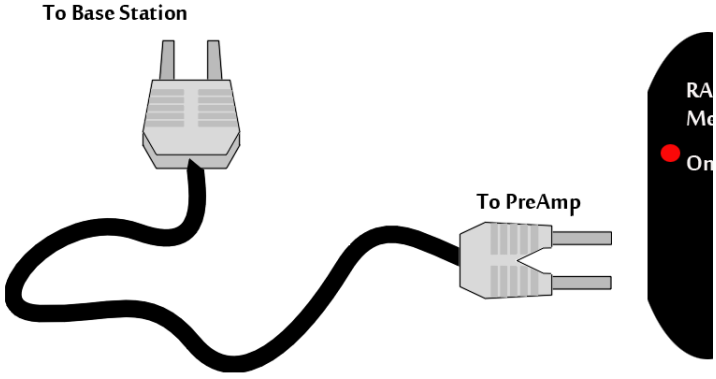
Headstage Connector

The headstage connector is a 25-pin (16-channel) connector. Information on the pin inputs is provided with the technical specifications.

Base Station Connector - To Base

Use the provided fiber optic pair (white connectors) to connect the To Base port on the preamplifier to the optical input port on the base station.

The duplex fiber optic cable has identical one-piece connectors at each end. There is a V-shaped groove on one side of the connector and a raised rectangle on the other. As shown in the image above, plug the connector into the RZ6 port with the raised rectangle side up. Plug the connector into the preamplifier with the V-shaped groove up.



Medusa PreAmp Connection Diagram

Power

A switch on the back powers up the amplifier. The fiber connector at the right will be illuminated when the amplifier is on.

LEDs

This switch turns the clip warning lights on top of the amplifier on or off.

Power Requirements

The Lithium-ion batteries charge in four hours. Keeping the battery charger connected to the amplifier does not affect the battery life. However, the charger will significantly increase the noise of the system if it is plugged in while an experiment is running. A 6 volt battery charger is included with the amplifier. The charger tip is center negative. If it is necessary to replace the charger make sure that the power supply has the correct polarity.

The Li-ion battery supplied with the system cannot be removed. If battery life longer than 30 hours is required, an external battery pack can be connected to the voltage inputs of the charger. TDT recommends a 6 (minimum) to 9 Volt (maximum) battery, such as lead acid batteries used for motorized wheel chairs. Contact TDT for more information.

RA16PA Medusa PreAmp Technical Specifications

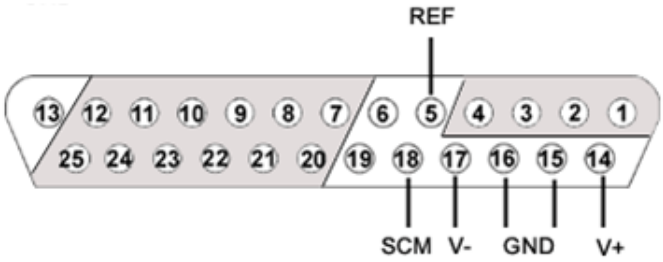
Includes specifications for the RA4PA, RA16PA, and RA16SD Medusa Preamplifiers.

A/D	RA4PA: 4-channels 16-bit PCM RA16PA: 16-channels 16-bit PCM RA16SD: 16-channels 16-bit sigma-delta
Sample Rate	6, 12, or 25 kHz
Maximum Voltage In	RA4PA and RA16PA: +/- 4 millivolts RA16SD: +/- 5 millivolts
Frequency Response	3 dB 2.2 Hz - 7.5 kHz
Highpass Filter	2.2 Hz
Anti-Aliasing Filtering	RA4PA and RA16PA: 7.5 kHz (3 dB corner, 1st order, 6 dB per octave) RA16SD: 7.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
S/N (typical)	RA4PA and RA16PA: 60dB
Input Referred Noise	rms 3 microvolts bandwidth 300 - 3000 Hz 6 microvolts bandwidth 30 - 5000 Hz
Group Sample Delay	RA4PA and RA16PA: NA RA16SD: 20 Samples
Input Impedance	10^5 Ohms

Power Requirements	500 mAmps while charging, 60 mAmps once charged
Battery	Li-ion Battery 1950 mAh, 20-25 hours between charges. 1000 cycles of charging, not removable by user
Charger	6-9 Volts DC, greater than 500 mAmps, center negative
Fiber Optic Cable	5 meters standard, maximum cable length 12 meters

Pinout Diagrams

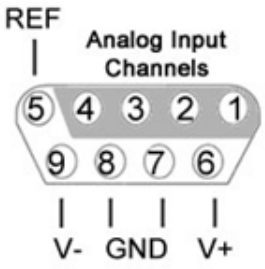
16/4-channel pinouts (all 16 and 4 channel models built after 2002):



Pin	Name	Description	Pin	Name	Description
1	A1	Analog Input Channel Number	14	V+	Positive Voltage Headstage Power Source (1.4 V as measured in reference to ground)
2	A2		15	GND	Ground
3	A3		16	GND	Ground
4	A4		17	V-	Negative Voltage Headstage Power Source (1.4 V as measured in reference to ground)
5	REF	Reference Pin	18	SCM	Sixteen Channel Mode Indicator Pin The status of pin 18 determines whether the preamplifier is in four or 16-channel mode. To use the preamplifier in 16-channel mode with a custom headstage, connect pin 18 to pin 17.
6	NA	TDT Use Only Pins 6, and 19 are for TDT use only and should not be used.	19	NA	TDT Use Only Pins 6, and 19 are for TDT use only and should not be used.
7	A5	Analog Input Channel Number	20	A6	Analog Input Channel Number
8	A7		21	A8	
9	A9		22	A10	
10	A11		23	A12	
11	A13		24	A14	
12	A15		25	A16	
13	GND	Ground			

Note: Grounds (pins 13, 15, 16) are tied together.

4-Channel Pinout



A 4-Channel connector is found only on models shipped before January 2002. **Note:** Pins 7 & 8, tied together.

Pin	Name	Description
1	A1	Analog Input Channel Number
2	A2	
3	A3	
4	A4	
5	REF	Reference Pin
6	V+	Positive Voltage Headstage Power Source
7	GND	Ground
8	GND	Ground
9	V-	Negative Voltage Headstage Power Source

RA8GA Adjustable Gain PreAmp

RA8GA Overview

The RA8GA was designed to acquire and digitize multi-channel data from a variety of analog voltage sources such as eye-trackers, amplifiers (including grass, axon, and WPI amplifiers), PH meters, and temperature sensors. The RA8GA digitizes up to eight channels at acquisition rates of 6, 12, or 25 kHz. All channels have a variable group gain setting of 10 Volts, 1 Volt, or 100 millivolts. The system has a bandwidth to DC, which allows users to acquire low frequency DC signals. In addition a two-pole low pass filter (12 dB per Octave) is set at 7.5 kHz.

Power and Interface

The device is powered via the System 3 zBus (ZB1PS) and requires an interface to the PC. If the RA8GA is housed in one of several ZB1PS chassis in your system, ensure that it is connected in the interface loop according to the installation instructions: Gigabit, Optibit, or USB Interface.

RA8GA Features

Max Input Lights

The Active light flashes once a second when the preamplifier is not connected to a base station. It glows steady when it is properly connected.

The 10 V, 1 V, and 0.1 V lights indicate the current acceptable voltage range. If the signal input reaches -6 dB from the maximum input for the selected range, a clip warning light on the base station will be lit. On RX5 or RX7 processors the LED located next to the fiber optic input port serves as the clip warning light.

Range Select Button

All channels use a group adjustable gain control i.e. all channels are either +/- 1 Volt, 10 Volts, or 0.1 Volt. A Range Selection button adjusts the gain setting among the following voltages: 0.1X gain = +/-10 Volts, 10X gain = +/- 100 milliVolts, 1.0 X gain = +/-1 volt. Press the button to scroll through the available

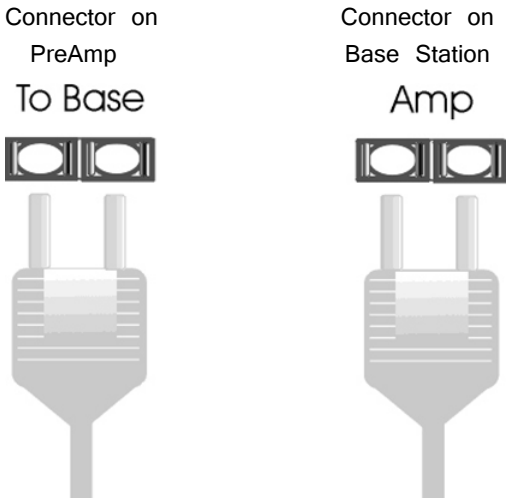
voltage ranges. Max input lights located to the left of the button, indicate the current selection.

To Base

The To Base connector is used to connect the device to the base station (such as RA16BA, RX5, or RX7) using a fiber optic cable pair. One end of the fiber optic cable connects to the device using this connection pair and the other end connects to the input on the base station.

Connecting the Base Station to the Preamplifiers

To make the connection, plug one end of the cable into one of the fiber optic connectors as shown below and connect the other end of the cable to the fiber optic port on the base station. Both ends of the cable are the same but the two sides of the connector are different. See the diagram below to determine the correct way to make the connection for each device.



Analog Input

Each Preamp comes with eight channels of analog input. Each analog input uses 16-bit PCM parts for high quality signal conversion. See the technical specifications for a Pinout Diagram for the 25-pin Analog Input connector.

A PP16 patch panel can be used to simplify connection to the preamplifier's analog inputs. A ribbon cable can be connected from the RA8GA Analog I/O connector to the RA16 connector on the back of the PP16 allowing acquisition of signals via the first eight BNC connectors on the front of the PP16.

RA8GA Gain Settings

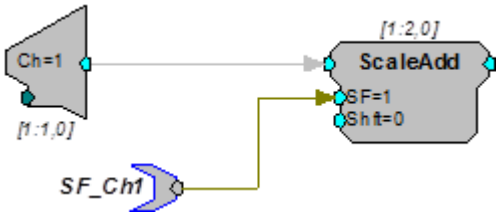
Gain	Voltage	RPvdsEx Scale Factor
0.1	+/-10 V	1700
1.0	+/- 1 V	170
10.0	+/- 0.1 V	17

Accounting for Gain Settings in RPvdsEx

The output from a RA8GA generates a floating-point value of between +/- 6 mVolts (i.e. the voltage value of the RA16PA). A scale factor must be used in order for the acquired signal to display the correct voltage. The scale factor for each gain setting is listed in the table above. The scale factor should be added after the channel input (ADCIn).

The following example shows a circuit segment that could be used to add the scale factor for a +/- 1 Volt range:

A parameter tag may be used to allow the scale factor of the channel input to be modified at run-time.

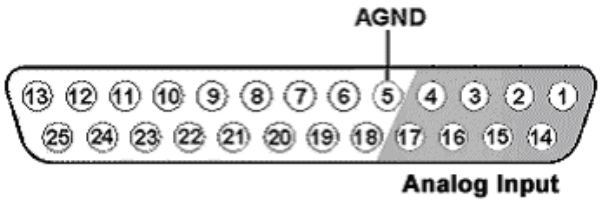


RA8GA Technical Specifications

A/D	8-channels 16-bit PCM
Maximum Voltage In	Variable gain settings allow +/-10V, +/-1 V or +/- 100 mV
Frequency Response	DC - 7.5 kHz (2nd order 12 dB per octave)
S/N (typical)	70 dB (+/- 1 V 1000 kHz) at 1 V Gain Setting
THD (typical)	0.01%

A/D Sample Rate	6, 12, or 25 kHz
Cross Talk	< -70 dB (DC - Nyquist)
Input Impedance	10 kOhm
Offset	< 5 mV at +/- 10 V < 3 mV at +/- 1 V and +/- 100 mV

Analog Input Pinout Diagram



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		14	A2	Analog Input Channels
2	A3			15	A4	
3	A5			16	A6	
4	A7			17	A8	
5	AGND	Ground		18	NA	Not Used
6	NA	Not Used		19		
7				20		
8				21		
9				22		
10				23		
11				24		
12				25		
13						

Headstage Connection Guide

Overview

Ground and Reference placement is important in all headstage configurations. They determine the operation of the headstage and can, if incorrectly wired, produce undesired results.

Important! High channel count recordings (implemented either with PZ or multiple Medusa preamplifiers) may be implemented using multiple headstages. **When using multiple headstages, ground pins on all headstages should be connected together to form a single common ground.** This ensures that all headstage ground pins are at the same potential and eliminates additive noise from varying potentials across the subject's brain.

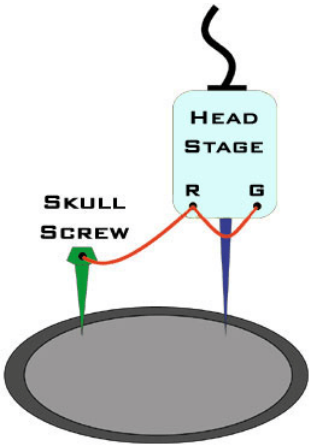
This section serves as a guide to headstage connection and will illustrate single and multiple headstage configurations. A common error example is provided for the final illustration.

Headstage Operation

Headstage operations can be categorized into three forms listed below. It is important that multiple headstage configurations use a common node for all grounds regardless of the operation of the headstage.

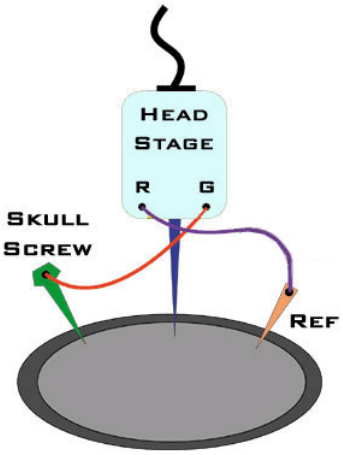
Headstage Operations	Description
Single-Ended	Ground and reference pins are tied together and the probe(s) reference all channels to ground.
Referential	Ground and reference pins are separate and the probes may use shared or multiple references.
Hybrid	A mixture of single-ended or referential operations when multiple headstages are used.

Single Headstage Configurations



Single Headstage with a Shared Ground and Reference

When using a single headstage with a shared ground and reference, the ground and reference pins of the headstage should be tied together. A ground is used and attached to a skull screw. All recordings will reference this connection. This configuration is referred to as "Single-Ended".

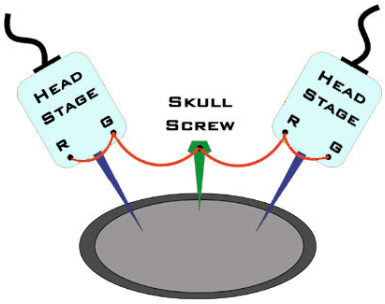


Single Headstage with a Separate Ground and Reference

When using a single electrode with a separate ground and reference, it is important that the headstage itself is not single-ended, that is, its ground and reference pins are NOT tied together. This will allow the headstage to reference each channel to ground as well as an additional chosen site on the subject. This configuration is referred to as "Referential"

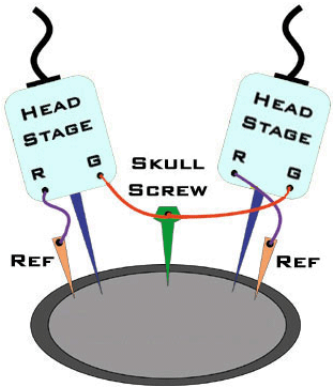
Multiple Headstage Configurations

Note: All headstages must use the same Ground wire. But not all headstages need to use the same Reference wire.



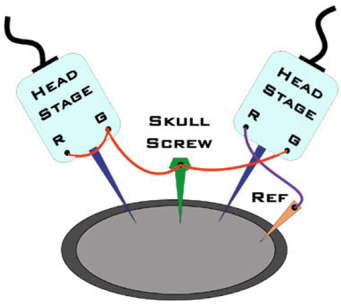
Multiple Headstages with a Shared Ground or Reference

When using multiple headstages with a shared ground or reference, the ground and reference pins of each headstage should be tied together. A ground is used and attached to a skull screw. This ground is used by all headstages and ensures the headstages are referencing the same potential. This is a multiple single-ended configuration.



Multiple Headstages with a Single Ground and Multiple References

This configuration uses multiple referential headstages each with their own separate references. Notice that all the headstages' ground pin are tied together. This is a multiple referential configuration.



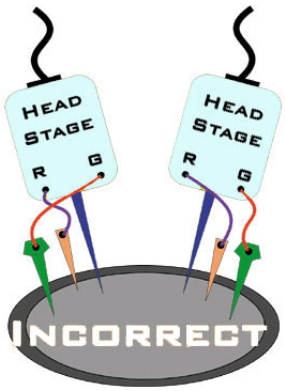
Multiple Headstages with a Shared Ground and different Ground/Reference configurations

When using multiple electrodes with a shared ground and separate reference, all headstages' grounds are connected to the skull screw. A reference wire is present and connected to the desired headstage. This ensures all headstages have the same ground potential and provides a reference for the desired headstage. This is a hybrid configuration and uses a mixture of single-ended and referential headstages.

Alternatively, to use a single reference for all headstages you may tie all headstage reference pins to the site labeled "Ref".

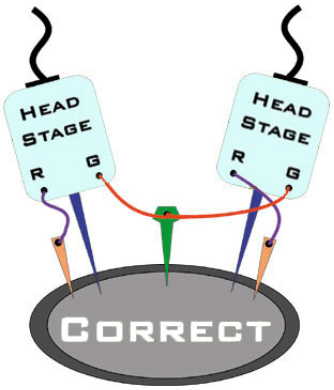
A Common Error to Avoid

When using multiple headstages a common error is to connect separate grounds for each headstage. This allows additional noise to corrupt signals increasing the number of artifacts present. To avoid this, ensure that all headstage ground pins are wired as a single ground.



Incorrect Configuration

Both headstages are connected to a unique node for ground. This will introduce additional noise artifacts into the recordings.



Correct Configuration

These headstages are correctly sharing a single node for ground. All headstages will be able to reference the same ground and will eliminate unnecessary noise artifacts from the recordings.

TB32 32-Channel Digitizer

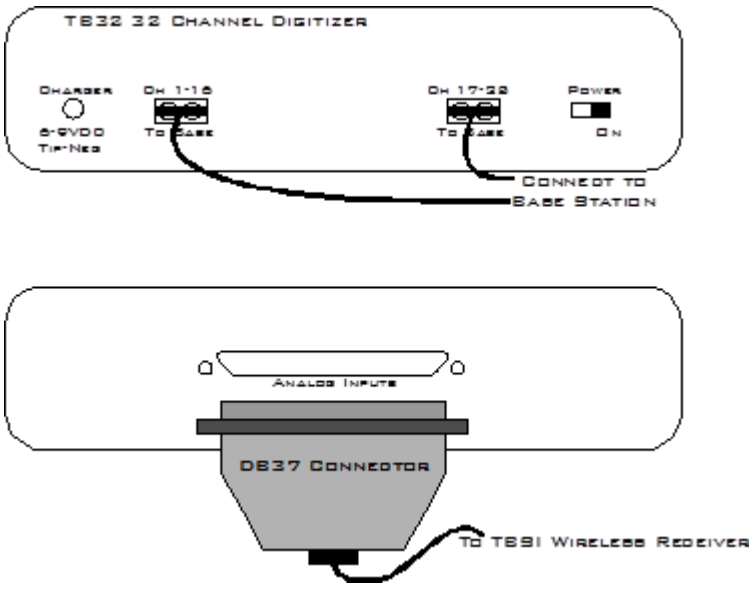
TB32 Overview

The TB32 32 channel digitizer interfaces directly with Triangle BioSystems, Inc. (TBSI) wireless headstage and receiver allowing up to 31-channels of recording from a free moving subject.

TBSI's wireless headstage captures the analog signals and wirelessly transmits them up to 3 meters from the subject to the TBSI receiver. The analog signals are then passed to the TB32 for digitization through a 37-pin connector. Signals are digitized at up to ~25 kHz on the digitizer and sent over two fiber optic links to a DSP device such as the RZ5 base station, where they are filtered and processed in real-time.

Hardware Setup

The diagram below shows the connections made to the front and back panels of the TB32 digitizer.



TB32 Front (top) and Back (bottom) Panels

TB32 Features

Analog Acquisition Channels

The TB32 acquires signals using 16-bit sigma-delta As, which provide superior conversion quality and extended useful bandwidths, at the cost of an inherent fixed group delay. Each converter has a two-pole anti-aliasing filter (12 dB per Octave) at 4.5 kHz.

Note: The TB32 16-bit sigma-delta A/D converters contain a 20 sample group delay.

Scale Factor

To determine the actual biopotential from the TB32, two scale factors should be applied in the DSP. The first scale factor is 400. This is used to convert the input from the TB32 into the standard voltage range expected by the DSP. The second scale factor is used to scale the signal according to the amplification of the TBSI headstage and receiver.

This can be simplified into a single conversion of $400/ G^{TBSI}$

Where G^{TBSI} = Gain of TBSI wireless headstage and receiver

Headstage Connector

The headstage connector is a 37-pin (31-channel) female connector. Information on the pin inputs is provided with "TB32 Digitizer Technical Specifications" on page 7-103.

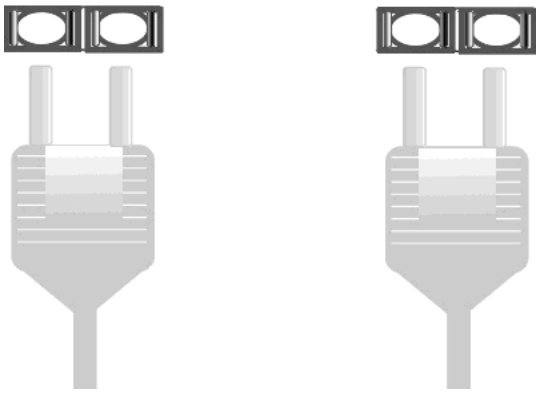
Base Station Connectors - To Base

One end of the fiber optic cable connects to the digitizer and the other end connects to the digitizer (amplifier) input on the base station. Two fiber optic base station connectors are provided. Connect each fiber optic cable as shown below.

Each connector on the TB32 is labeled and corresponds to the channels of the wireless headstage. Refer to the System 3 Manual for specific device channel configurations.

Digitizer Output to Base Station

Base Station Connector for Digitizer Input



Power Switch

A switch on the front panel powers up the digitizer. The power light and fiber connectors at the left will be illuminated when the digitizer is on.

Power Light

The power light is illuminated when the device is on. It flashes quickly if the battery is low. It flashes slowly while the battery is charging.

Power Requirements

Onboard lithium-ion batteries charge in ten hours. Keeping the battery charger connected to the digitizer does not affect the battery life. However, the charger will significantly increase the noise of the system if it is plugged in while an experiment is running. A 6 Volt battery charger is included with the digitizer. The charger tip is center negative.

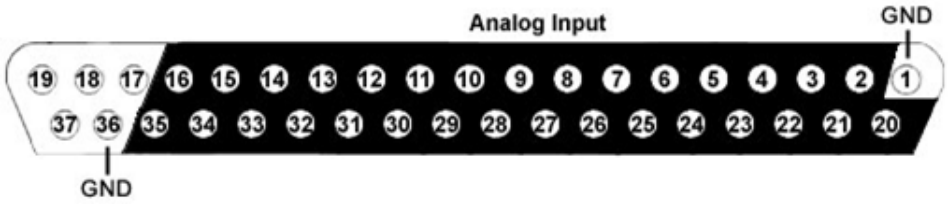
The Li-ion battery supplied with the system cannot be removed. If battery life longer than 20 hours is required, contact TDT for more information.

TB32 Digitizer Technical Specifications

A/D	31-channels: 16-bit sigma-delta
Maximum Voltage In	+/- 2 Volts
Frequency Response	3 dB 2.2 Hz - 4.5 kHz
Highpass Filter	2.2 Hz
Anti-Aliasing Filtering	4.5 kHz (3 dB corner, 2nd order, 12 dB per octave)
S/N (typical)	74 dB
Input Referred Noise (Re 2V)	rms 400 microvolts bandwidth 300 - 3000 Hz* 1 millivolt bandwidth 30 - 5000 Hz*
Group Sample Delay	20 Samples
A/D Sample Rate	6, 12, or 25 kHz
Input Impedance	10^5 Ohms
Power Requirements	500 mAmps while charging, 50 mAmps once charged
Battery	Li-Ion Polymer Battery 5000 mAh, 20-30 hours between charges.
Charger	6-9 Volts , greater than 500 mAmps, center negative
Fiber Optic Cable	5 meters standard, maximum cable length 20 meters

***Note:** Given the standard gain on the TB32 these values are 1 uV and 2.5 uV respectively.

Pinout Diagrams



Pin	Name	Description		Pin	Name	Description
1	GND	Ground		20	A1	Analog input channels 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31
2	A2	Analog input channels 2,4,6,8,10,12,14,16,18, 20,22,24,26,28,30		21	A3	
3	A4			22	A5	
4	A6			23	A7	
5	A8			24	A9	
6	A10			25	A11	
7	A12			26	A13	
8	A14			27	A15	
9	A16			28	A17	
10	A18			29	A19	
11	A20			30	A21	
12	A22			31	A23	
13	A24			32	A25	
14	A26			33	A27	
15	A28			34	A29	
16	A30			35	A31	
17	NA	Not Used		36	GND	Ground
18	NA			37	NA	Not Used
19	NA					

Note: No connections should be made to pins 17, 18, 19, and 37.

PZ5-BAT External Charger

PZ5-BAT Overview

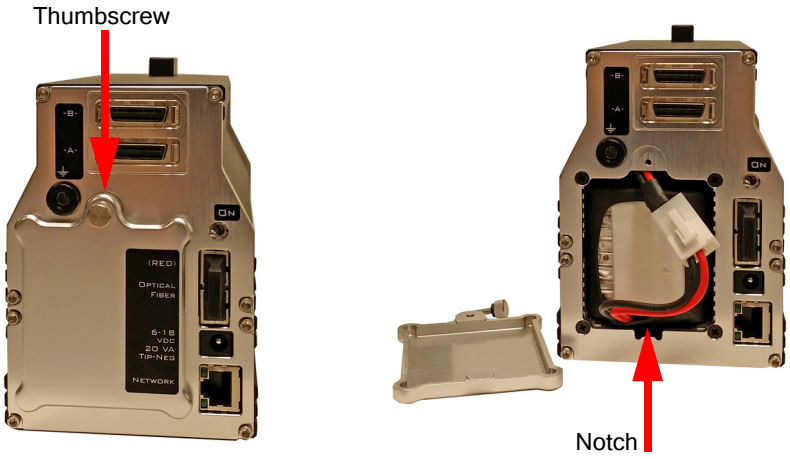
The PZ5-BAT is an external battery charger for the PZ5 NeuroDigitizer's 32 Amp-hour Lithium ion, user serviceable, battery pack. The PZ5-BAT unit is comprised of an off the shelf, programmable charger that has been pre-programmed for use with the PZ5 battery pack and a custom connector cable.

Using the Charger

Before using the external charger, you will often need to remove the battery pack from the device. The PZ5 battery cover is located on the back side and is held on by a single thumbscrew at the top and a simple notch at the bottom.

To remove the battery pack:

1. Unscrew the thumbscrew then lift and pull away the battery cover.



2. The connector between the batter pack and the device will be immediately visible. Press down on the tab to release the connection then gently pull the battery pack free from the device.

To charge the battery:

1. Power on the charger by plugging it in to AC power with the provided cable.

   Upon power up, verify the display reads "LiPo CHARGE" on the first line and then "3.5A" and "3.7V(1S)" on the second line.

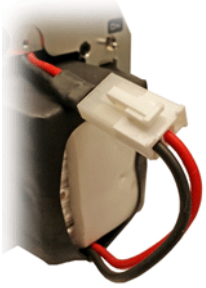
   Note: If this message is NOT displayed see "Charger Programming Instructions" below.

2. Plug the battery pack into the charger using the custom connector cable.

3. Press and hold the **ENTER (Start)** button to begin. The charger will check the battery to verify that it is okay to charge.
4. When the check is complete, press the **ENTER (Start)** button again to CONFIRM and then it will begin to charge.
5. Charging will stop (no numbers changing on the display) when the battery pack is fully charged.

While the battery pack is charging you can install an alternate pack in the PZ5 or when charging is complete re-install the charged pack.

To install a battery pack:



1. Connect the pack's cable to the PZ5 cable. The connectors are keyed to prevent miswiring and snap in place when securely connected.
2. Gently slide the battery into the unit. Ensure that the cable is tucked inside the opening.
3. Line-up the tabbed end of the cover with the notch at the bottom of the opening and slide it into position.
4. Use the thrumbscrew to securely attach the cover.

Charger Programming Instructions

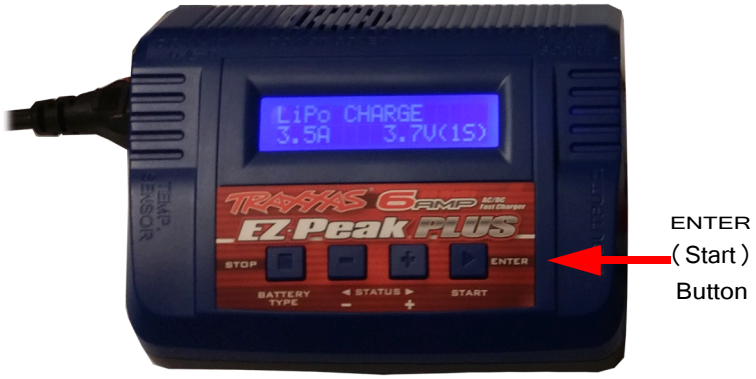
When powering on the charger the display should read:

LiPo CHARGE

3.5A 3.7V(1S)

If the expected message is not displayed, the settings may have been erroneously changed and it may be necessary to re-program the unit.

Before re-programming, try pressing the **ENTER (Start)** button. If the display changes to display the beginning message above, return to the charging instruction, step 2.



To program the charger:

1. Upon power up, press and hold the **BATTERY TYPE** button until the display reads, **"PROGRAM SELECT LiPo BATT"** then press the **ENTER (Start)** button.

2. Verify the display reads “LiPo CHARGE” on the first line and then “3.5A” and “3.7V(1S)” on the second line.
3. If the display does not read 3.5A, then press the **ENTER (Start)** button to change the charge rate. Press the ‘**+**’ plus or ‘**–**’ minus Status buttons to adjust the value to **3.5A**. When 3.5A is displayed, press the **ENTER (Start)** button.
4. Verify that **“3.7V”** is blinking. If not, use the ‘**+**’ plus or ‘**–**’ minus Status buttons to adjust the value to 3.7V and then press the **ENTER (Start)** button.

   ```
   LiPo CHARGE

   3.5A      3.7V(1S)
   ```

5. Press the **BATTERY TYPE** button until the display reads, “USER SET PROGRAM”. Then press the **ENTER (Start)** button.

   ```
   USER SET

        Program->
   ```

6. Press the ‘**–**’ minus Status button (4 times) until the screen reads “SAFETY TIMER”.
7. Press the **ENTER (Start)** button and then press the ‘**+**’ plus Status button to set the timer to “OFF”.
8. Press the **ENTER (Start)** button twice and verify that “OFF” is no longer flashing.

   ```
   SAFETY TIMER

   OFF    120min
   ```

9. Press the ‘**+**’ plus Status button (once) until the screen reads “CAPACITY CUT-OFF”
10. Press the **ENTER (Start)** button twice and then press the ‘**+**’ plus Status button to change the capacity to “40000 mAh”.

    ```
    CAPACITY CUT-OFF

    OFF    40000mAh
    ```

11. Press the **ENTER (Start)** button and verify that “40000” is no longer flashing.
12. Press the **BATTERY TYPE** button (twice) until the display reads, “PROGRAM SELECT LiPo BATT”. Then press **ENTER (Start)** button.
13. Verify the screen displays the following:

    ```
    LiPo CHARGE

    3.5A      3.7V(1S)
    ```

The charger is ready to use.

PZ-BAT External Battery Pack for the PZ Amplifiers

PZ-BAT Overview

An external battery pack is available for use with the PZ amplifier. Ideal for long recording sessions, the PZ-BAT provides 42 AmpHours and requires 8-10 hours to charge to 95% capacity and 14 hours to fully charge.

Charging the Batteries

A 100-240 VAC, 50-60HZ 2A(MAX) power connection socket is provided on the back or the PZ-BAT. Connect to AC power to charge.

Using the External Battery Pack

The DC power output cable on the front panel can be connected directly to the round female charger socket on the back panel to a PZ amplifier.

Set the three position switch on the front of PZ amplifier to either the A or B position to power on the PZ amplifier. When the PZ-BAT is connected the PZ's Battery Status LEDs will behave as if the internal batteries are charging.

Important! To avoid introducing EMF noise, DO NOT connect the PZ-BAT to AC power while connected to a PZ amplifier that is collecting data.

PZ-BAT Technical Specifications

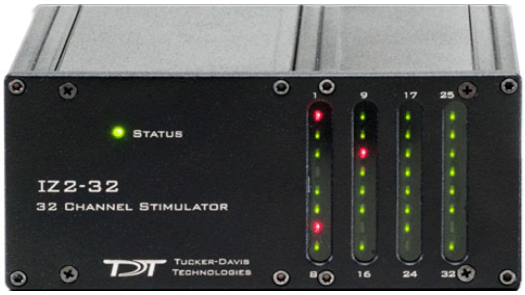
External battery performance:	
# of Ch	PZ_BAT
32	55 hrs
64	46 hrs

96	40 hrs
128	34 hrs
256	21 hr
Charger:	internal 6V, 3A power supply

Note: All time values are typical.

Part 8: Stimulus Isolator

IZ2/IZ2H Stimulator



IZ2 Overview

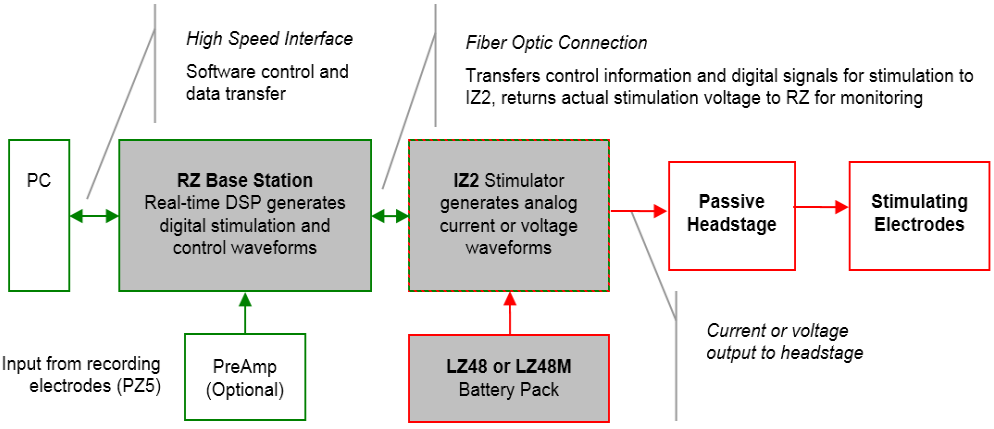
The IZ2 Stimulator converts digital waveforms into analog waveforms as part of a computer-controlled neural microstimulator system that delivers user-defined stimuli through up to 128 electrodes. The IZ2 can output either a voltage-controlled waveform or a current-controlled waveform and provides feedback of the actual voltages delivered to the electrodes.

The IZ2H is a high current range version of the IZ2.

The IZ2 Stimulator System

A typical system consists of a Stimulator (IZ2-32, IZ2-64, IZ2-128, or IZ2H-16); a Battery Pack (LZ48-200, LZ48-400, LZ48M-250, or LZ48M-500); and an RZ processor equipped with a specialized DSP (RZDSP-I) and additional fiber optic connector on the back panel.

The block diagram below illustrates the functionality of the system.



Multichannel IZ2/IZ2H Stimulator System Diagram

Stimulation control waveforms for each electrode channel are first defined on the RZ base station and digitally transmitted over a fiber optic cable to the battery powered stimulator. On the stimulator, specialized circuitry for each electrode channel generates an analog voltage waveform.

In Current mode, the driving voltage is adjusted to produce the desired current regardless of the electrode impedance, within bounds.

Onboard Analog-to-digital (A/D) converters on the IZ2/IZ2H read the output voltage and a chosen bank of eight channels is sent back to the RZ for monitoring.

In Current mode, the IZ2 Stimulator System can deliver up to 300 µA of current simultaneously across up to 128 stimulating electrodes (impedance up to 50 kOhm). The IZ2H Stimulator System can deliver up to 3 mA of current simultaneously across up to 16 stimulating electrodes (impedance up to 5 kOhm).

In Voltage mode, both the IZ2 and IZ2H can deliver up to +/-12V across each individual electrode.

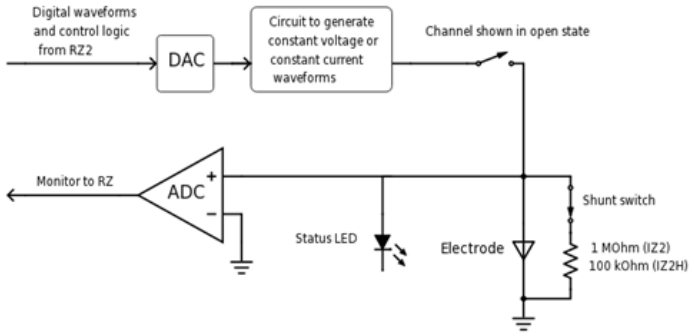
Special features for IZ2 serial numbers > 2000 and all IZ2H devices:

- Individual channels can be open circuited or shorted to ground.
- A shunt resistor to ground can optionally be switched on all channels. This is most useful for electrodes with very high impedance at DC that would normally produce large quiescent voltages when in Current mode. The IZ2 shunts are 1 MOhm each, the IZ2H shunts are 100 kOhm.

The Stimulator System

The IZ2 stimulator features 32, 64, or 128 channels that can deliver arbitrary waveforms of up to 80 kHz bandwidth. The IZ2H features 16 channels for high current range stimulation. Each channel uses PCM D/As to ensure sample delays of only 4 samples.

Special circuitry on the IZ draws on the LZ high voltage inputs to convert low voltage waveforms from the D/A converters to constant voltage or constant current waveforms as shown in the diagram below. The LZ battery pack also provides the power to run the IZ logic control.



Stimulator Diagram

Stimulator Batteries

There are two types of compatible battery packs, the LZ48 and the LZ48M that make up the four models of available batteries (LZ48-200, LZ48-400, LZ48M-250 or LZ48M-500). All batteries produce the same output voltage/current characteristics for powering the IZ2, but differ in battery life and features.

When using the LZ48 battery pack, the IZ2 uses the V_C battery for logic control. V_A and V_B batteries are used to drive the positive and negative stimulation waveforms.

The LZ48M battery pack is a single battery bank that drives both the logic control and the waveform output, and includes additional over-current fault protection. IZ2 and IZ2H devices manufactured before 07/13/2017 require a firmware update to operate with LZ48M batteries.

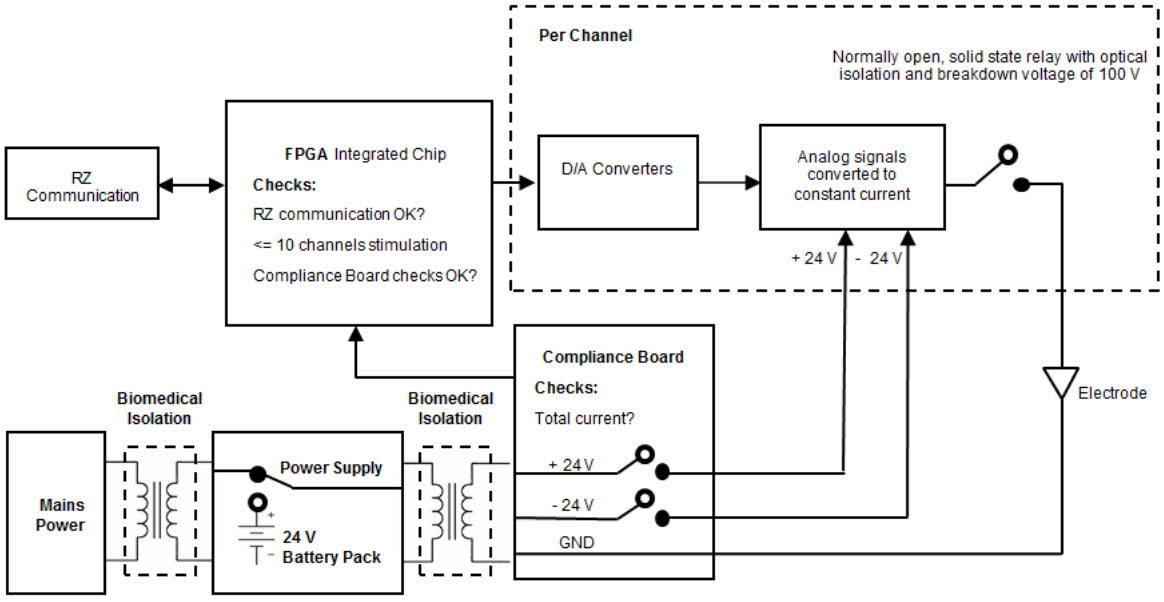
The number of channels needed for stimulation determines power requirements. The IZ2-128 and IZ2H-16 should only be used with the LZ48-400 or LZ48M-500. The IZ2-32 and IZ2-64 can be used with any LZ battery.

See "LZ48 Battery Reference" on page 8-18, for technical specifications and for more information.

Safety (LZ48M Version Only)

The LZ48M battery pack's robust safety profile includes both software and hardware components. Control software ensures that the device always boots in safe-mode, meaning all channels power up by default with their relays open. The relays are kept open until the device finishes booting, passes all internal safety checks, and is armed by the user. This ensures absolutely zero current can flow until proper software control is established. During operation, control software ensures that no more than 10 of the channels can be enabled for stimulation at the same time and that maximum output current is not exceeded.

At the hardware level, the stimulator features an air flow system to regulate temperature and a power supply monitoring system. These systems are controlled on an independent compliance board that will not allow stimulation currents to flow unless all safety checks are met.



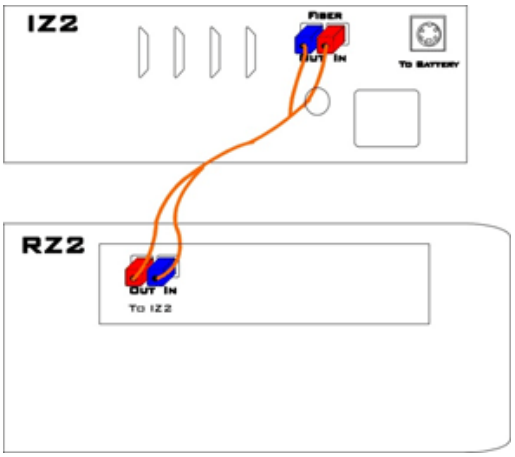
LZ48M Functional Safety Diagram (with IZ2 or IZ2H Stimulator)

The stimulator's power supply has been validated to ensure 4,000 volts of isolation between the input and output, 1,500 volts of isolation between the input and ground, and 500 volts of isolation between the output and ground.

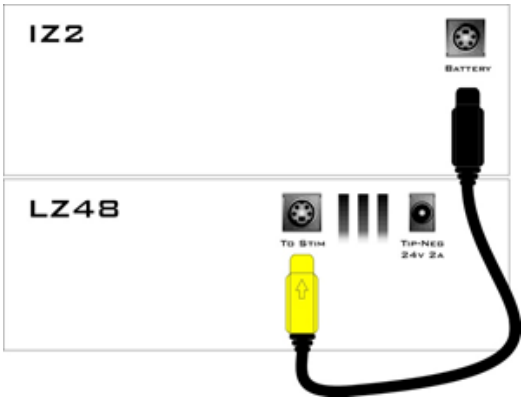
Hardware Set-up

The IZ2 Connection and Boot Procedure

1. Ensure that the TDT drivers, PC interface, RZ and zBus devices are installed, setup, and configured according to the installation guide provided with your system.
2. Connect the stimulator to the base station using the provided fiber optic cable. If using an RZ2 or RZ6 base station, connect the fiber optic cable from the IZ2 fiber optic port labeled 'Fiber' to the fiber optic port labeled 'To IZ2' on the back side of the RZ. If using an RZ5D base station, connect the fiber to the 'IZ' port on the front of the RZ5D. Be sure to note the difference in the two sides of the fiber optic cable connectors and ensure they are inserted with the correct side up.



3. Power on the RZ base station.
4. Verify that the subject is NOT connected to the IZ2 stimulator.
5. Verify that the LZ48 battery is off and connect the battery pack cable to the back panel of the stimulator via the connector labeled **Battery**, as shown in the diagram below.



WARNING! Shorting the battery connection pins can cause damage to the device and injury to the user. Always use caution when handling or connecting the devices.

6. Connect the DB26 output connectors on the stimulator to the stimulating electrodes using your preferred method such as direct wiring or a custom

pass through connector (available from TDT). See "IZ2 Stimulator Technical Specifications" on page 8-14, for pinouts.

7. If you are not using an LZ48M, skip to step 11. The LZ48M has configuration pins on the back of the device.

These switches must be correctly set according to **the number of channels currently connected to the IZ2 (NOT the total number of channels that the IZ2 supports)** and for the IZ2 device type (IZ2 vs IZ2H). The LZ48M uses this information to determine if the IZ2 is safe to operate. Start with all switches in the 'Off' position (down) and turn on switches according to the table below.

Device	# Banks	Channels	Pin Configuration
IZ2H	1	up to 8	Pin 6 ON
IZ2H	2	up to 16	Pins 1, 6 ON
IZ2	1	up to 16	Pin 1 ON
IZ2	2	up to 32	Pins 1, 2 ON
IZ2	3	up to 48	Pins 1, 3 ON
IZ2	4	up to 64	Pins 1, 2, 3 ON
IZ2	6	up to 96	Pins 1, 2, 4 ON
IZ2	8	up to 128	Pins 1, 2, 3, 4 ON

8. If operating the IZ in voltage mode, turn Pin 8 ON. This also bypasses the over-current fault detection in the LZ48M.
9. Press the LZ48M power button. The red Fault light should activate, after about five seconds the green Ready light should activate and the Status light on the IZ2 should turn orange. If Pin 8 is ON, the Ready light will flash green. If Pin 8 if OFF, the Ready light will be solid green.
10. If the Ready light is on but the IZ2 status light is blinking green, check the optical connection to the IZ2 and try again.
11. If using an LZ48, power on the LZ48 using the power switch on the LZ48's front panel. This will also power on the stimulator.

    Note: Ensure that the LZ48 rechargeable batteries are fully charged before starting your protocol.

12. Wait at least five minutes to ensure the IZ2 is at calibrated temperature. The IZ2 stimulation circuitry is heat sensitive and is calibrated at TDT after it has warmed up and reached temperature equilibrium.
13. Initiate your recording session in Synapse or OpenEx. By default, your protocol design should have zero current output and all IZ2 channels should be in the 'Open' state before you begin stimulation. If the IZ2 status light is blinking green when you start your experiment, it is in a fault state. This is because either there are more than 10 channels activated or you are running in Voltage mode (this includes using the "IZ2 Ground" option in the Signal Injector gizmo in Synapse). If you require Voltage mode or more than 10 stim channels, turn Pin 8 to the ON position and repeat the boot cycle. See "Software Control" on page 8-11 for more information.

14. Connect headstage to the subject.
15. The hardware is ready to use.

If using the system with other devices, such as a switching headstage or preamplifiers, see the documentation for those devices for hardware connection information in the System 3 Manual.

Testing the System

The IZ2 system includes a resistor block that is used to verify stimulation output. The RB100 is a 100kOhm resistor block that is included with the IZ2. The RB10 is a 10kOhm resistor block that is included with the IZ2H. In Synapse, use the impedance test built into the IZ2n HAL object at run time to verify that the correct impedance is measured. Download the test files and instructions from http://www.tdt.com/files/tech/IZ2ImpedanceTest.zip. See “Software Control” on page 8-11 for more information.

Best Practices

We recommend enabling the shunt resistors via the IZ2 hardware setting in Synapse, or the IZ2_Control macro in OpenEx/RPvdsEx.

When a channel is not used for stimulation, TDT recommends setting it to “Open” unless a ground or zero state is specifically called for by the stimulation protocol. If a non-stimulating channel must be left connected, the user can use capacitive coupling (ACC16-Z device adapter) or enable the Shunt to minimize the effects of direct current on the electrode. This is highly recommended to reduce unnecessary current flow in the subject.

To minimize risk, never allow the LZ48 battery to fully discharge. When the battery charge indicator is getting low, stop the experiment (open all channels), disconnect the subject, and recharge before further use.

Always verify proper operation of your device before connecting to a research subject. If you observe a red Status light or blinking green Status light on your IZ2 during setup, do not connect a research subject or proceed with the experiment.

If you encounter any problems or need help verifying proper device operation, please contact TDT Technical Support for assistance at support@tdt.com.

Do’s and Don’ts

Always follow the system power up sequence described above.

Always monitor indicator lights and electrode voltages to verify proper device operation.

Always connect only the channels needed for stimulation, extra connections are a path for inadvertent current.

Always have your default system state programmed for zero current delivery and all output relays open.

Always be aware of battery level and discontinue use when level gets low.

Never power the system on while it’s connected to the subject.

Never connect the system to the subject while it’s in an unknown state.

Never disconnect or reconnect the battery pack while the system is on or while the subject is connected.

Never disconnect or connect headstages while the system on or connected to the subject.

Never deliver more total current than is safe.

Common Problems with LZ48M

IZ2 Status light turns off after some time

After successfully powering up, the IZ2 may turn back off if banks of channels are added or removed on the back of the IZ2. It is important that bank connections are secure during operation. If you want to add or remove banks, they must be established prior to powering the IZ2 and the LZ48M configuration pins must be switched accordingly, then repeat the LZ48M boot procedure.

LZ48M will not attempt to power on IZ2

After initially turning on the LZ48M, with the Fault light on (red), the LZ48M can only attempt to power the IZ2 once. Try fully turning off (hold power button) and back on (press once) the LZ48M, then pressing the power button (once more) to reattempt powering the IZ2.

IZ2 Status light blinking green

IZ2 has successfully been powered by the LZ48M, but has not been properly connected to a compatible DSP. Ensure that the optical connection has properly been established.

IZ2 Features

Analog Outputs (Stim Outputs)

The IZ2 is equipped with 32, 64, or 128 analog output channels, arranged in sixteen-channel banks that are powered down when no headstage is connected.

The IZ2H is equipped with 16 analog output channels, arranged in eight-channel banks that are powered down when no headstage is connected.

Stim Lights

The Stim Lights are located on the front plate of the IZ2/IZ2H and are labeled by channel number. Each LED indicates the voltage at the corresponding electrode site. The Stim Light will turn green when a channel has greater than +/- 150 mV at the output and will turn red when a channel output is beyond +/- 10 V.

Status Light

This LED provides connection and output mode information.

Light Pattern	Description
Solid Red	IZ2/IZ2H is not properly connected to RZ base station or cannot sync.
Solid Green	IZ2/IZ2H is properly connected to RZ and is operating in current mode.
Solid Green, Slowly Flashing Red	IZ2/IZ2H is properly connected to RZ and is operating in voltage mode.
Solid Orange	IZ2/IZ2H is properly connected to RZ and LZ48M.
Blinking Green	IZ2/IZ2H is correctly powered by the LZ48M but is in a fault state. If this occurs during LZ48M boot-up, check the fiber optic connection. If this happens during the experiment, check your experiment settings Step 13 of the boot sequence above.

Fiber Optic Port (Fiber)

The IZ2 is battery powered and optically isolated from the RZ base station. One end of the fiber optic cable connects to the IZ2/IZ2H fiber optic input port and the other end connects to a fiber optic port on the RZ base station. See “Hardware Set-up” on page 8-6.

Battery Input (Back Panel)

The stimulator uses an LZ battery pack for stimulation and to power the logic circuitry. The battery pack should be connected via the Battery connection on the back panel using the battery pack cable provided. See “Hardware Set-up” on page 8-6.

Power Switch (Front Panel of LZ)

The Power switch turns the power on or off. The status lights on the front panel will be illuminated when the IZ2/IZ2H is on.

External Ground (Back Panel)

A banana jack below the fiber optics on the back panel provides a connection to analog ground. This connection was added with IZ2-32 serial number 3011, IZ2-64 serial number 3001, IZ2-128 serial number 3003, and IZ2-16H serial number 2017. This external ground is optional and should only be used if there is no other ground connection to the subject, or if you need to connect the IZ2 and recording amplifier grounds together for noise reduction.

A cable kit is also provided to ensure cables used with the external ground are suitable for this use. Each kit includes one male to male banana plug cable and one male banana to alligator clip cable. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

An IZ2 Battery Interconnect cable with a ferrite bead is also included for use when using the external ground. For best results position the ferrite bead close to the LZ.

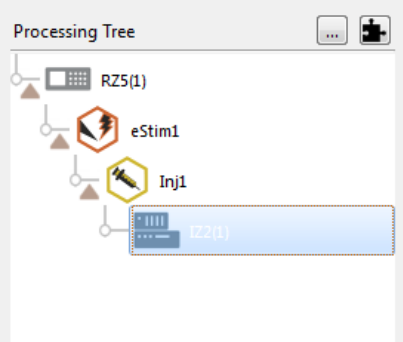
Software Control

Synapse

Operation of the stimulator system is controlled by an IZ2 object in the Synapse Rig and Processing Tree. Consult the Synapse Manual for more detailed information on general Synapse use.

Ensure that hardware your rig is properly set up in the Rig Editor (Menu > Edit Rig) and you have the required elements: RZ processor, DSPI (or DSPQ with optics) and IZ2 stimulator. Make sure the IZ2 object has the correct model selected (IZ2 or IZ2H) and channel count.

A typical electrical stimulation experiment includes an Electrical Stimulation gizmo to generate monophasic or biphasic pulses, then a Signal Injector gizmo which routes this single channel signal to one or more channels in a multi-channel stream and determines what the non-stim channels are doing (typically set to "IZ2 Open" mode), and then this multi-channel stream connects to the IZ2 object to control all channels on the IZ2 at once.



Important Experiment Design Considerations

Sampling Rate

The IZ2 can control 128 channels at up to 50 kHz, 64 channels at up to 100 kHz, and 32 channels at a maximum 200 kHz. The IZ2/IZ2H sampling rate is the same as the sampling rate of the RZ device, so the maximum sampling rate of the IZ2/IZ2H is also limited to the maximum sampling rate of the type of RZ device controlling it.

Note: When sampling at 200 kHz, the channel stim lights and output monitoring are not available, and stimulation is limited to the first five channels of each bank of channels.

Signal Resolution

Signal resolution is dependent on the sampling rate used. PCM D/A converters allow users to generate precise pulsed signals, including square waves with durations of only 1 sample. When using the maximum sampling rate of ~200kHz, the sample period is 5.12 microseconds. The IZ2/IZ2H has an effective bandwidth of 80 kHz for continuous (non-pulsed) waveforms.

Designing the Stimulus Signal

The IZ2/IZ2H Stimulator system offers flexible stimulus delivery capable of generating complex patterns of pulses or arbitrary waveforms.

This allows you to make use of the full range of the stimulation gizmos in the Synapse library, or create your own user gizmo for custom stimulation patterns.

IZ2 Serial Number > 2000 or any IZ2H

The Signal Injector gizmo provides default values for the non-stimulating channels. This can be zero voltage (or current), open circuit, or channel shorted to ground. Use the IZ2 object settings to enable the shunt resistors on all channels and to toggle voltage or current mode.

Monitoring the Stimulation

PCM A/D converters on the IZ2/IZ2H monitor the actual output voltage and a chosen bank of eight channels is sent back to the RZ. This information is available from the output of the IZ2 object. The IZ2 runtime UI allows you to select which bank of eight channels is updating on the Monitor output (the rest of the channels of the Monitor output will be latched) by clicking on the column of LEDs.

Note: There is a single pole 16kHz lowpass filter on these inputs. The filter can affect impedance checking beyond 10 kHz.

Note: The onboard A/D converters provide the feedback clip at +/-20V, which is higher than any possible output signal in either voltage or current mode.

Important Notes Regarding the Channel Indicator LEDs

In current mode, the IZ2 can stimulate a maximum 300 uA per channel (up to 15 V) and the IZ2H can stimulate up to 3 mA per channel (up to 15 V) through the electrode and the return path.

Channels connected to ground (Fill Value set to 'IZ2 Ground' in the Injector gizmo) are switched into voltage mode and set to output 0V, so the monitored voltage will always be 0V and the LED status lights for grounded channels will remain dim.

Channels that are open circuit (Fill Value set to 'IZ2 Open' in the Injector gizmo) in current mode will follow the voltage in the tissue. This must occur so that no current flows across the electrode. The open circuit electrode then acts like a recording electrode that is following the voltage at the electrode tip. This may cause the LED for an Open channel to light up. For example, if there is a 15V potential relative to ground at the tip of an open circuit electrode, there must also be a 15V potential on the stimulator side of the electrode so that no current is flowing across that electrode. Therefore, an open channel nearby the stimulating channel may show a non-zero voltage on the voltage monitor. If this measured voltage is greater than +/- 150mV (which is likely to be the case), this will light the LED status light on an open channel.

Similarly, if you hold one channel to 0 uA (Fill Value set to 'Zero' in the Injector gizmo) and stimulate through another nearby channel, the voltage on the channel held at 0 uA must rise so that no current flows across the electrode. This will also light the LED status light on a channel set to 0 uA output.

If the headstage/adapter/electrodes are not in the subject, then the electrical circuit is incomplete and the impedance that the IZ2 sees on its outputs is very high. This

is enough to raise the output voltage and turn on the LED status lights. This is also true of electrodes that have very high impedance at DC - even though the IZ2 output noise floor is low, a high enough impedance at DC will cause a non-negligible DC current on the outputs. Therefore, we recommend enabling the Shunt resistors to reduce the DC current flow to the subject when attempting to stimulate through very high impedance electrodes.

IZ2 Stimulator Technical Specifications

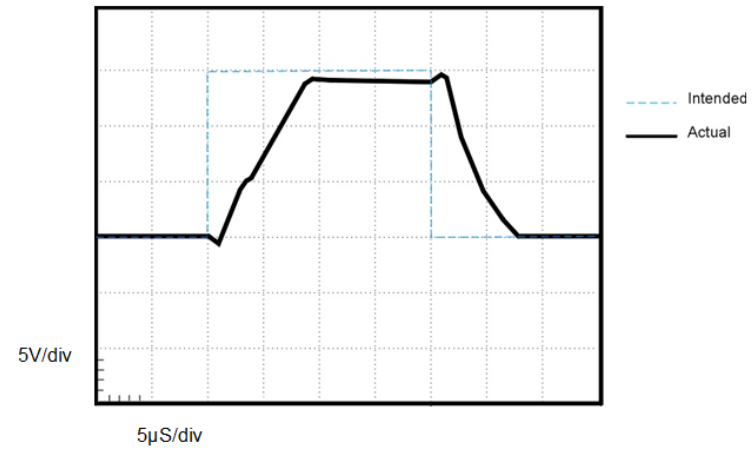
Includes specifications for the IZ2-32, IZ2-64, IZ2-128 and IZ2H-16.

Stimulus Output Channels	16 (IZ2H-16), 32 (IZ2-32), 64 (IZ2-64) or 128 (IZ2-128) PCM DACs
Sampling rate	IZ2H-16: Up to 195.3125 kHz^ IZ2-32: Up to 195.3125 kHz^ IZ2-64: Up to 97.65625 kHz^ IZ2-128: Up to 48.828125 kHz^
Stimulus Output Voltage	+/- 12 V in voltage-controlled mode
Stimulus Output Current	IZ2: +/- 300 µA up to 50 kOhm load IZ2H: +/- 3 mA up to 5 kOhm load
Offset Current	< 100 nA on active channels and < 3 nA on open channels
ADC Filter	Single pole 16kHz on voltage monitors
Power Control/Stimulation	LZ48 or LZ48M Rechargeable Battery Pack with Li-Poly batteries
Battery Life	LZ48-200 ~ 6-8 hours to charge LZ48-400 ~ 12-14 hours to charge Battery life between charges: LZ48-200 w/ IZ2: 2 banks (up to 32 ch) ~ 20 hrs 4 banks (up to 64 ch) ~ 10 hrs LZ48-400 w/ IZ2H: 1 bank (up to 8 ch) ~ 12 hrs 2 banks (up to 16 ch) ~ 6 hrs LZ48-400 w/ IZ2: 2 banks (up to 32 ch) ~ 30 hrs 4 banks (up to 64 ch) ~ 20 hrs 8 banks (up to 128 ch) ~ 10 hrs LZ48M-250 w/ IZ2: 2 banks (up to 32 ch) ~ 15hrs LZ48M-250 w/ IZ2H: 2 banks (up to 16 ch) ~ 15hrs LZ48M-500 w/ IZ2: 2 banks (up to 32 ch) ~ 30hrs LZ48M-500 w/ IZ2H: 2 banks (up to 16 ch) ~ 30hrs **Note:** The LZ48-200 is not recommended for use with the IZ2-128 or the IZ2H-16

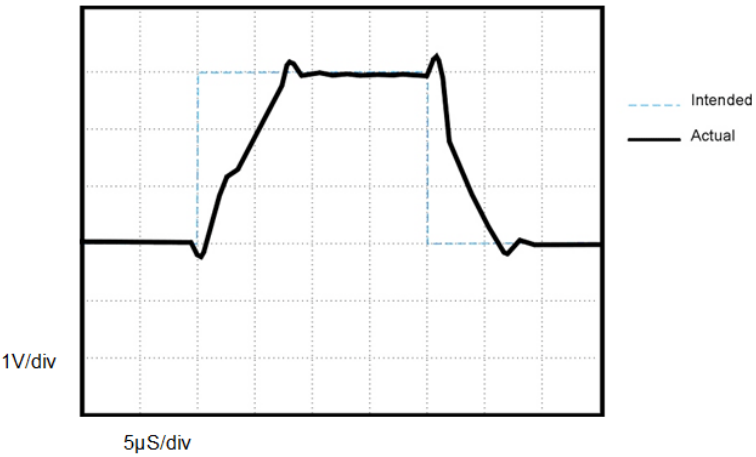
^Note: the sampling rate is also limited by the RZ processor used for stimulator control. When sampling at 195.3125 kHz, recording is limited to the first five channels on each bank of channels.

Slew Rate for the IZ2H-16

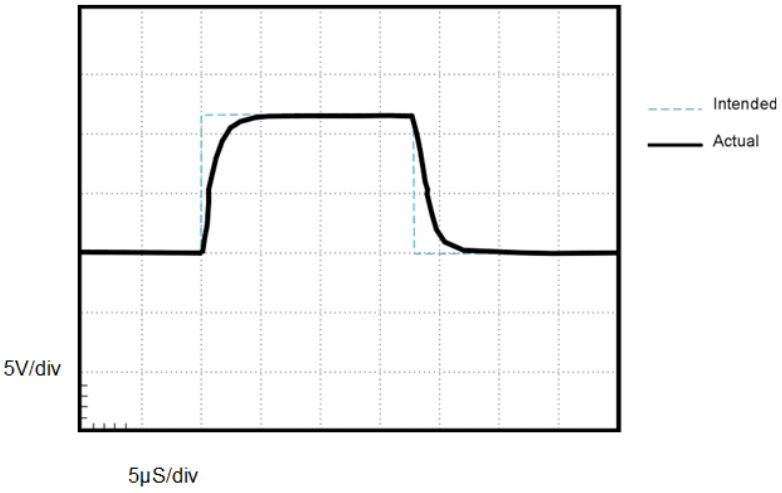
The slew rate is a measure of how quickly the output voltage of the device can change. The plots below show the effect of the slew rate on a square wave produced by the IZ2H at different loads and levels.



5k load, 3 mA stim, 50 kHz sampling rate. Slew rate: ~ 1.6 V/us
Devices SN < 2018: ~0.21V/us



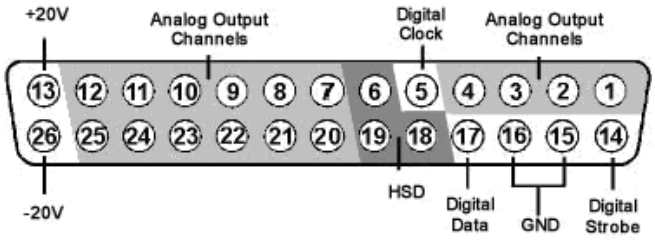
1k load, 3mA stim, 50kHz sampling rate. Slew rate: ~0.38V/us



5k load, 12V stim, 50kHz sampling rate. Slew rate: ~2.0V/us
Devices SN < 2018: ~ 0.16V/us

Note: Changes to the device improved the slew for IZH-16s, SN 2018 and greater.

Mini-DB26 Connector Pinouts for the IZ2

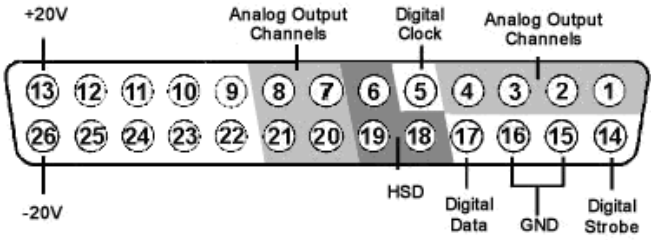


Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channels		14		Digital Strobe
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17		Digital Data
5		Digital Clock		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A5	Analog Output Channels		20	A6	Analog Output Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	V+	+20 V		26	V-	-20 V

Note: See this tech note before attempting to make any custom connections.

https://www.tdt.com/technotes/#0896

Mini-DB26 Connector Pinouts for the IZ2H



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channels		14		Digital Strobe
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17		Digital Data
5		Digital Clock		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A5	Analog Output Channels		20	A6	Analog Output Channels
8	A7			21	A8	
9		Not Connected		22		Not Connected
10				23		
11				24		
12				25		
13	V+	+20 V		26	V-	-20 V

Note: See this tech note before attempting to make any custom connections.

https://www.tdt.com/technotes/#0896

LZ48M Battery Reference

The LZ48M battery pack powers both the stimulation and the IZ2 stimulator logic circuitry. The LZ48M has built in protection circuitry to prevent over-current faults. The LZ48M charges from a standard wall plug.

Battery Capacity	LZ48M-250: 250 Whr. Up to 15 hr continuous stim on 2 banks (32 channels for IZ2, 16 channels for IZ2-H). LZ48M-500: 500 Whr. Up to 30 hr continuous stim on 2 banks.

Rechargeable	Yes
Compliance voltage	+/- 15V

Important! The LZ48M has configuration switches that must be set correctly based on your desired channel count and IZ2 configuration (IZ2 vs IZ2H). See Step 7 of the boot sequence above.

LZ48M Status LEDs

Fault: LZ48M has detected a fault and is not supplying voltage to the IZ2.

Ready: Solid green when stimulation is ready. Flashing green when ready for stimulation and in safety bypass mode (Config switch 8 is in the ON position).

The LZ48M uses mains power for charging. Connect the power connector on the back panel to a mains power outlet, using the provided AC power cable. The battery is always charging when connected to the mains power, regardless of whether the LZ48M is turned on.

There is a row of five LEDs next to the power button. The first LED from the left indicates whether the LZ48M is being powered from mains or battery power. The next four LEDs indicate the power level of the battery.

When the battery is fully charged, all four LEDs will be lit green. When the battery voltage is low, only one green LED will be lit. If the voltage drops further, the last LED will flash red. TDT recommends charging the battery before this flashing low-voltage indicator comes on.

LZ48M Battery Pack

The LZ48M Battery Pack uses Lithium Polymer (LiPoly) batteries.

WARNING! Just as with all batteries, shorting the LZ48M Battery Pack can cause damage to the device and injury to the user. Always use caution when handling or connecting the devices.

Important! Used LiPoly batteries must be recycled.

The LZ48M Battery pack should be stored at normal room temperatures. Temperature extremes can affect the operation of the batteries. Battery packs stored for longer than two months should be tested prior to use.

LZ48 Battery Reference

The LZ48 has three batteries to both drive the stimulation and power the IZ2 stimulator logic circuitry. A 24 Volt battery charger with 2.7A of current capacity is included with the stimulator and can be connected via the connector on the LZ48's back panel. The charger tip is center negative. If it is necessary to replace the charger, ensure that the power supply has the correct polarity.

	LZ48-200	LZ48-400
Battery Capacity	200 Wh	400 Wh
Rechargeable	Yes	Yes
Compliance Voltage	+/- 15V	+/- 15V
Maximum Impedance for a 300 microAmp Current	50 kOhms	50 kOhms
Ambient Temperature	Normal room temperatures	Normal room temperatures

LZ48 Status LEDs

V_A: Positive Battery Pole

V_B: Negative Battery Pole

V_C: Logic Battery Level

Eight LEDs indicate the voltage level of the currently displayed battery. When the battery is fully charged, all eight LEDs will be lit green. When the battery voltage is low, only one green LED will be lit. If the voltage drops further, the last LED will flash red. TDT recommends charging the battery before this flashing low-voltage indicator comes on. While charging, the Status LEDs will flash.

Status	Description
8 Green	Fully Charged
1 Green, 7 Unlit	Low Voltage
1 Flashing Red	Low Voltage - Charge Immediately!
8 Green Flashing	Charging in Progress

LZ48 Battery Pack

The LZ48 Battery Pack uses multiple Lithium Polymer (LiPoly) batteries.

WARNING! Just as with all batteries, shorting the LZ48 Battery Pack can cause damage to the device and injury to the user. Always use caution when handling or connecting the devices.

Important! Used LiPoly batteries must be recycled.

The LZ48 Battery pack should be stored at normal room temperatures. Temperature extremes can affect the operation of the batteries. Battery packs stored for longer than two months should be tested prior to use.

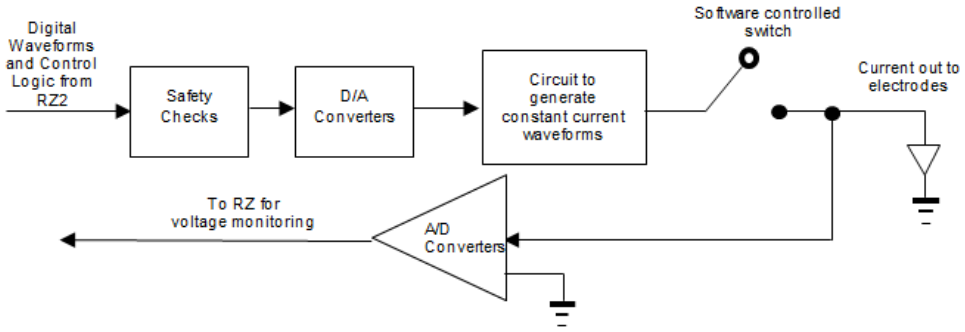
IZ2M/IZ2MH Stimulator

IZ2M/IZ2MH Overview

As part of a computer-controlled neural stimulator system, the IZ2M/IZ2MH outputs constant-current stimulation across multichannel electrodes and provides feedback of actual voltages delivered to the electrode. The stimulator converts user-defined digital waveforms to analog current and provides high precision electrical stimulus control. With up to 64 channels, the IZ2MH delivers a maximum of 3 mAmps (300 µAmps for the IZ2M) of current per electrode up to 12 V on up to ten electrodes simultaneously. The device is battery operated with alternative Mains power, used primarily for charging. Full medical grade isolation between the mains power and the electrode outputs ensures electrical isolation, and additional safety features ensure safe operation at all times.

Stimulation

The stimulator can deliver arbitrary waveforms at up to 50 kHz sampling rate. Each channel uses PCM D/As to ensure sample delays of only 4 samples and square edges on pulse stimulation waveforms. Stimulation control waveforms for each electrode channel are first defined on the RZ base station and digitally transmitted to the stimulator. Special circuitry on the stimulator converts voltage waveforms from the D/A converters to constant current waveforms as shown in the diagram below.



Stimulator Diagram

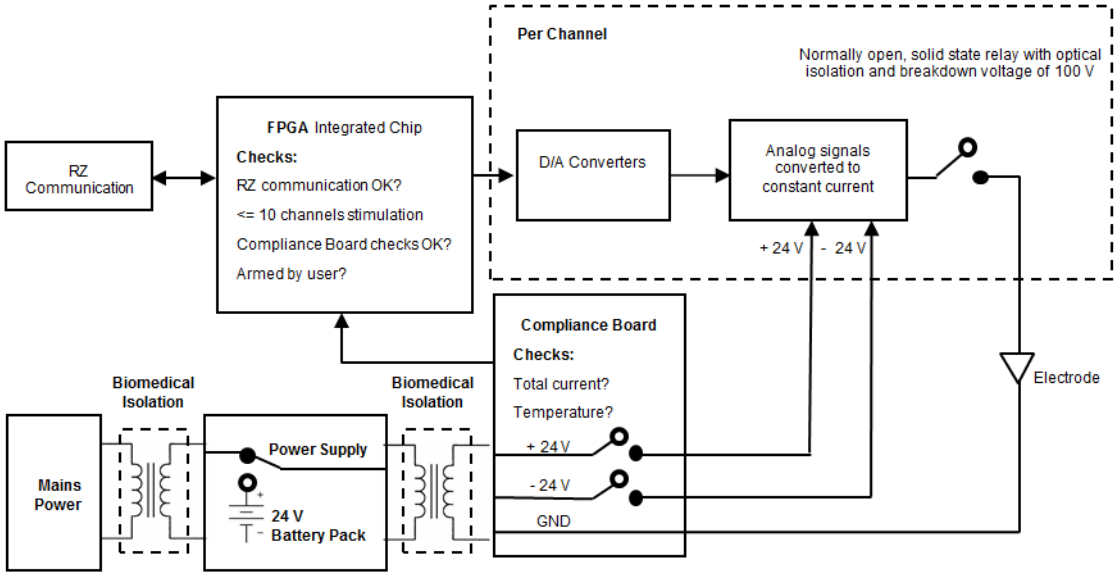
The driving voltage is adjusted according to Ohm's law (V=IR), where I is the desired stimulation current and R is the electrode impedance. Eight analog-to-digital (A/D) converters read the output voltage and send that information back to the RZ for monitoring.

Individual channels can be open circuited. A shunt resistor to ground can be applied to all channels (100 kOhm for IZ2MH and 1 MOhm for the IZ2M). This is most useful for electrodes with very high impedance at DC that would normally produce large quiescent DC voltages.

Safety

The IZ2M/IZ2MH's robust safety profile includes both software and hardware components. Control software ensures that the device always boots in safe-mode, meaning all channels power up by default with their relays open. The relays are kept open until the device finishes booting, passes all internal safety checks, and is armed by the user. This ensures absolutely zero current can flow until proper software control is established. During operation, control software ensures that no more than 10 of the channels can be enabled for stimulation at the same time and that maximum output current is not exceeded.

At the hardware level, the stimulator features an air flow system to regulate temperature and a power supply monitoring system. These systems are controlled on an independent compliance board that will not allow stimulation currents to flow unless all safety checks are met. An ARM/STOP button allows for manual safety override.



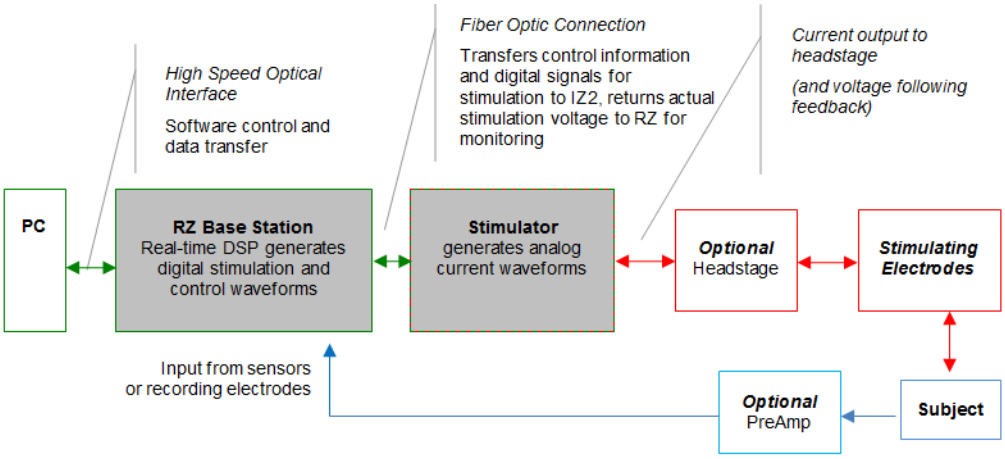
IZ2M/IZ2MH Functional Safety Diagram

The stimulator's power supply has been validated to ensure 4,000 volts of isolation between the input and output, 1,500 volts of isolation between the input and ground, and 500 volts of isolation between the output and ground. Safety approvals for the power supply include the following: UL60601-1, EN60601-1, CSA C22.2 No. 601.1 CE Mark LVD.

The Stimulator System

A typical system consists of an RZ processor equipped with a specialized DSP (RZ-DSP-I) and additional fiber optic connector on the back panel.

The block diagram below illustrates the functionality of the system.



Multichannel Stimulator System Diagram

Stimulation control waveforms for each electrode channel are first defined on the RZ base station and digitally transmitted over a fiber optic cable to the stimulator. On the stimulator, specialized circuitry for each electrode channel generates an analog voltage waveform. Analog-to-digital (A/D) converters read the output voltage for a chosen bank of 8 channels and send that information back to the RZ for monitoring.

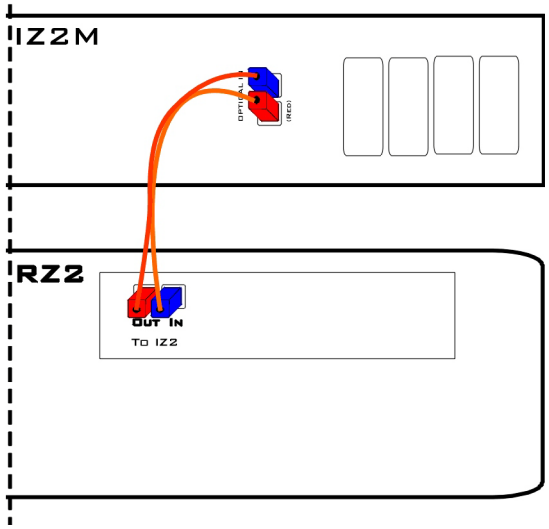
Hardware Set-up

To connect the system hardware:

Ensure that the TDT drivers, PC interface, and RZ and zBus devices are installed, setup, and configured according to the installation guide provided with your system.

Connect to RZ Base Station

Connect the stimulator to the base station using the provided duplex fiber optic cable.



Connect the fiber optic cable from the stimulator's fiber optic port labeled *Fiber* to the fiber optic port labeled *To IZ2* on the back side of the RZ. Use the RED labels to match up the color coded fiber connectors and be sure to line up the notch and keys on each.

Connect electrodes.

Connect the DB26 output connectors on the stimulator to the stimulating electrodes using your preferred method, such as direct wiring or a custom pass through connector (available from TDT). See "IZ2M/IZ2MH Stimulator Technical Specifications" on page 8-29, for pinouts.

Power on.

Power on the RZ base station, then power on the stimulator by pressing and holding the small square button to the left of the status lights. After one second, release the button.

The stimulator is powered on using battery for operation.

Important: The IZ2M/IZ2MH uses mains power for charging. Connect the power connector on the back panel to a mains power outlet, using the provided AC power cable. The battery is always charging when the mains power switch is in the ON position, regardless of whether the IZ2M/IZ2MH is turned on.

When battery power is turned on, the blue LED on the mains power switch, to the right of the status button, will be lit even when the mains power is off (used to indicate temperature). Verify whether mains power is on or off by looking at the position of the switch and by looking at the left-most power status LED. It will be red when the device is using battery power or green when the device is using Mains power.

The hardware is ready for use.

If using the system with other devices, or preamplifiers, see the documentation for those devices for hardware connection information.

Arming Sequence

Before the stimulator can be armed the RZ2 must be connected to the stimulator and powered on. If the stimulation circuit is loaded and running, it MUST not be actively sending stimulus signals on any channels.

The instructions below provide step-by-step sequence and more detail about each stage of device operation.

Step one. Boot—turn power on.

When the device is powered on (see above) the blue LED blinks until the device comes up to optimal temperature. This can take up to 10 minutes. If no faults are found at start-up, the stimulator may be armed before optimal temperature is reached (not recommended).

If a safety fault condition is found at start-up; the blue LED will blink at 1 Hz and the yellow LED will be off.

If a communication error, such as no signal detected from the RZ device, is found; or the RZ is trying to actively stimulate, the yellow Ready LED will blink.

When all safety checks have passed both the blue (mains power) and yellow (Ready) LEDs will be lit (no flashing). The device is ready to arm.

Step two. ARM—hold down the Start/Stop button for 3 seconds.

When the red LED flashes the Start/Stop button may be released and the red (Armed) LED will remain lit. If any fault is detected the red LED will not come on (or turn off) and the blue LED will begin to blink at 1 Hz.

Step three. Stimulate—send stimulation (up to 10 channels) from the RZ processor.

Once the device is armed, it is under the control of the RZ processor. If the RZ is not actively controlling the IZ2M, the default state is channels are closed and output set to zero current. The stimulator will deliver stimulation to the subject whenever stimulation signals are received from the RZ processor.

The stimulator faults and returns to safe mode (all channels open/no voltage output possible) if any of the below occurs:

- Stimulation is attempted on more than 10 channels.
- More than 100 mA total output is detected by the compliance board. Note: It is not possible to reach 100 mA under normal software controlled conditions.
- IZ2_Control macro is set to Voltage mode instead of Current mode.

See your software documentation for end user applications.

Step four. STOP—press Start/Stop button.

The user can press the *Start/Stop* button at any time to stop stimulation immediately and revert to safe mode.

Status LEDs

A blue LED is located on the on/off switch on the right side of the stimulator's front panel. It reports power on/off state and indicates temperature and over voltage faults. On the left side of the device, there is a Start/Stop button for arming the device with adjacent yellow (Ready) and red (Armed) LEDs that report any communication errors and armed status. Between the Battery on/off button and the Mains on/off switch there is a row of power status LEDs.

The chart below compiles the various stages of operation and blue, yellow, red LED status for each.

LEDs	Blue	Yellow	Red
Power on (Safe Mode)	blink (1 Hz – 50/50)	off	off
Ready to ARM	solid (w/temp flash*)	solid	off
Arming	solid (w/temp flash*)	solid	blink
Ready to Stim (Armed)	solid (w/temp flash*)	solid	solid
Safety Fault	blink (1 Hz – 50/50)	off	off
Communication Failure	solid	blink	off
Safety Fault and Communication Error	blink (1 Hz – 50/50)	off	off

*The Blue LED is primarily used to indicate power on/off and safety ok/fault. However, when the IZ2M/IZ2MH is actively stimulating (no faults) it also indicates temperature deviation from optimal by blinking off (short off duration) with the frequency of the off blink indicating the number of degrees off from optimal.

Power Status LEDs

Immediately to the left of the mains power button there is a row of small LEDs. The first LED (from left) indicates whether the devices is being powered from mains or battery power.

LED Color	Status
Green	the device is using mains power and the battery is charging.
Red	the device is using battery power.

The four LEDs on the right end of the row indicate the power level of the battery.

# of LED's Lit	Battery Power Level
4	Fully charged
3-2	Not fully charged
1	Critically low, charge immediately

The LED between the Power Mode LED and the Power Level LEDs is not used at this time.

Testing the System

The IZ2M includes a resistor block that is used to verify stimulation output. The RB100 is a 100kOhm resistor block that is included with the IZ2M. The RB10 is a 10kOhm resistor block that is included with the IZ2MH. In Synapse, use the impedance test built into the IZ2n HAL object at run time to verify that the correct impedance is measured. Download the test files and instructions from http://www.tdt.com/files/tech/IZ2ImpedanceTest.zip.

IZ2M/IZ2MH Features

Analog Outputs (Stim Outputs)

The analog output channels are arranged in sixteen-channel banks.

Stim Lights

The Stim Lights are located on the front plate of the IZ2M/IZMH and are labeled by channel number. Each LED indicates the voltage at the corresponding electrode site. The Stim Light will turn green when a channel has greater than +/- 150 mV at the output and will turn red when a channel output is beyond +/- 10 V.

Fiber Optic Port (Fiber)

The fiber optic input port provides an isolated connection to the RZ base station. One end of the fiber optic cable connects to the stimulator fiber optic input port (labeled Fiber) and the other end connects to the fiber optic input port (labeled To IZ2) on the back panel of the RZ base station. See "Hardware Set-up" on page 8-23, connection diagram.

Battery Operation and Charging

The stimulator has an onboard, 240 Wh battery for device operation. The battery charges whenever the Mains power is connected and the Mains power switch is in the on position.

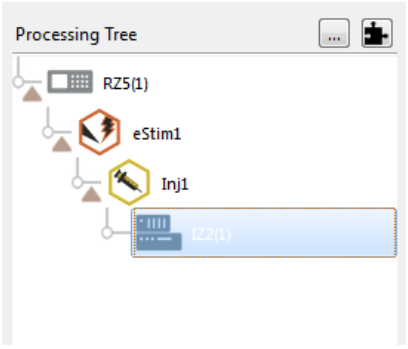
Software Control

Synapse

Operation of the stimulator system is controlled by an IZ2 object in the Synapse Rig and Processing Tree. Consult the Synapse Manual for more detailed information on general Synapse use.

Ensure that hardware your rig is properly set up in the Rig Editor (Menu > Edit Rig) and you have the required elements: RZ processor, DSPI (or DSPQ with optics) and IZ2 stimulator. Make sure the IZ2 object has the correct model selected (IZ2M or IZ2MH) and channel count.

A typical electrical stimulation experiment includes an Electrical Stimulation gizmo to generate monophasic or biphasic pulses, then a Signal Injector gizmo which routes this single channel signal to one or more channels in a multi-channel stream and determines what the non-stim channels are doing (typically set to "IZ2 Open" mode), and then this multi-channel stream connects to the IZ2 object to control all channels on the IZ2 at once.



Important Experiment Design Considerations

Sampling Rate

The IZ2M/IZ2MH can control 64 channels at up to 50 kHz. The stimulator sampling rate is the same as the sampling rate of the circuit running on the RZ device, so the maximum sampling rate of the stimulator is also limited to the maximum sampling rate of the type of RZ device controlling it.

Signal Resolution

Signal resolution is dependent on the sampling rate used. PCM D/A converters allow users to generate precise pulsed signals, including square waves with durations of only 1 sample.

Designing the Stimulus Signal

The IZ2M/IZ2MH Stimulator system offers flexible stimulus delivery capable of generating complex patterns of pulses or arbitrary waveforms.

This allows you to make use of the full range of the stimulation gizmos in the Synapse library, or create your own user gizmo for custom stimulation patterns.

The Signal Injector gizmo provides default values for the non-stimulating channels. This can be zero current or open circuit for the IZ2M/IZ2MH. Use the IZ2 object settings to enable the shunt resistors on all channels and to toggle voltage or current mode.

Ensure no more than ten channels have non-zero stimulus.

Monitoring the Stimulation

Eight PCM A/D converters on the stimulator monitor the actual output voltage for a chosen bank of channels and send that information back to the RZ. This information is available from the output of the IZ2_Control macro. The MonBank macro input specifies which bank of eight channels is updating on the Monitor output (the rest of the channels of the Monitor output will be latched). A zero indicates that the first bank of eight is monitored.

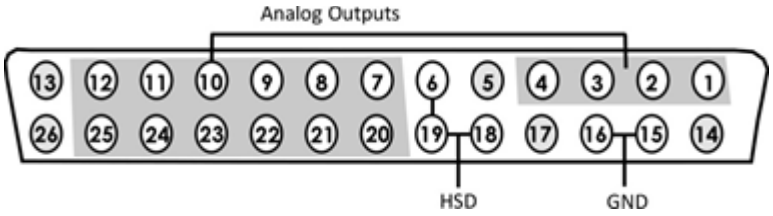
Note: The onboard A/D converters provide the feedback clip at +/-20V, which is higher than any possible output.

IZ2M/IZ2MH Stimulator Technical Specifications

Stimulus Output Channels	32 or 64
Sampling Rate	Up to 48.828125 kHz
Stimulus Output Voltage	+/- 12 V
Stimulus Output Current	IZ2M: +/- 300 µA up to 40 kOhm load IZ2MH: +/- 3 mA up to 4 kOhm load
Offset Current	< 100 nA on active channels and < 3 nA on open channels
Battery	240 Wh 20 hours to fully charge 16-18 hours to charge to 95% capacity 7.5 hours between charges

Mini-DB26 Connector Pinouts for the IZ2M/IZ2MH

Stim Output Connector



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channels		14		Reserved
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17		Reserved
5		Reserved		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	
7	A5	Analog Output Channels		20	A6	Analog Output Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13		Reserved		26		Reserved

Note: Contact TDT technical support (386-462-9622 or support@tdt.com) before attempting to make any custom connections to pins 6, 18, or 19.

MS4/MS16 Stimulus Isolator

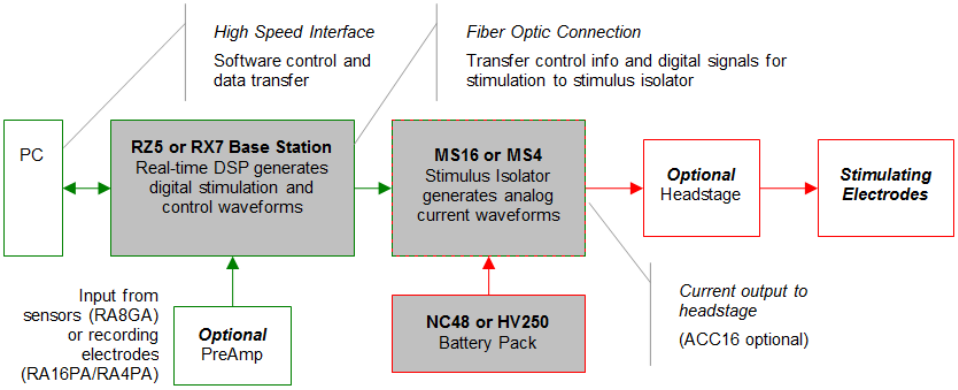
MS4/MS16 Overview

The MS4/MS16 Stimulus Isolator converts digital waveforms into analog current waveforms as part of a computer controlled neural microstimulator system that delivers user-defined current waveforms through multichannel electrodes.

The MicroStimulator System

A typical system consists of an RZ5 or RX7 processor base station (RX7 must be housed in a zBus Device Caddie with power supply and interface module), an MS4 or MS16 Stimulus Isolator, ACC16 AC Coupler (Optional) and NC48 or HV250 Battery Pack.

The block diagram below illustrates the functionality of the system.



Multichannel MicroStimulator System Diagram

As seen in the illustration above, stimulation control waveforms for each electrode channel are first defined on the base station and digitally transmitted over a fiber optic cable to the battery powered stimulus isolator. On the isolator, specialized circuitry for each electrode channel generates an analog current waveform as specified by the digital stimulation control waveform.

The final analog current output from the isolator is adjusted to match the stimulation control waveform by adjusting the isolator's driving voltage according to Ohm's law where: V=IR. That is, the driving voltage is adjusted for the stimulation control waveform level and the electrode impedance. In this way, the stimulation current specified by the user will be constant regardless of electrode impedance, within system limits.

The MicroStimulator System standard configuration is capable of delivering up to 100 µA of current simultaneously across up to 16 stimulating electrodes (impedance up to 1 Mohm). See "Working with the MS16 MilliAmp Mode" on page 8-46, for information if your stimulus isolator has been configured for MilliAmp mode.

The Stimulus Isolator

The stimulus isolator features either four or 16 D/A converters that can deliver arbitrary waveforms of up to 10 kHz bandwidth. PCM D/As are used to ensure sample delays of only 4-5 samples and square edges on pulse stimulation waveforms.

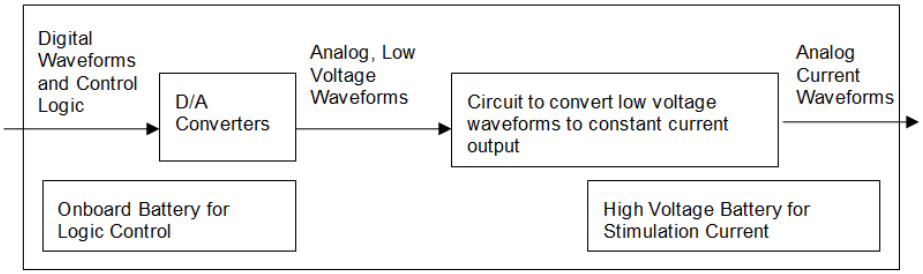
Each of the device's stimulation channels can be configured in one of three states:

Stimulate: Channels in stimulate mode pass current through the selected electrodes.

Reference: Channels in reference mode become part of the return path for the current. All channels in Reference mode use the same return path to analog ground on the stimulator. **Note:** Users can also use a dedicated global reference channel as a current return path. In this mode all channels can be used for stimulation.

Open: The Open mode is the default mode for all channels. In the open mode, the corresponding electrode channel is disconnected from output and internally grounded to eliminate noise and crosstalk. On multichannel electrodes, these electrodes might instead be connected to a recording preamp. In this mode a channel can be used to acquire neural signals.

The stimulus isolator utilizes an onboard, rechargeable Li-Ion battery for logic control and D/A converter operation. Special circuitry on the stimulus isolator draws on external high voltage battery packs to convert low voltage waveforms from the D/A converters to analog current waveforms as shown in the diagram below.



Stimulus Isolator Diagram

The ACC16 AC Coupler

The stimulus isolator may generate a DC bias current of up to 0.2% of full scale (up to 0.2 µA on 100 µA device) on any stimulation channel, even during a quiescent state. While this may not have significant short-term effects, over time, it may cause unintended tissue damage. This problem primarily affects researchers using electrodes with impedance of more than 100 kOhms. Users may connect the ACC16

AC coupler (supplied with all MS4/MS16s) directly to the Stim Output connector on the stimulus isolator to block any bias present on the Stim Output lines.

Note: Single-ended operation (G and Ref jumper pins tied together) is the only mode supported on the ACC16.

Each channel of the ACC16 coupler includes an RC circuit with a 0.1µF capacitor in parallel with a one MOhm resistor. The coupler acts as a 1.6 Hz highpass filter, eliminating the DC bias current. It also acts as a voltage divider, decreasing the voltage and thus the current delivered through the electrode.

Note: When using the ACC16 you will NOT be able to deliver the MAXIMUM Rated current. See "Designing the Stimulus Signal" on page 8-37, for more information.

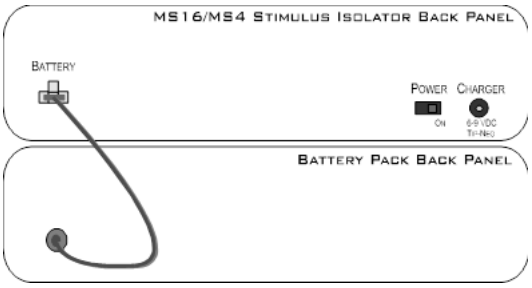
Stimulus Isolator Batteries

Power for stimulation is supplied by one of TDT's battery packs. Power requirements are determined by the amount of current needed for stimulation and the impedance of the electrode being used. When using a high impedance electrode (approximately 1 MOhm), the HV250 Battery Pack will most likely be required. With lower impedance electrodes (100 kOhms to 200 kOhms), the NC48 Battery Pack may be more suitable. Users should contact TDT for further information before attempting to use an external power supply. See "Battery Reference" on page 8-49, technical specifications and for more information.

Hardware Set-up

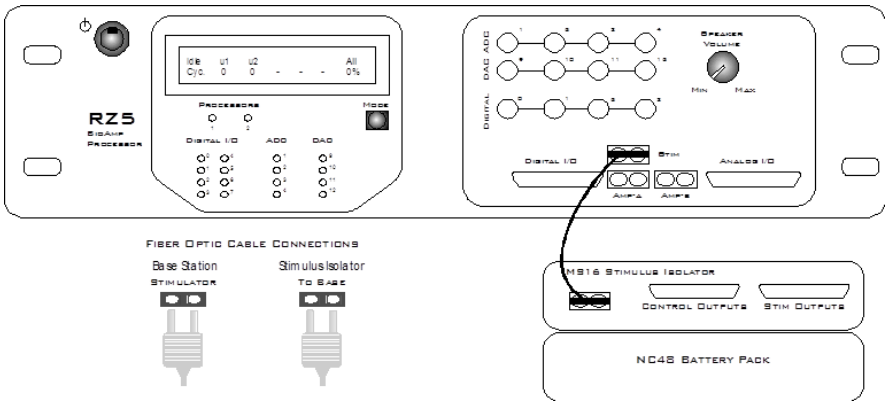
To connect the system hardware:

1. Ensure that the TDT drivers, PC interface, and device chassis are installed, setup, and configured according to the installation guide provided with your system.
2. Connect the battery pack to the back panel of the Stimulus Isolator via the connector labeled **Battery**, as shown in the diagram below.

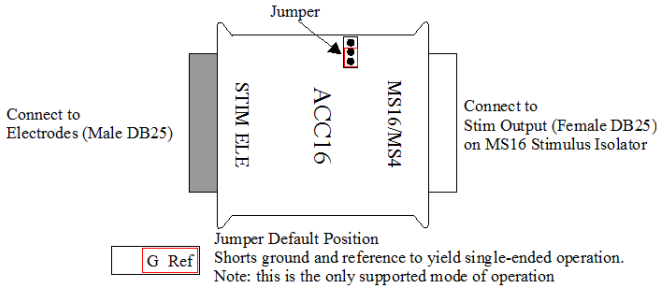


WARNING! The HV250 is a high voltage power source, capable of delivering up to 250 Volts DC at high currents. Shorting the battery connection pins can cause damage to the device and injury to the user. Always use caution when handling or connecting the devices.

3. Connect the Stimulus Isolator to the base station using the provided fiber optic cable.



4. Connect the fiber optic cable from the MS16 fiber optic port labeled **To Base** to the fiber optic port labeled **Stimulator** on either the RZ5 or the RX7 (not shown). Be sure to note the difference in the two sides of the fiber optic cable connectors and ensure they are inserted with the correct side up as shown under Fiber Optic Cable Connections above.
5. If desired, connect the ACC16 AC Coupler to the Stimulus Isolator's Stim Output port.



6. Connect the Stimulus Isolator's **Stim Output** or the ACC16's **Stim Ele** connector to the stimulating electrodes using your preferred method such as direct wiring, the SH16 switching headstage, or a custom pass through connector (available from TDT). See "MS4/MS16 Stimulus Isolator Technical Specifications" on page 8-47, for pinouts.
7. Power on the base station, then power on the stimulus isolator using the power switch on the isolator's back panel.

   Note: Ensure that the rechargeable batteries (onboard Li-Ion and NC48) are fully charged before starting your protocol.

   The hardware is ready for use.

If using the system with other devices, such as a switching headstage or preamplifiers, see the documentation for those devices for hardware connection information.

Stimulus Isolator Features

Analog Outputs (Stim Outputs)

The Stimulus Isolator is equipped with four or 16 analog current output channels, arranged in four-channel banks that can be powered down when not in use. Channels can operate in three modes: Stimulate, Reference, or Open. Simultaneously

setting any channel in a bank to both Stimulate and Reference mode turns off that entire bank of channels.

An ACC16 AC Coupler is supplied with all MS4/MS16 modules and may be connected directly to the Stim Output connector to block any DC current bias present on the Stim Output lines (this problem primarily affects researchers using electrodes with impedance of more than ~100 kOhms) when set in stimulate mode.

Note: When using the ACC16 you will NOT be able to deliver the MAXIMUM current.

Stim Lights

A Stim Light (one for each channel) indicates that a Stim Output channel is in use as a stimulus output. The Stim Lights are located above the Stim Output connector and are numbered 1 - 16, to indicate the active channel number. The LEDs will flash once every three seconds to indicate any bank of channels that has been powered off.

Ref Lights

A Ref Light (one for each channel) indicates that a Stim Output channel is in use as a reference. The Ref Lights are located above the Stim Output connector and are numbered 1 - 16, to indicate the active channel number.

Status Lights

Sync: Flashes once a second when the stimulator is not connected to a base station and glows steady when it is correctly connected.

Stim Ref: When lit, indicates that the stimulator has been configured to use a global reference.

Battery: When lit, indicates when the stimulator's onboard battery is low. The battery voltage decreases rapidly once the battery low light is on.

Fast: charging
Slow: low battery

High Voltage: When lit, indicates that the stimulator is correctly connected to the designated Battery Pack.

Solid: correct working voltage
Flashing: low voltage

Digital Output (Control Outputs)

The Control Output connector provides access to the stimulator's 16 channels of Word addressable digital output. These outputs can control the relays on the SH16 switching headstage or other digital output device (maximum current 40 mA, maximum voltage 3.3 Volts).

Control Output Lights

A Control Output Light (one for each digital I/O) indicates that the digital output channel is set high (or active). The Control Output Lights are located above the Control Output connector and are numbered 1 - 16, to indicate the active digital output channel.

Fiber Optic Port (To Base)

The stimulus isolator's fiber optic input port (labeled To Base) provides an isolated connection to the base station (RZ5 or RX7). The fiber optic cable carries digital signals to D/A's on the stimulus isolator. It also carries control information and information about the state of the stimulation channels. One end of the fiber optic cable connects to the device using the To Base connection pair and the other end connects to the Stimulator input on the base station.

Keep in mind, because of the fiber optic cable data transfer rate, the corresponding Stimulator fiber optic output port on the base station (RZ5 or RX7) will be disabled if the system sampling rate is set to a value greater than 24.414 kHz.

High Voltage Input (Back Panel)

The stimulator uses either the NC48 or the HV250 High voltage Battery Pack for stimulation. The battery pack should be connected via the Battery connection on the back panel.

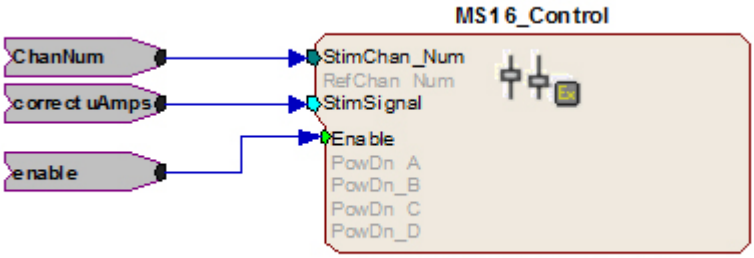
WARNING! The HV250 battery packs are capable of delivering up to 250 Volts DC at high currents. Shorting the device can cause damage to the device and injury to the user. Always use caution when handling or connecting the devices.

Power Switch (Back Panel)

The Power switch turns the stimulus isolator power off or on. The fiber connector on the front panel will be illuminated when the stimulator is on.

Software Control

Operation of the MicroStimulator system is controlled via an RPvdsEx circuit loaded and run on the connected base station processor (RZ5 or RX7). TDT recommends using the MS16_Control Macro (pictured below) in your control circuits. This macro simplifies setup of stimulus and reference channels, stimulus signal output, and power conservation. The macro is also used to configure the correct scale factors and poke addresses for the RZ5 or RX7 processor. Select the correct device in the macro settings dialog.



Single Ended Stim Mode (RZ5)

When the MS16_Control macro is not sufficient for your task, a circuit can be designed using the Poke component to control the system. This component writes to special memory locations on System 3 devices and is intended primarily for TDT use. While both methods are described here, keep in mind that the Poke component should be used with caution.

Important Circuit Design Considerations

Sampling Rate

When using the RZ5 or RX7 with the stimulus isolator, the maximum sampling rate of the system is 24.414 kHz, a limitation of the fiber optic connection between the base station and the stimulus isolator.

Signal Resolution

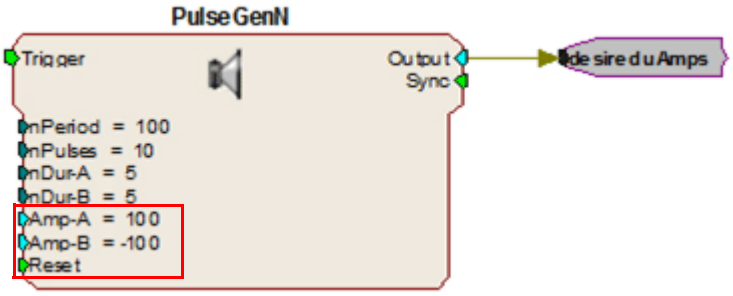
Signal resolution is dependent on the sampling rate used. The stimulus isolator's PCM D/A converters allow users to generate precise pulsed signals, including square waves with durations of only 1 sample. When using the maximum sampling rate of 24.414 kHz, the sample period is 40.96 microseconds. The stimulus isolator has an effective bandwidth of 10 kHz for continuous (non-pulsed) waveforms.

Designing the Stimulus Signal

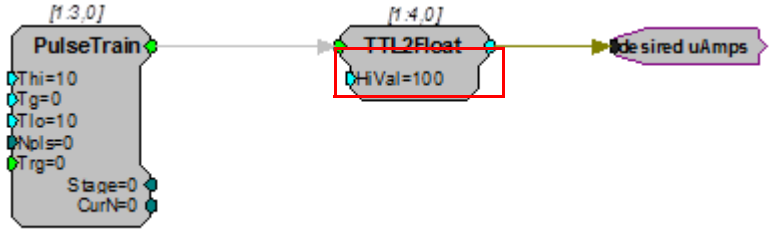
The MicroStimulator system offers flexible stimulus delivery capable of generating complex patterns of pulses or arbitrary waveforms. This allows you to make use of the full range of the waveform and pulse generators in the RPvdsEx component library, including the PulseGenN macro.

Desired Signal Range

When adding and configuring waveform components you must consider the output range of the system. The default configuration of the stimulus isolator can deliver stimuli in the range of +/- 100 µA; be sure to set component amplitude parameters with this output range in mind. In the figure below, the amplitude of a biphasic pulse is defined in the Amp-A and Amp-B parameters.



When using components that output a logical signal, such as a PulseTrain, the output range can be defined when the output is converted to the desired data type. In the figure below the PulseTrain component sends out a standard TTL signal with a fixed duration. A TTL2Float component is then used to convert the signal to a user specified value between 0 and 100. This value indicates the desired stimulator output in microAmps.



If the ACC16 is not in use the desired uAmps in floating point format can be fed directly to the MS16_Control macro's Stim Signal input. If the ACC16 is being used a correction factor must be applied (see below).

ACC16 Correction Factor

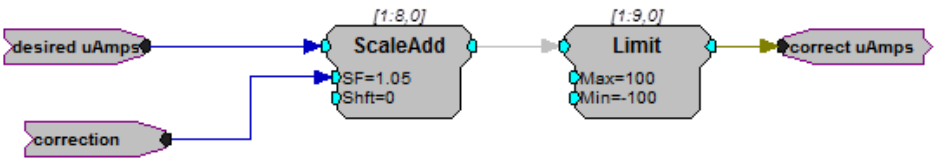
An ACC16 AC coupler can be used with the system in single-ended operation (global reference) to block any DC bias present on the Stim Output lines (a problem primarily affecting researchers using electrodes with impedance of more than 200 kOhms). When the ACC16 is in use, it acts as a voltage divider, decreasing the voltage and thus the current delivered through the electrode. The actual current delivered through the ACC16 depends on the ratio of the coupler impedance to the impedance of the electrode in use. For 50 kOhm electrodes the error is about 5%.

To calculate a correction factor for actual current delivered:

1. Determine the impedance of your stimulating electrode.
2. Calculate the following equation:

   Correction = 1/(1,000,000/(Electrode Imp+1,000,000))

   = (Electrode Imp +1,000,000)/1,000,000
3. In your circuit, scale the current output by this value.



In the example correction circuit above:

- The value for "correction" represents the results of the calculation above.
- The value for "desired uAmps" represents the desired amplitude of the stimulus signal.
- The values for the "Limit" component should be set based on the actual limits of your systems. The MS4/MS16 is available in 100 µA and 1 mA versions. **In either case, when using the ACC16 you will NOT be able to deliver the MAXIMUM current. The maximum current = 1/correction factor x 100. Calling for higher currents will deliver currents at the defined limit.**

If using the recommended MS16_Control Macro, the *correct uAmps* value is fed to the macro's **Stim Signal** input.

Selecting Global or Local Reference Mode

The **MS16_Control** macro should be included in all circuits for stimulus isolator control. The **Stimulation Mode** setting on the Setup tab of the macro properties dialog box determines whether the stimulus isolator is configured to use a global reference *(Single ended)* or a local reference(s) *(Differential)*.

Global Reference Mode

If a global reference is desired, set the MS16_Control macro's **Stimulation Mode** to *Single Ended* on the **Setup** tab of the macro properties dialog box. In this mode the **RefChan** input is disabled.

Local Reference Mode

If local reference is desired, set the **MS16_Control** macro's **Stimulation Mode** to *Differential* on the **Setup** tab of the macro properties dialog box. In this mode the **RefChan** input is enabled.

Note: In Local Reference (*Differential*) mode, writing a 0 to the **RefChan_Mask** macro input while the **Channel Select Method** is set to **With Chan Mask**, will disable all local reference channels and enable the global reference.

Configuring Reference and Stimulation Channels

The **MS16_Control** macro sets reference and stimulation channels. Feeding an integer value to the macro's **StimChan** and **RefChan** inputs will *turn on* channels for stimulation or reference, respectively. The **Channel Select Method** on the **Setup** tab of the macro properties dialog box determines whether the integer is read as a single channel number or as a mask value representing multiple channels.

Important! Configuring a channel, as both stimulus and reference will cause the unit to automatically turn off that bank of channels.

Setting a Single Channel for Stimulation or Local Reference

By default, the **Channel Select Method** on the **Setup** tab of the macro properties dialog box is set to **With Chan Number**. The **StimChan** and **RefChan** inputs accept an integer value of 0 through 16 and the macro will set the selected channel for stimulation or local reference.

Note: An integer value of 0 fed to StimChan disables all channels.

Setting Multiple Channels for Stimulation or Local Reference

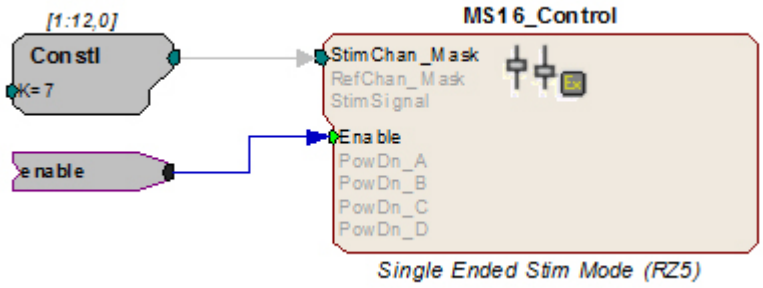
To configure multiple reference channels, the **Channel Select Method** on the **Setup** tab of the macros properties box must be set to **With Chan Mask**. In this mode, **StimChan** and **RefChan** inputs accept an integer value channel mask representative of the desired channels (shown in the table below). The integer value is the sum of the channel masks for the channels.

Channel Mask Table

Channel #	Channel Mask		Channel #	Channel Mask
1	1		9	256
2	2		10	512
3	4		11	1024
4	8		12	2048
5	16		13	4096
6	32		14	8192
7	64		15	16384
8	128		16	32768

For example:

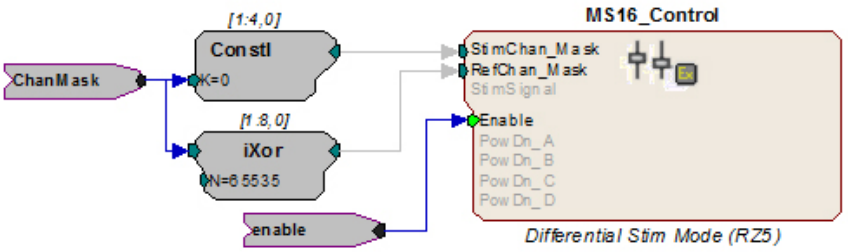
If you wish to simultaneously set channels 1 (channel mask 1), 2 (channel mask 2), and 3 (channel mask 4) to stimulation mode add their respective channel masks from the table above (1 + 2 + 4 = 7), and send that sum (7) to the StimChan_Mask input as shown in the figure below.



Single Ended Stim Mode (RZ5)

This example sets channels 1, 2, and 3 for stimulation. Unused banks of channels are powered down. The stimulus design and delivery are not included in this circuit segment.

The reference channels can be configured in the same way, using the integer values in the Channel Mask Table above. The iXor component can also be used to set all channels NOT set as stimulation to reference. In the figure below, an iXor is used to perform an **exclusive** bitwise OR function. The channel mask for stimulation is XORed with the integer mask value for all channels, resulting in a channel mask that sets all non-stimulus channels to reference channels.



Important! Writing a **0** to the **RefChan_Mask** macro input while the **Channel Select Method** is set to W**ith Chan Mask**, will disable all local reference channels and enable the global reference.

Delivering the Stimulation

The stimulus delivery segment of the circuit can be handled within the MS16_Control macro or external to the macro using the Poke component. TDT recommends using the MS16_Control macro whenever possible.

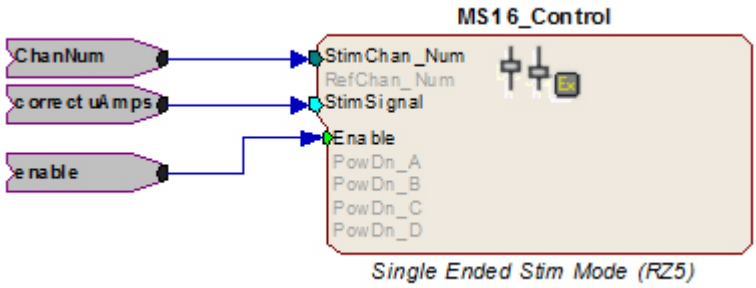
The Poke component should be used with caution; however, it is necessary for some tasks, including simultaneous stimulation on multiple channels.

Important! The memory addresses used with the Poke component are different for the RZ5 and RX7. See "Memory Address Reference for Using the Poke Component" on page 8-43, for more information.

Single Channel Stimulation with Global Reference

When the global reference is used, the **MS16_Control** macro can be used for single channel stimulation. The **Stimulation Mode** on the **Setup** tab of the macro's properties box must be set to *Single Ended* and the **Channel Select Method** must be set to **With Chan Number** to enable the StimSignal input.

StimSignal accepts floating-point input, representative of the desired stimulus current waveform. The macro will send the stimulus signal to the channel set using the **StimChan_Num** input.



This example sends floating point values representing the amplitude of the waveform in microAmps to a user-specified channel of the stimulator as long as the enable is high. If using the ACC16 be sure to scale the signal by the necessary correction factor. See "The ACC16 AC Coupler" on page 8-32, for more information.

Note: To conserve the life of the stimulus isolator's onboard and external batteries, remember to power down unused bank of channels on the **MS16_Control** macro's **Power Control** tab.

Simultaneous Stimulation on Multiple Channels and/or Local Reference Mode

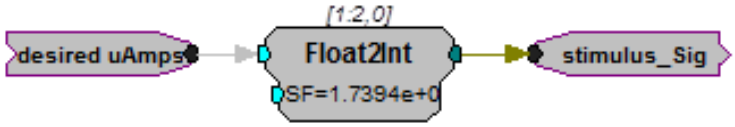
The MS16_Control macro's StimSignal is disabled whenever the local reference mode is used or when a channel mask is used to set multiple stimulation channels. In these cases the macro should still be used to configure or turn on channels for stimulation (see "Configuring Reference and Stimulation Channels" on page 8-39), but stimulus delivery must be handled external to the macro.

Converting the Signal to an Integer Value

When designing the stimulus signal it is convenient to work with floating point values that represents the desired current in microAmps (See "Designing the Stimulus Signal" on page 8-37), However, when the macro is not used the stimulus signal must be converted to an integer value representing a voltage level in the proper range for the stimulus isolator. The scale factor required to scale the current in the desired range of +/-100 µA is dependent on the type of base station processor being used.

RZ5 When using the RZ5, use a scale factor of: **1.7394e+007**

RX7 When using the RX7, use a scale factor of: **265.41**



In this circuit segment, the desired floating point value in microAmps is fed to a Float2Int, which converts the data type and applies the scale factor.

Signal Output to Stimulus Channels

Once output waveforms are converted to an integer value they are poked (written) to memory locations on the MS4/MS16, using the Poke component. Memory addresses vary be processor as described here. Reference tables are also provided below "Memory Address Reference for Using the Poke Component" on page 8-43.

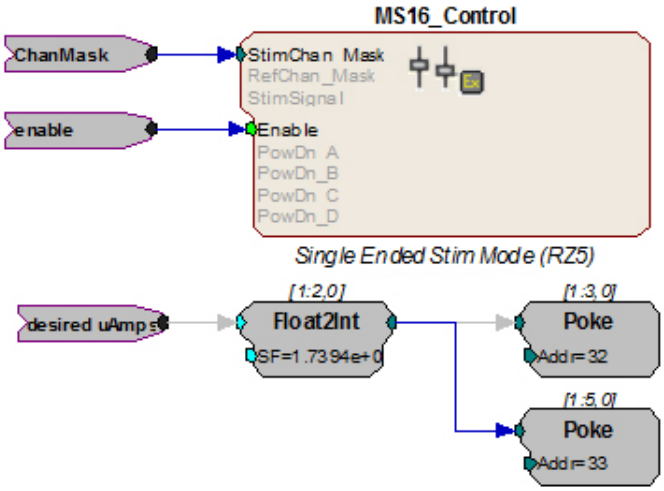
RZ5 When using the RZ5, output to channels 1-16 must be written to memory addresses 32-47, respectively. To do so, offset the channel number by 31 and enter this value in the address parameter of the Poke component.

The circuit segment above sends out a stimulus signal to channel one of the stimulator.

RX7 When using the RX7, output to channels 1-16 must be written to memory addresses 20-35, respectively. To do so, offset the channel number by 19 and enter this value in the address parameter of the Poke component.

Summary: Simultaneous Stimulation on Multiple Channels

The example below shows a more complete picture, with the MS16_Control macro used to set or *turn on* multiple channels using the ChanMask hop, "Setting Multiple Channels for Stimulation or Local Reference" on page 8-40, and the Poke used to write the signal value to the MS4/MS16 memory location for channels one and two with the RZ5.



Circuit Design Using the Poke Component

Using the MS16_Control macro simplifies circuit design for the MicroStimulator System. If the macro **cannot** be used, you can use the RPvdsEx Poke component to control the stimulus isolator by writing information to memory addresses on the RZ5 or RX7.

Memory Address Reference for Using the Poke Component

The table below summarizes each stimulus isolator control function and its memory address.

Control	Value Description	Memory Address	
		RZ5	RX7
Stimulus Channels	Mask for channels between none and 16; integer value between 0 and 65535	48	7
Signal Output	Integer representing current level scaled for D/A (varies depending on device).	32-47	20-35
Global Reference	0 (off) or 1 (on)	50	9
Reference Channels	Mask for channels between none and 16; integer value between 0 and 65535	49	8
Digital Out	Mask for channels between none and 16; integer value between 0 and 65535	51	3

Signal Output to Stimulus Channels

To generate signals on the stimulus isolator, the output waveforms are poked (written) to memory locations as integer values. See "Converting the Signal to an

Integer Value" on page 8-42. for more information.

The table below maps the output channels of the RZ5 and RX7 to their poke address.

Isolator Output Channel	Poke Waveform To Address		Isolator Output Channel	Poke Waveform To Address	
	RZ5	RX7		RZ	RX7
1	32	20	9	40	28
2	33	21	10	41	29
3	34	22	11	42	30
4	35	23	12	43	31
5	36	24	13	44	32
6	37	25	14	45	33
7	38	26	15	46	34
8	39	27	16	47	35

Global Reference Enable

Global reference uses the analog ground to complete the stimulation circuit. The global reference feature can be enabled by setting the value of a specific memory address to one. The StimRef indicator light on the front panel of the stimulus isolator is illuminated when the global reference has been set.

RZ5 To enable global reference when using an RZ5 **set the value of memory address 50 to one** as pictured above.

RX7 To enable global reference when using the RX7 **set the value of address 9 to one.**

Channel Masks

Memory addresses for stimulus, reference, or digital I/O channel setup expect an integer value between zero and 65535. Masked values for each channel are noted in the table below. Adding masked values together will set multiple channels.

The table below maps channel numbers to mask values:

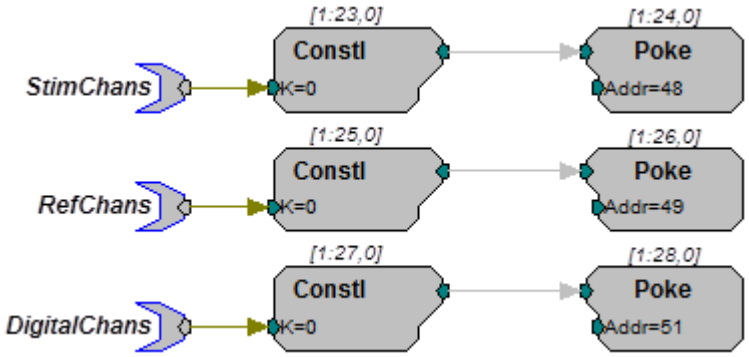
Channel #	Channel Mask	Channel #	Channel Mask
1	1	9	256
2	2	10	512
3	4	11	1024
4	8	12	2048
5	16	13	4096
6	32	14	8192
7	64	15	16384
8	128	16	32768

For example:

If channels 1 (channel mask 1), 2 (channel mask 2), and 3 (channel mask 4) are desired, use a channel mask of 7 (1 + 2 + 4 = 7).

Stimulus, Reference, or Control Channel Setup

To enable a given channel, an integer value is written to the appropriate memory address of the base station. The integer value is the sum of the channel masks (see table above for mask values) for all the stimulation channels that the user wishes to activate.



In the example circuit above, the StimChans parameter tag feeds a ConstI an integer value used to assign channels as stimulus channels, RefChans sets the reference channels, and DigitalChans sets the digital channels. This example above is configured for the RZ5.

Important! The memory addresses for the RZ5 and RX7 are different. See "Memory Address Reference for Using the Poke Component" on page 8-43, for more information.

Note: When using the SH16 switching headstage, the digital I/O channels on the MS4/MS16 are used to control the switching headstage. These are accessed via a DB25 connector labeled **Control**. For SH16 switching headstages (serial number 2000 and greater), channels 1-3 are used for communication and channels 4-8 are used to provide power to the SH16. When the SH16 is not being used, the MS4/MS16 digital I/O can be used for any type of digital control.

See "SH16 Switchable Headstages" on page 11-49, for more information about controlling the headstage.

Working with the MS16 MilliAmp Mode

The MS16 can be modified at the factory to deliver stimuli in the +/- 1 mA range. If your device has this modification, please note the following important differences in operation.

The HV250 battery pack **CANNOT** be used with milliAmp mode. This mode should only be used with the NC48 battery pack.

Circuit Design for the MS16 in MilliAmp Mode

MS16_Control Macro

When using the **MS16_Control** macro set **High Current Range** on the **Setup** tab of the macro's properties box to Yes. If High Current Range is set to Yes, all other circuit design considerations are handled automatically by the macro.

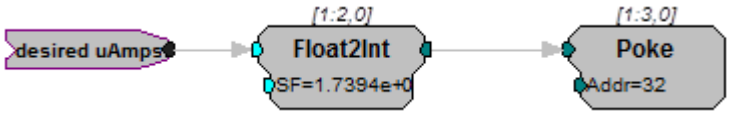
Scale Factor

When using the Poke component for stimulus delivery, use the appropriate scale factor for your processor to convert the signal in desired or corrected microAmps to the necessary voltage for A/Ds.

RZ5 When using RZ5, use a scale factor of **1.7394e+006.**

RX7 When using RX7, use a scale factor of **26.541.**

See "Converting the Signal to an Integer Value" on page 8-42, for more information.



In this circuit segment, the desired floating point value in microAmps is fed to a Float2Int, which converts the data type and applies the necessary scale factor for MilliAmp mode.

High Current Mode

When the MS16_Control is not used at all, the high current mode can be set by sending a specific value to the appropriate memory address for your processor. This memory address is the same address used to turn on or off the global reference. The value used to set the high current mode can be added to the global reference values 0 (off) and 1(on).

RZ5 When using the RZ5, the high current mode can be set by sending **a value of 54784 to memory address 50.**

Therefore, poking 54784 to the address turns on high current mode and turns off the global reference; while poking 54785 to the address turns on high current mode and turns on the global reference.

RX7

When using the RX7, the high current mode can be set by sending **a value of 214 to memory address 9.**

Therefore, poking 214 to address 9 turns on high current mode and turns off the global reference; while poking 215 to address 9 turns on high current mode and turns on the global reference.

MS4/MS16 Stimulus Isolator Technical Specifications

Stimulus Output Channels	4 (MS4) or 16 (MS16)
Sampling rate	Up to 24.414 kHz
Stimulus Output Current	+/- 100 µA up to 1 MOhm load with HV250 +/- 100 µA up to 200 kOhms load with NC48*
Offset Current	Less than 0.2% of full range setting
Digital Output Max Current	40 mA
Digital Output Max Voltage	3.3 V
Selectable Reference	Local or Global
Power	
Control	Onboard Rechargeable Li-Ion battery
Stimulation	NC48 Rechargeable Battery with NiCad batteries* or HV250 Battery Pack with Carbon Zinc batteries

***Note:** the Stimulus Isolator may be modified at the factory for 1 MilliAmp Mode.

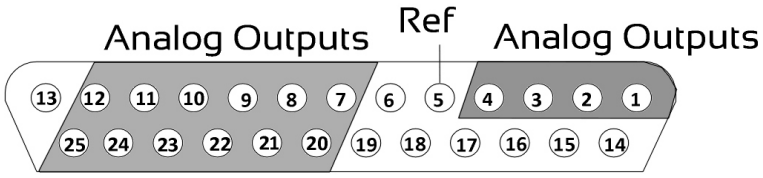
DB25 Connector Pinouts

STIM ELE Connector on the ACC16

The ACC16 AC Coupler is used to block DC bias and connects directly to this Stim Output Connector, passing signals through to its STIM ELE connector with the same pinout.

Stim Output Connector

The Stim Output connector provides access to the analog output channels. These channels are used primarily for stimulus output.

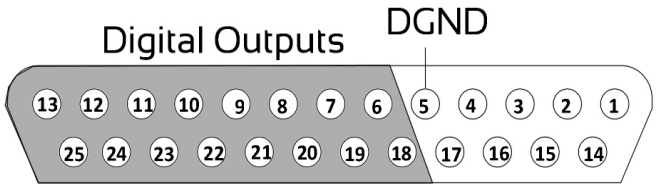


Pin	Name	Description		Pin	Name	Description
1	A1	Analog Channels Ch 1-4		14	NA	Not Used
2	A2			15		
3	A3			16		
4	A4			17		
5	Ref	Reference		18		
6	NA	Not Used		19		
7	A5	Analog Channels Ch 5, 7, 9, 11, 13, and 15		20	A6	Analog Channels Ch 6, 8, 10, 12, and 14, 16
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	NA	Not Used				

Note: Channels 5 - 16 not available on the MS4.

Control Output Connector

This connector provides access to control or relay output channels.



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		14	NA	Not Used
2				15		
3				16		
4				17		
5	DGND	Digital Ground		18	D0	Digital Outputs Bits 0, 2, 4, 6, 8, 10, 12, and 14
6	D1	Digital Output Bits 1, 3, 5, 7, 9, 11, 13, and 15		19	D2	
7	D3			20	D4	
8	D5			21	D6	
9	D7			22	D8	
10	D9			23	D10	
11	D11			24	D12	
12	D13			25	D14	
13	D15					

Battery Reference

The stimulus isolator uses an onboard Lithium-Ion battery for general device operation. These batteries charge in four hours. A 6-9 Volt battery charger with 500 mA of current capacity is included with the stimulator and can be connected via the Charger connector on the stimulator's back panel. The charger tip is center negative. If it is necessary to replace the charger, ensure that the power supply has the correct polarity.

Issue	HV250	NC48	Onboard Li-Ion
Battery life	130 mAh (up to 27 hours stimulation)	1000 mAh (up to 240 hours of stimulation)	12-15 hours battery life between charges
Rechargeable	No	Yes	Yes
Maximum impedance for delivering a 100 microAmp current	1 MOhms	200 kOhms	N/A
Usable in MilliAmp Mode	No	Yes	Yes
Ambient temperature	Normal room temperatures	Normal room temperatures	Normal room temperatures

HV250 Battery Pack

The HV250 Battery Pack uses four Carbon Zinc batteries, each delivering 67 Volts. Because the HV250 Battery Pack is non-rechargeable, it must be replaced periodically. The High Voltage LED on the front panel of the MS4/MS16 will flash to

alert the user of a low voltage condition. To extend the life of the battery, we recommend enabling only the desired channels for stimulation.

WARNING! The HV250 is a high-voltage power source, capable of delivering up to 250 Volts DC at high amperages. Shorting the device can cause damage to the device and injury to the user. Always use caution when handling or connecting the devices. Never attempt to charge the HV250.

NC48 Battery Pack

The NC48 Battery Pack uses 32 Nickel Cadmium (NiCad) batteries to supply a peak-to-peak voltage of 48 Volts with a range of +/- 24 Volts.

WARNING! Just as with all batteries, shorting the NC48 Battery Pack can cause damage to the device and injury to the user. Always use caution when handling or connecting the devices.

WARNING! Overcharging the NC48 battery pack can cause the cells to rupture.

The NC48 Battery Pack should be connected to its charger for a maximum of 16 hours. Overcharging shortens battery life and may burn out the battery in extreme cases. Although the batteries used in the NC48 are designed to provide the user with dozens of charge/discharge cycles, the performance of all rechargeable batteries deteriorates over time. The major sign that a battery is deteriorating is a shortened use cycle between charges.

Important! Used NiCad batteries must be recycled.

The NC48 Battery pack should be stored at normal room temperatures. Temperature extremes can affect the operation of the batteries. Battery packs stored for longer than two months should be tested prior to use.

MS4/MS16 Anomalies

If the stimulus isolator control bits and relay switching control bits do not work after power up, execute a hardware reset on the base station using zBusMon.

Serial numbers 4000 and above

Previous versions of the stimulator automatically switched banks of channels off when not in use. A recent change to the microcode eliminates this feature, giving users control over when channels are turned off. By default, all channels are on and must be turned off manually.

Serial numbers below 4008 (MS4) and 4015 (MS16)

When the NC48 is connected to the stimulus isolator, the High Voltage LED on the front panel of the MS4/MS16 will constantly flash even when the NC48 (+/-24 V) is at full charge, because the voltage monitoring circuitry was designed to detect a low voltage of the HV250 battery pack.

Serial numbers below 4000

The MS4/MS16 has undergone several design changes to improve performance and usability. TDT recommends that all users upgrade to the latest versions (serial numbers 4000 and above). Contact TDT for an RMA to upgrade your current module.

Serial numbers below 3000

Noise on outputs is high when the output is in "Open" mode. The noise is especially evident during recording and stimulation events. Contact TDT for an RMA for upgrade of your current device.

Conservation of Power

The stimulus isolator's analog channels are arranged in four-channel banks. Each of these banks is powered up on reset of the device and will remain powered on. To conserve power, TDT recommends powering down unused banks of channels. The MS16_Control macro can be used to turn off unused banks of channels. When not using the macro, simultaneously setting any channel in a bank to both Stimulate and Reference mode turns off that four-channel bank.

Maximum Voltage Output

The stimulus output channels drive a current signal that ranges from 0-100 microAmps. The maximum voltage output from the MicroStimulator system using the TDT NC48 battery is the 24 volts and the maximum voltage output using the TDT HV250 battery is 125 Volts. The actual voltage output depends on the current waveform specified and the impedance of your electrodes, that is, V = ZI where V=Volts, Z = impedance and I = current.

Using the MicroStimulator with TDT's Switching Headstage

When using TDT's switching headstage, ensure that relays for channels used for stimulation have been switched to the correct position using the SH16_Control macro. Any stimulus channel for which the corresponding control channel has not also been set will fail to generate a signal. See "SH16 Switchable Headstages" on page 11-49.

Part 9: Video Processor

RV2 Video Processor

RV2 Overview

As part of a system is comprised of a machine vision color camera (VGAC), and a dedicated video processor and collection device (RV2). Video is streamed from the camera to the RV2 collection device where it is processed and stored. Camera triggering is precisely synchronized to the collection system (RZ) allowing frame by frame correlation between video data and other recorded system signals.

A number of methods support robust target tracking including red/green LEDs mounted on the ZIF-Clip® headstage or limb tracking. Positional information is available in real-time on the RZ device and can be processed and/or stored. Image data is stored on dedicated hard drives within the RV2 in DIVX encoded AVI files.

Access to the RV2 storage array can be provided through a LAN connection or direct connection to a PC.

The RV2 is recommended for use with TDT systems only.

Power and Communication

A fiber optic port on the back panel of the RV2 is used to communicate with an RZ device. The RV2 receives timing pulses from a special DSP (RZDSP-V) and returns real-time frame and tracking information for further processing and storage.

Communication to the RV2 is provided through a touch screen user interface independent from the TDT system. Firmware updates for the RV2 interface are available online through the TDT web server. See “Config” on page 9-15, for more information.

Snapshots are sent from the RV2 over the network to the PC for laying out regions using RVMap software. Configuration files are sent from RVMap software to the RV2, also over the network.

The RV2 contains an integrated switched-mode power supply. The power supply auto-detects your region's voltage setting and no further configuration is needed. A switch located on the back panel of the RV2 is used to enable/disable the power supply.

Software Control

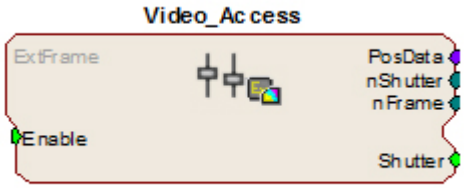
Software control is implemented with circuit files developed using TDT's RP Visual Design Studio (RPvdsEx) on the RZ processor through TDT's OpenEx software package. A single RPvdsEx macro is provided to configure the RZ to send trigger information to the RV2 and receive frame and positional information.

See the "RZ Z-Series Processors", for more information on your RZ processor. For circuit design techniques and a complete reference of the RPvdsEx circuit components, see "MultiProcessor Circuit Design" and "Multi-Channel Circuit Design" in the *RPvdsEx Manual*.

RVMap software is used to define regions and tracks for the RV2 search algorithm and determine what data is returned to the RZ for real-time analysis and/or storage. See "RVMap Software for RV2" on page 9-21, for more information.

Triggering the RV2

The Video_Access macro is provided for configuring video tracking and must be added to the circuit file used in OpenEx. The macro has settings for the frame control, rate, and storage. See the macro internal help for more information.



This macro also requires that the CoreSweepControl macro is present in the circuit to handle all circuit timing. The Video_Access macro stores timestamps when frame information is received. The PosData multi-channel stream contains tracker positions. Information for up to eight targets can be returned to the RZ for storage. RVMap is used to define the targets that are returned to the RZ. The Video_Access macro **must** be assigned to the DSP that is physically connected to the RV2.

The Video_Access macro controls when frame triggers are sent from the RZ to the RV2. The RV2 receives the trigger, retrieves an image from the camera, adds it into the video file, performs the tracking algorithm and prepares the tracking data to be sent to the RZ.

The RV2 waits until the next camera trigger from the RZ before returning the tracking data from the previous frame to the RZ. This ensures that there is always enough time to collect an image from the camera and run the tracking algorithm on it, and greatly reduces the likelihood that a frame is missed due to jitter in the collection process. However, because of this protection the data received by the RZ is always off by one frame.

When track data is sent to the RZ it is also written to the tracking.txt file. The timestamp in the tracking.txt file indicates when the data was collected from the camera and is relative to when the RV2 began recording.

Recording Sessions

When OpenWorkbench is set to 'Record' mode and a Video_Access macro is present in the circuit, Workbench sends a UDP packet over the network to find RV2s. If Workbench doesn't receive a response within five seconds an error message is displayed and recording begins without video storage. The UDP packet contains the tank and block name so the RV2 can properly name its files. Once an RV2 responds, OpenEx begins sending frame triggers and recording data. When OpenEx switches modes to anything other than 'Record' a packet is sent to the RV2 to close the files it is currently writing to and wait for the next recording session.

Frame Rate

The maximum frame rate depends on the camera's exposure setting. This value can be adjusted using the 'Lighter' and 'Darker' buttons on the RV2 touch screen interface. The frame rate is overlaid on the camera image in the Live tab. The current maximum rate based on the camera settings is displayed when the camera is in free run mode.

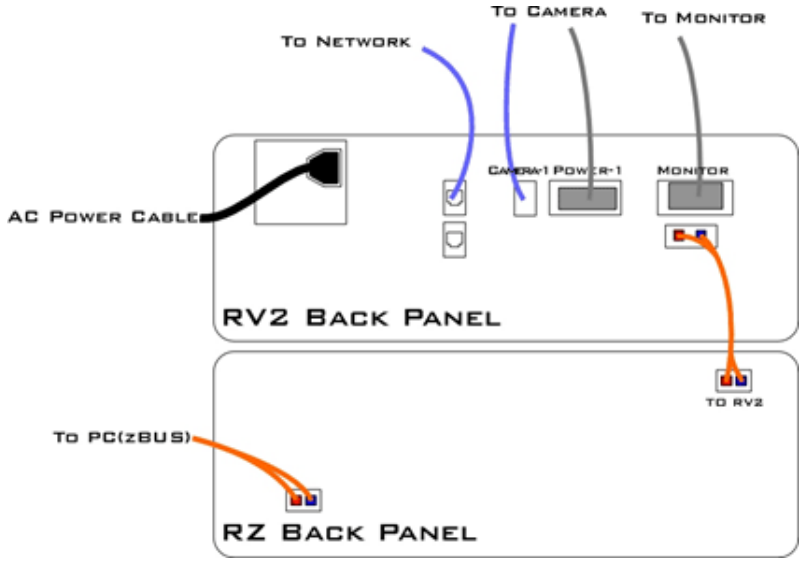
Note: When recording data it is important that the desired frame rate is no greater than the observed free run frame rate, otherwise frame loss will occur. A lost frame counter is overlaid on the lower right corner the camera image. To reset this counter, see the Status tab. A reboot will also reset the lost frame counter.

Hardware Requirements

Basic requirements include a VGAC, an RV2, an RZ equipped with at least one video fiber optic port, one fiber optic cable for connection between the RV2 and RZ, the VGAC power cable, one Gigabit Ethernet cable to connect the VGAC to the RV2, a PC equipped with an Ethernet port or an Ethernet jack connected to a local area network, and an Ethernet cable.

Setting-Up Your Hardware

Important! Make sure that all cables are connected before powering on the RV2.



RV2 to RZ Connection Diagram

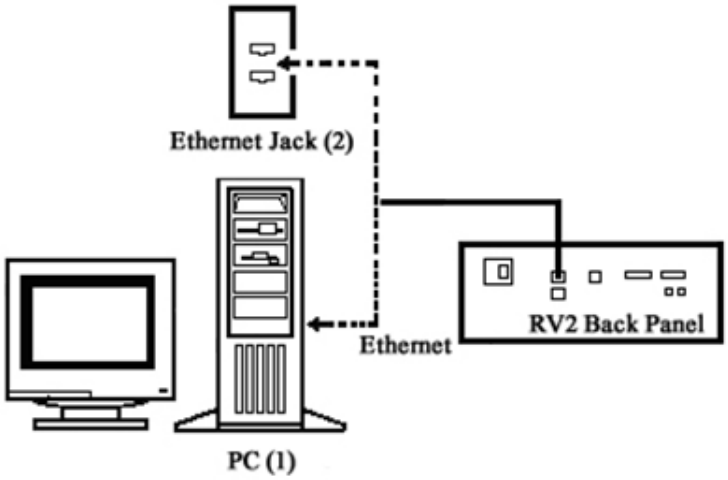
In the diagram above, a single RZ connects to the RV2. The fiber optic cables are color coded to prevent wiring errors.

The RV2 Video Processor connects to one RZ processor via orange fiber optic cables from the back of the RV2 to the dedicated RV2 port on the back of the RZ (labeled 'To RV2').

The gray camera power cable connects the 'Power-1' port on the RV2 to the VGAC camera. A GigE cable connects the 'Camera-1' port on the RV2 to the VGAC.

An Ethernet cable connects the 'Network' port on the RV2 to either a local area network or directly to the PC running OpenEx.

Optionally a VGA cable is connected from the 'Monitor' port on the RV2 to an external monitor.



RV2 PC and Network Connection Diagram

The diagram above illustrates possible connections from the RV2 to a PC (1) or network (2). Connect the Ethernet cable to the RV2 port labeled Network.

Configuring the RV2

Default configuration settings allow the RV2 to begin streaming video immediately. The RV2 supports the DHCP (Dynamic Host Configuration) protocol for automatic configuration of network parameters. Once connected to an active network, the RV2 will attempt to lease an IP address.

The DHCP Protocol

DHCP or "Dynamic Host Configuration Protocol" is a protocol used by networked devices (clients) to obtain various parameters necessary for the clients to operate in an IP (Internet Protocol) network. By using this protocol, system administration workload greatly decreases, and devices can be added to the network with minimal or no manual configuration.

DHCP automates the assignment of IP addresses, subnet masks, default gateway, and other IP parameters. Three modes for allocating IP addresses exist: Dynamic, Reserved, and Manual. The RV2 relies on Dynamic mode for its IP configuration. If no DHCP server responds, enable manual configuration mode with the following static IP configuration:

IP Address: 10.1.0.42

Netmask: 255.255.255.0

You can configure the IP address manually through the touchscreen interface. See "To enable manual configuration:" below or "Status" on page 9-14.

Dynamic mode

In dynamic mode a client is provided with a temporary IP address for a given length of time. The duration is dependent on the server configuration and may range from several hours to months.

The RV2 will automatically renew the current IP address as needed. This renewal is used by properly functioning clients to maintain the same IP address throughout their connection to a network.

Accessing the RV2

There are two methods provided for accessing the RV2:

- Directly connecting to a PC
- Connection to a local area network

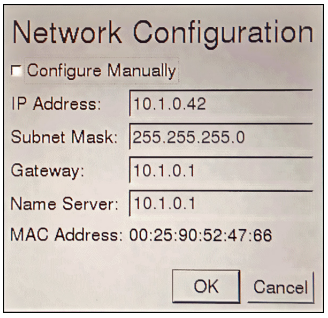
Direct Connection to a PC

Direct connection to a PC allows data on the RV2 to be viewed and modified through the standard Microsoft Windows file sharing protocol.

Important: When using a Static IP, the RV2 Current IP must be set to "Configure Manually" using the touch screen interface.

To enable manual configuration:

1. Touch the **Status Tab and then** touch the **Current IP field,** to display the Network Configuration window.



2. Touch the **Configure Manually** check box and click OK to accept the default value.

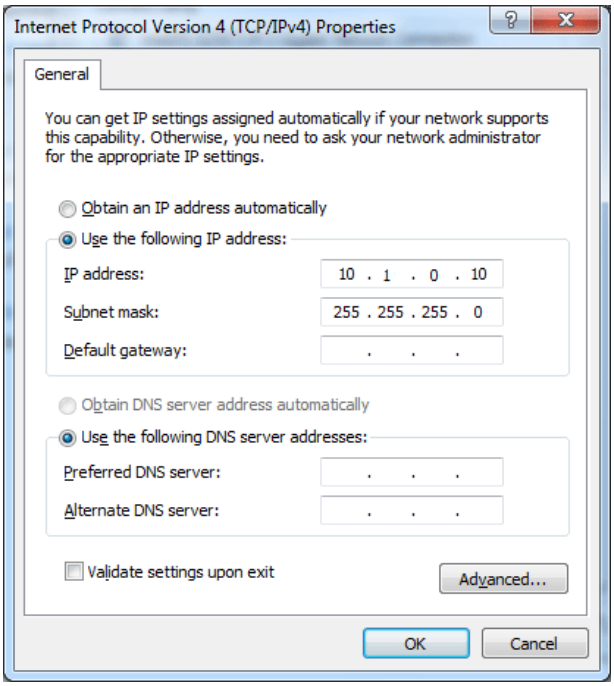
Using Windows 7

To access the RV2 file system through a PC, running Windows 7:

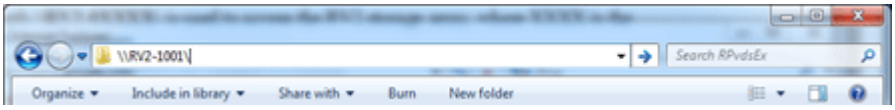
3. You will have to configure the PC TCP/IP settings. Open **Control Panel** then double-click **Network and Sharing Center**.
4. Click the desired connection link (this is usually a Local Area Connection).
5. In the status dialog, click the **Properties** button.

6. In the item list, select **Internet Protocol (TCP/IP)** or if there are multiples, select **Internet Protocol (TCP/IPv4)**.
7. Click the **Properties** button.
8. Select **Use the following IP address** and enter these values:

   IP address: 10.1.0.x, where x can be any value from 1 to 254 except 42.
   Subnet mask: 255.255.255.0
   Default gateway: Leave empty



9. Click **OK**. The RV2 can now be accessed by the PC.
10. Obtain the RV2 device address.
    a. Press the **Live** tab on the RV2 interface.
    b. The device address is displayed at the top of the page to the right of **Device Name** field.
11. Enter the device address as shown in a windows address bar to access the RV2 file system.



Typically, the path \\RV2-XXXX\ is used to access the RV2 storage array, where XXXX is the device serial number, but the name should be verified on the Live tab.

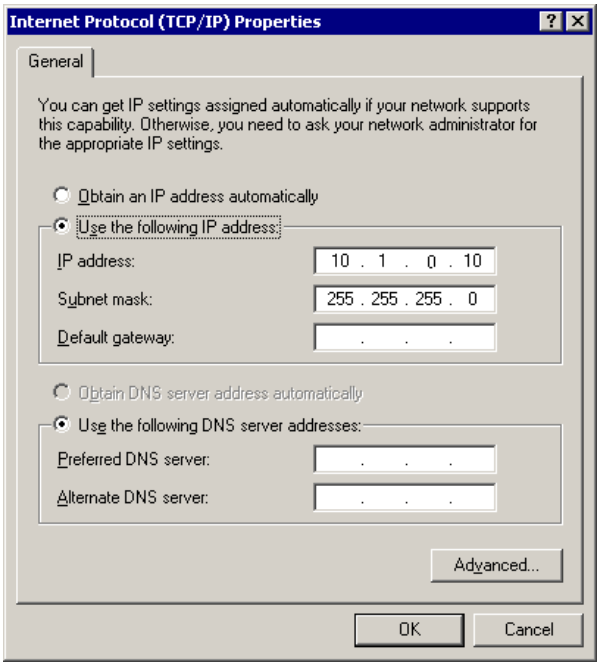
12. Access the files on the RV2 by reading or writing.

WARNING! Do not attempt to write to the RV2 at any time while data is actively recording Doing so may corrupt data currently being stored.

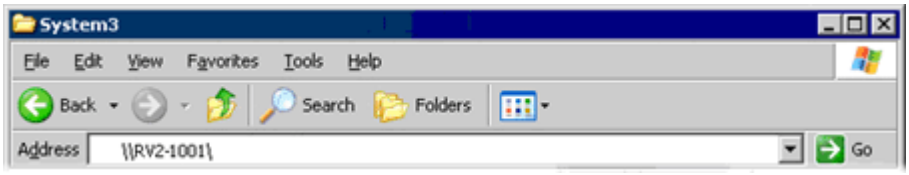
Using Windows XP

To access the RV2 file system through a PC:

1. You will have to configure the PC TCP/IP settings. Open **Control Panel** then double-click **Network Connections.**
2. Right-click the desired connection (this is usually a Local Area Connection) and select **Properties.**
3. Select Internet Protocol (TCP/IP) or if there are multiples, select Internet Protocol (TCP/IPv4).
4. Click the **Properties** button.
5. Select **Use the following IP address** and enter these values:
   IP address: 10.1.0.x, where x can be any value from 1 to 254 except 42.
   Subnet mask: 255.255.255.0
   Default gateway: Leave empty



6. Click **OK.** The RV2 can now be accessed by the PC.
7. Obtain the RV2 device address.
   a. Press the **Live** tab on the RV2 interface.
   b. The device address is displayed at the top of the page to the right of **Device Name** field.
8. Enter the device address as shown in a windows address bar to access the RV2 file system.



Typically, the path \\RV2-XXXX\ is used to access the RV2 storage array, where XXXX is the device serial number, but the name should be verified on the Live tab.

9. Access the files on the RV2 by reading or writing.

 WARNING! Do not attempt to write to the RV2 at any time while data is actively recording. Doing so may corrupt data currently being stored.

Connecting Through a Network

Connection to a local area network also allows data to be viewed and modified through the standard Microsoft Windows file sharing protocol from any PC connected to the same network as the RV2.

To access the RV2 file system through a network:

1. DHCP must be enabled on the network in order to access the RV2. If DHCP is disabled or not supported, you can connect the RV2 directly to a PC.
2. Obtain the RV2 device address.
   a. Press the **Status** tab on the RV2 interface.
   b. The device address is displayed in the middle of the page just under the **Fan Speeds**.
3. Enter the device address in a windows address bar to access the RV2 file system.
4. Access the files on the RV2 by reading or writing.

 WARNING! Do not attempt to write to the RV2 storage array at any time while data is actively streaming. Doing so may corrupt data currently being stored.

Finding the MAC Address

In some labs, the network administrator may require RV2 users to provide the device's MAC address.

To determine the address, follow the instructions below:

1. On the touchscreen interface, press the Status tab. Press in the Current IP field.
2. A Network Configuration dialog is opened and the MAC address is displayed at the bottom of the pop-up window.

Note: If the RV2 does not automatically identify on a network, you can force it to reset its IP address by unplugging the Ethernet cable the plugging it in again.

RV2 Storage Format

The RV2 has three main storage folders – configs, recordings, snapshots.

Configs: All of the rvm configuration files sent from RVMap are stored here.

Recordings: For each recording, a new folder is created that contains the avi file, the rvm used for that recording and a text file (tracking.txt) that contains the results of the tracking algorithm. The tracking.txt file contains a list of frame numbers and tracked point information for each frame. The total number of points may exceed the 8 tracked target limit of the RZ2

Snapshots: Holds JPG images from when the Snapshot button was pressed on the Live tab of the RV2 interface.

Naming Convention

When connected to an active network, TDT's OpenEx software sends information to the RV2 via a broadcast UDP packet allowing it to properly name the video file recorded on the RV2. This allows you to easily match up the video with data stored in the tank. For example, if you are recording for the event Vid0 in Block-3 of DemoTank2 the RV2 will store in the following location and format:

\recordings\DemoTank2\Block-3\DemoTank-Block-3_Vid0.avi

Without the OpenEx network information the RV2 falls back to the default data format:

\recordings\YYYY-MM-DD hh_mm_ss\YYYY-MM-DD hh_mm_ss.avi

Note: The snapshots always store in the default format.

\snapshots\YYYY-MM-DD hh_mm_ss.jpg

RV2 Features

Power Button

A power button located on the front plate of the RV2 is used to turn the device on and off. Prior to powering on/off, the device will enter a brief boot/shutdown period.

Important! Only power the RV2 down when it is not actively recording a video. Failure to do so may result in the RV2 performing a file system check during the next boot process and possible data loss.

Note: If the RV2 becomes unresponsive and fails to shutdown normally, you can shut the device down by holding the power button for longer than five seconds. This will force the device to shutdown. After a forced shutdown, the RV2 may perform a file system check.

LCD Touch Screen

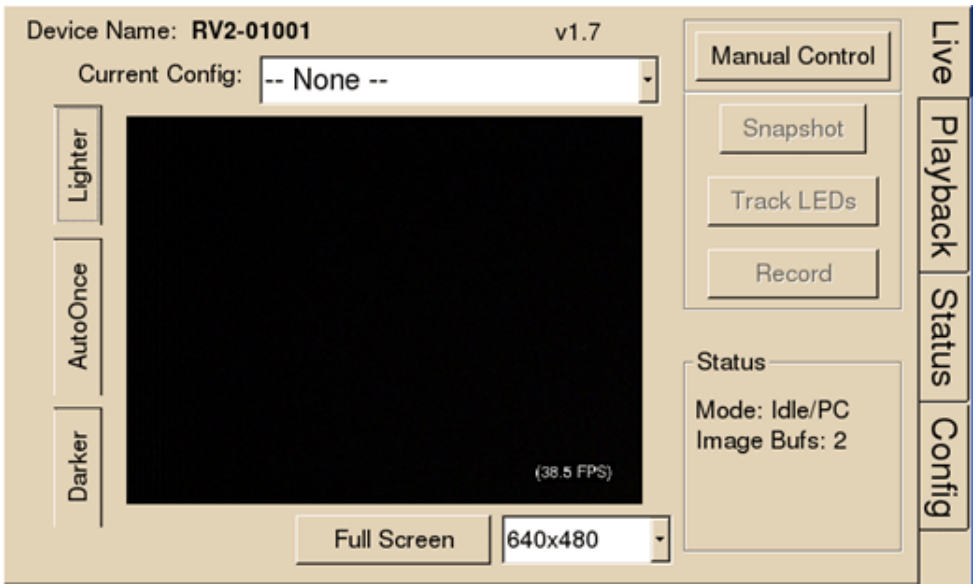
The LCD touch screen allows navigation through the RV2 interface. To make a selection, gently press the touch screen on the desired item.

Interface

The interface reports information and allows configuration of available options. A selection tab located on the right-side of the screen allows the user to select between the available pages. To navigate to the desired window, press the corresponding tab on the right side of the LCD screen.

Live

The Live tab shows the current image captured by the camera, allows changes to the camera settings, and allows the user to choose the current tracking configuration.



Device Name: The NetBIOS name of the device.

Firmware Version: The currently installed firmware version number. This is useful for identifying the current firmware version and also to verify that a recent firmware update has been installed. See "Config" on page 9-15, for more information on updating the firmware.

Current Config: A dropdown list of all available configurations. Tap a configuration to select it.

AutoOnce: Tells the camera to perform its built-in auto-adjustment of exposure, gain and white balance.

Lighter/Darker: Adjusts the exposure time longer and shorter, respectively.

Full Screen: Displays the camera image over the entire screen. Tapping on the full screen image returns the interface to normal.

Resolution: (v1.6b & above) A dropdown list at the bottom of the screen controls the camera resolution (640x480 or 320x240). Lower the resolution to achieve a higher frame count.

Manual Control: Enables the Snapshot, Track LEDs and Record buttons. You cannot record from OpenEx while the RV2 is in Manual mode. When in Manual Control mode, tap the Manual Control button to disable Manual Control.

Snapshot: Copies the current camera image to a JPG file on the RV2 hard drive, into the snapshots folder.

Track LEDs: Applies the tracking specification in the currently selected configuration file to the live camera feed. If colored targets are tracked, dots will appear in the image where the algorithm is finding targets. Use this mode to

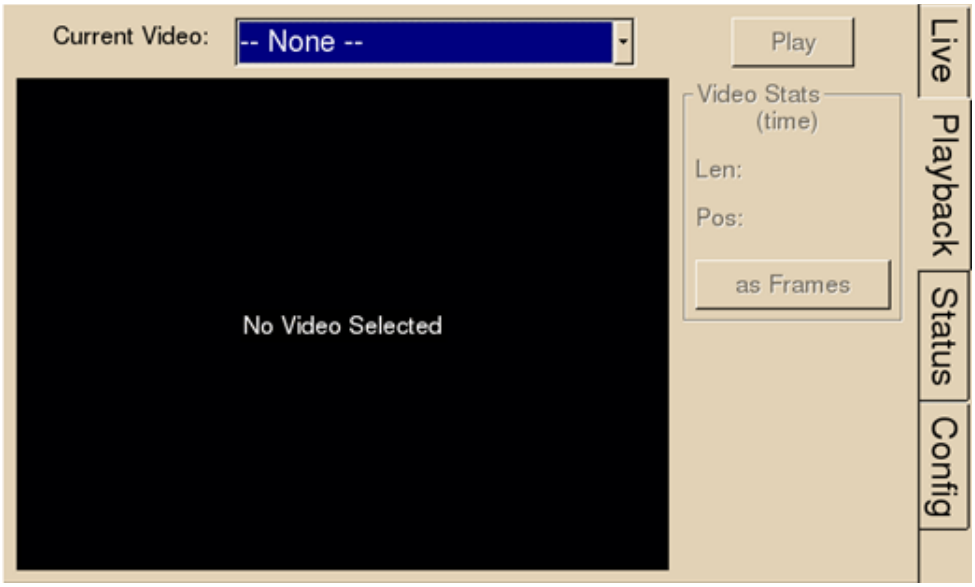
preview the efficiency of the tracking algorithm and then modify the configuration and/or camera settings if needed.

Record: Performs a manual recording. Since the camera is in free-run mode the frame rate will be maximized. Tap Record again to stop recording.

Color: Switches between color and black-and-white modes.

Playback

The Playback tab provides a list of video files currently stored on the RV2. Videos may be reviewed through this interface. The video's length is displayed, in time or in frames, as well as the current position.



Current Video: A dropdown list containing all video files on the RV2. Tap a video name to select it.

Play: Begin playing the currently selected video. Tap again to pause playback. To restart the video, you must select a different video and then select the original video.

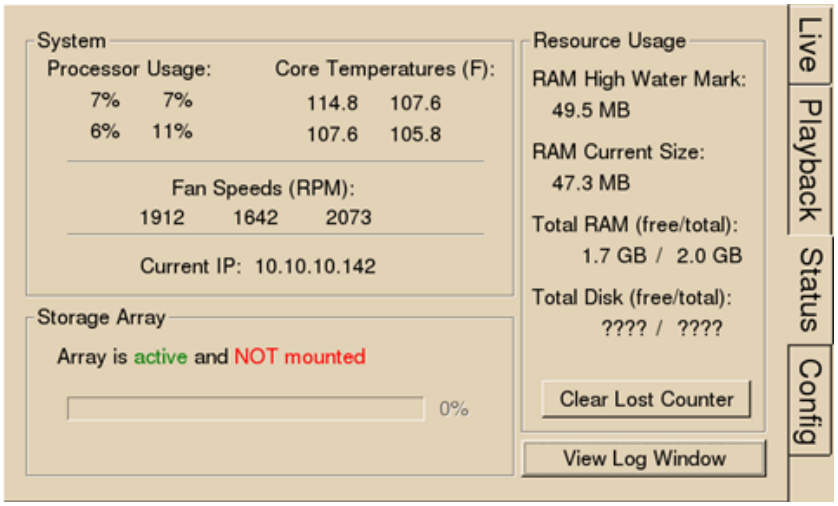
As Frames/As Time: Switch the Video Stats units from time to frames.

Synchronized playback: When tank data is accessed by a TDT application (such as OpenExplorer or OpenScope) the application will detect epoch event names that begin with 'Vid'. When the TDT application retrieves data from that epoch, the TDT application will send a UDP packet containing the tank name, block name and current value of that epoch (which corresponds to the frame number). An RV2 on the network will receive the packet, open the corresponding video file (if it exists) and jump to that frame. The RV2 must be on the Playback tab for this functionality.

Rerun tracking algorithm: While playback is occurring on the RV2, the rvm file in the same directory as the avi file on the RV2 file system is used to run the tracking algorithm and overlay the results on the video image.

Status

The Status tab provides system information such as processor usage rates, core temperatures, fan speeds, device IP address, array reformat progress, memory buffer allocation, and communication errors. Log information can also be retrieved from this tab.



System: Displays important system status information.

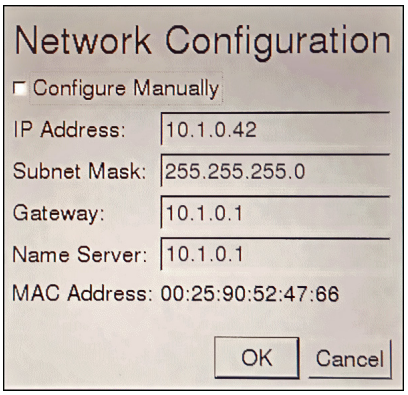
Processor Usage: Displays the current percent usage for each processor core.

Core Temperatures (F): Displays the current processor core temperatures measured in Fahrenheit. The text will turn yellow or red if the processor gets too hot. This can occur if there is an issue with the heatsink or internal fans. When this happens the RV2 will sound a warning and should be shut down immediately.

Fan Speeds (RPM): Displays the approximate rpm for all three fans located inside of the RV2.

Current IP: Displays the IP address currently assigned to the RV2.

Press to display Network Configuration Window.



Configure Manually - select to enable manual configuration and make fields editable.

Storage Array: Displays information about the state of the current storage array.

Active and mounted: Storage array is available and ready to store data.

Active and not mounted: A support storage array is available but is not configured to store data.

Array was not found!: The system did not detect a supported storage array.

Progress bar: Displays progress for various processes which run on the RV2 including:

Reformatting: When reformatting a storage array, the progress completed (%) as well as the estimated amount of time remaining is displayed.

Resyncing: If a mirrored array type has been formatted, the progress completed (%) as well as the estimated amount of time remaining for the Resync process is displayed.

File System Check: The RV2 will perform a file system check during the boot process once every 30 boots. This ensures the integrity of the storage array and file system. If the RV2 is performing a file system check, the progress completed (%) and estimated amount of time remaining is displayed. During this time the Playback tab will be disabled and the RV2 cannot be triggered for storage.

Memory Usage: Displays current and maximum memory (RAM) usage since last reboot

Memory Usage: High Water Mark displays the most memory used by the system since last reboot. Current Size displays the currently used memory. Total System (free total) indicates how much memory is available vs how much total memory the system has.

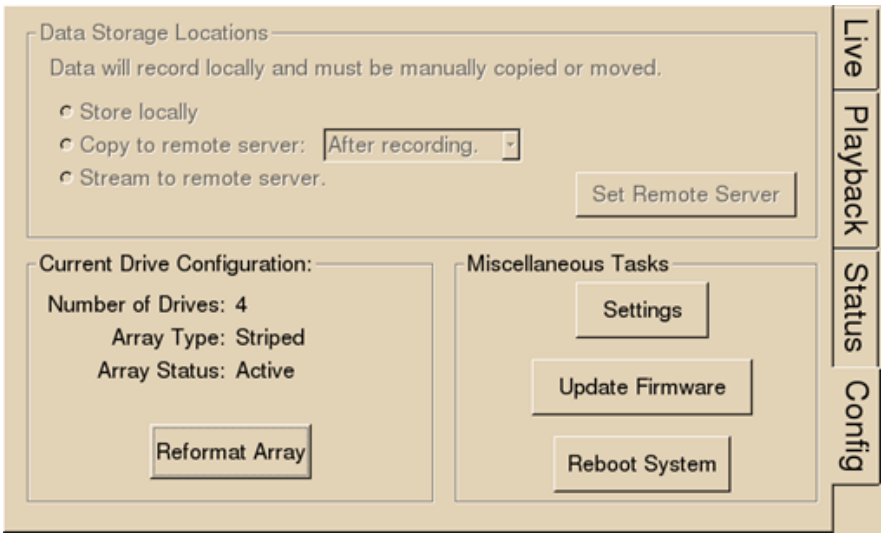
Clear Lost Counter: Resets the lost frame counter.

View Log Window: A log stores relevant messages and any communication errors encountered while the RV2 is in use. Click to open and view the log window. The log.txt file can be copied from the storage array for transfer to a PC.

Note: Individual comments can be saved as well. Use a drag gesture to highlight the desired comment(s) and click Save to write the selection to the log.txt file.

Config

The Config tab provides options for reformatting the currently installed storage array, updating the RV2 firmware, and rebooting the system.



Data Storage Locations: Not currently implemented.

Current Drive Configuration: Displays information about the currently installed data drives.

Number of Drives: Displays the number of drives currently installed.

Array Type: Displays the currently configured array type and the status of the drives.

Striped: Array type is currently configured as striped.

Mirrored(UU): Array type is currently configured as mirrored. A U indicates that a drive is up and running. A _ indicates a drive failure.

Missing: No array type is detected.

Array Status: Displays the current status of the array.

Preparing: Storage array is currently being reformatted.

Resyncing: Storage array is being reformatted as a mirrored array and is currently resyncing the mirrored partitions.

N/A: Storage array is not detected.

Active: Storage array is detected and configured.

Reformat Array: Press to prompt the reformat array dialog. This dialog will ask for confirmation as well as the desired array type: Striped or Mirrored. Reformatting an array will erase all data contained in the array. **Note:** When reformatting an array, the interface may become temporarily unresponsive.

Miscellaneous Tasks: Provides options for updating the current RV2 firmware and rebooting the system.

Settings: Press to display the settings window, then set date and time and select unit of measure for temperature.

Update Firmware: Press to update the RV2 firmware. Firmware is downloaded from the TDT server and automatically installed on the RV2. Connection to a DHCP enabled network that has Internet connectivity is required to retrieve any updates.

Reboot System: Click to reboot the system.

Device Status LEDs

The device status LEDs report streaming or network activity. The following tables display the status LED indicators.

Video	Status	Information
	Off	No video camera is detected.
	Lit	Video camera has been found
Network	**Status**	**Information**
	Off	No network traffic detected.
	Lit	Network traffic is present and detected on the RV2.
Storage	**Status**	**Information**
	Off	No storage access to the RV2 is detected.
	Lit	Storage access to the RV2 is in progress

Ethernet Ports

Two Ethernet ports are provided on the back panel, Video and Network.

Camera-1 The Camera-1 port connects directly to the Ethernet port on the VGAC. **Important!** The cable connecting the RV2 to the VGAC MUST support gigabit Ethernet (e.g. Cat 5e, Cat 6).

Network The Network port allows connections to either a PC or local area network via a standard Ethernet cable. The RV2 supports automatic DHCP protocol.

Power Port

A 9-pin serial port is provided on the back panel, labeled Power. This port is connected to a special cable that provides power to the VGAC using the special gray cable provided with the system.

VGA Port

A VGA port is provided on the back panel, labeled Monitor. This port can be connected to an external monitor that will show the current camera image or a video that is being played in the Playback tab.

Important!: The external monitor must be connected before the RV2 is powered on.

USB 2.0 Port

This port is currently not in use.

Technical Specifications

Processing Cores	4
Storage Array Size	2 Terabytes
System RAM	2 GB
Number of Video Inputs	1
Frame Rates (typical with standard VCAC)	640x480 color -- 40 FPS 320x240 color -- 100 FPS (firmware v1.6b and above)
Video File Format	DIVX encoded AVI

VGAC Specifications:

Camera type	CCD
CCD sensor size	1/3"
Aperture (f/#)	F1.4
Focal Length	4.0 – 8.0 mm
Resolution	8-bit per channel (24-bit total)
Features	Auto Exposure Auto Gain Auto White balance
Field of View (degrees)	vertical = 57.2, horizontal = 70.6
Spatial Resolution (minutes)	vertical = 16.3', horizontal = 15.7'
Resolutions	640x480 color 320x240 color
Cables Provided	Power: 30 ft (9 m) Ethernet: 30 ft (9 m)

Troubleshooting

The following section provides examples and solutions to some of the errors that could be encountered while using the RV2 Video Tracker.

Device Will Not Power Up

Check the position of the power supply switch. If set to the "O" position the power supply is disabled. To enable, simply ensure that the switch is in the "1" position and attempt to power on the RV2. If the device does not power up after verifying that the power supply is enabled contact TDT.

Can't Access the RV2 Storage Array

Check the Ethernet cable connection to ensure that the RV2 is connected to a network or PC using the Network Ethernet port located on the back panel of the RV2. If the Ethernet cable is connected to the Video Ethernet port, network traffic will cause the Network status LED to light up. See "Setting-Up Your Hardware" on page 9-5, for connection diagrams.

If you are attempting to access the RV2 through a network, ensure that the server supports DHCP. If not, the RV2 will default to its static IP address (10.1.0.42). If you encounter this issue, see "Direct Connection to a PC" on page 9-7, for information on how to access the RV2 using a direct connection to a PC.

RV2 Interface Becomes Slow or Unresponsive

Every thirtieth time the RV2 is booted up, it performs a disk check. The length of time required to perform this check depends on how much video data is currently stored on the RV2. During this time, the Playback tab will be grayed out and you will be unable to record to the RV2. The Status tab. TDT recommends removing unnecessary data remaining on the storage array.

RV2 Is Not Correctly Naming Data Folders

When connected to an active network, TDT's OpenEx software sends information to the RV2 via a broadcast UDP packet allowing it to properly name the video files stored on the RV2. If the RV2 is powered on before connecting the necessary network cables it may default to the basic naming format. Power off the RV2, connect all the necessary cables then power the RV.

RVMap Software for RV2

RVMap Overview

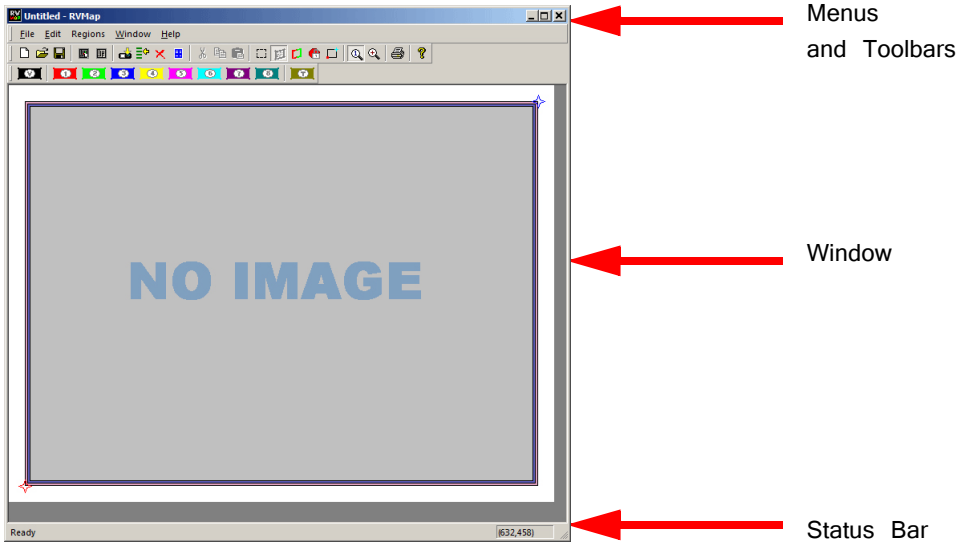
The RVMap application provides a simple visual interface to define regions and targets for video tracking. RVMap is installed with TDT drivers, version 72 or greater. See "Setting-Up Your Hardware" on page 9-5, for information on setting up the RV2 video processor, VGAC camera, and RZ recording system.

The overall process for using the RVMap is as follows:

1. Get a snapshot of the experiment space from the camera connected to the RV2.
2. Describe targets that will be tracked in the experiment space and regions of interest.
3. Upload the configuration to the RV2 file system.

The Workspace

RVMap provides a workspace where users can display a camera snapshot and define regions and targets.



Window

The main workspace window displays an image from a camera or loaded file. Click-and-drag tools are used to define regions and targets on a map overlaying the image.

Menus and Toolbars

A comprehensive set of menus and toolbars provides access to commands and tools. Frequently-used commands are available via toolbar buttons. Move the mouse pointer over a toolbar button to display the button name. A tool tip for the button is also displayed in the Status Bar. See “Menu and Toolbar Reference” on page 9-34, for a complete list of commands and tools. Context sensitive menus are available by right-clicking the workspace.

Status Bar

A status bar along the bottom of the window displays status messages, tool tips. The right side of the status bar displays the coordinates of the pointer.

Creating a Configuration

Before a recording session can be started, an RVMap configuration file (*.rvm) must be created, saved, and uploaded to the RV2. Configurations are created by drawing regions and targets to create a map overlaying a reference image. The *.rvm files contain region descriptions, reference points, target descriptions and camera settings.

Loading an Image

RVMap can load a snapshot image from a connected RV2 and camera or from a previously saved image file.

Loading Existing Image Files

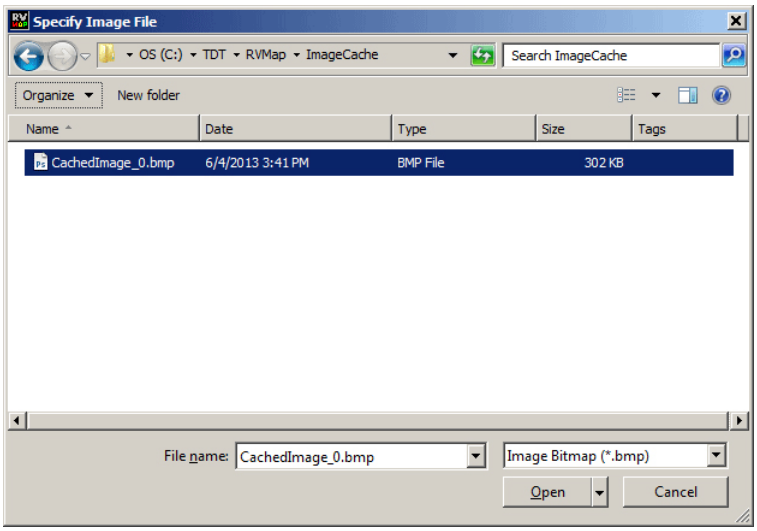
To load an existing image:

1. Click the **File** menu and click **Load Image**.

   or

   Click the  **Load Image** button on the Standard Toolbar.
2. The Specify Image File dialog box is launched.

   Browse to the desired folder.



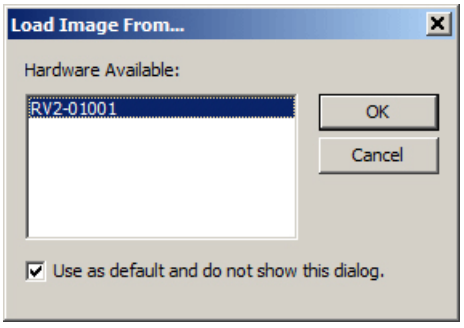
3. Select the image file and click **Open**.

Loading Images from the RV2

RVMap can auto-detect the RV2 and then retrieve a snapshot from a connected camera. Before loading an image from an RV2, ensure the RV2 is on and connected to the PC or network and then connect and position the camera over the experiment space, preferably with the targets visible. Try to make the conditions as close as possible to the recording conditions as this will aid in creating accurate target and region definitions.

To load an image from the RV2:

1. Click the **File** menu and click **Load Image from RV2**.
2. If a default RV2 has not previously been defined, the **Load Image From** dialog is opened.



In this dialog box, any available RV2s connected to the system or available across a network will be displayed.

In the *Hardware Available* list, select the desired RV2.

Note: Every time RVMap needs information from an RV2, it pings the network for available RV2s and lists them. To make the selected RV2 the default hardware and bypass this step in the future, select the **Use as default and do not show this dialog** check box.

3. Click **OK**. A snapshot from the RV2 is retrieved and displayed.

Defining Regions

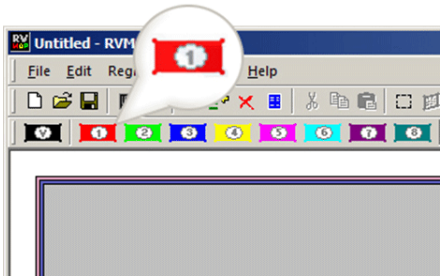
RVMap allows users to define up to eight active regions and one void region. Active regions are numbered one to eight and the corresponding region number will be included in the returned data when a target is found in that region. A void region can be used to eliminate areas of the image which are outside the experiment space. The tracking algorithm will not look for targets in void regions.

Regions are defined by drawing a region shape over the image in the main window. The shape must be a polygon and may have any number of vertices.

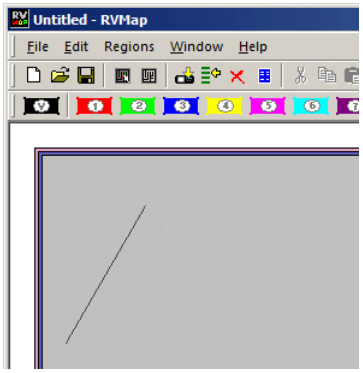
Note: The X,Y coordinates of the pointer are displayed in the right end of the status bar for more specific information about placement of the region vertices.

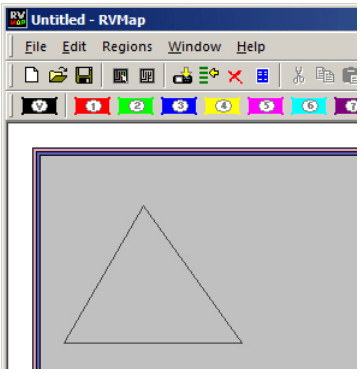
To place a region:

1. Click a region button on the region toolbar.

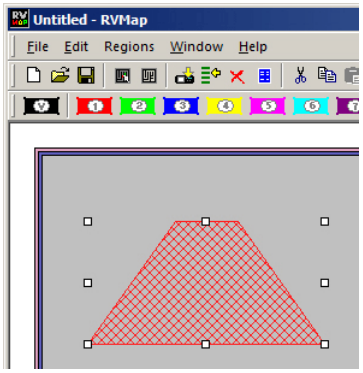


2. Click the image area in one corner of the desired region to begin drawing a polygon. Click each corner of the region in turn to create a vertex point.





3. Double-click the last vertex to complete the region shape.



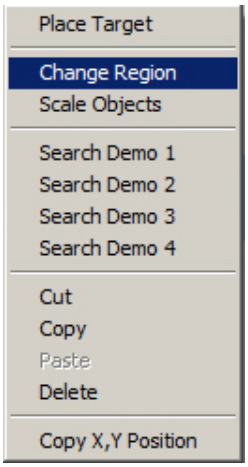
Modifying a Region

To move a region:

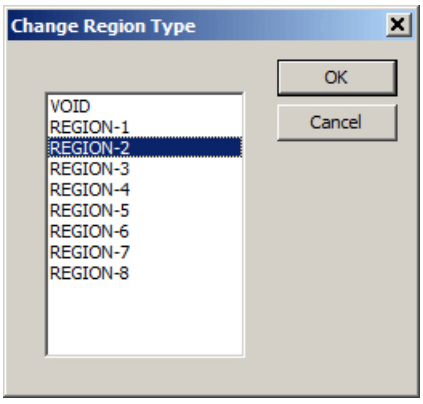
- Click and drag the region to the desired location.

To change the region number:

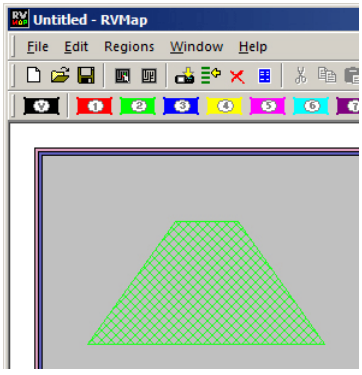
1. Regions are numbered and identified on screen using colors. Right-click the region to be changed.



2. Click **Change Region** on the shortcut menu.



3. In the *Change Region Type* dialog box, select the desired region label in the list and click **OK**.



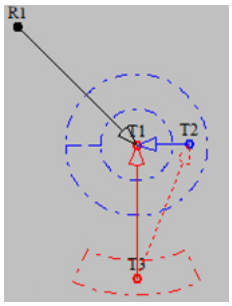
The region has been changed and should be displayed in the color corresponding to the new region number.

Note: Selected regions can also be changed using the *Regions* menu.

To edit the vertices:

1. Hold down CTRL and double-click a region. The regions outline will be wider and the vertices will be selectable.
2. You can now move, add, or remove a vertex.
   - To move a vertex, click and drag the vertex.
   - To add a vertex, hold CTRL and click on the region's boundary to place a new vertex in that location.
   - To remove a vertex, hold CTRL and click the vertex you want to remove.

Defining Targets



Targets are added to the configuration to identify fixed, relative, or reference targets for tracking.

Fixed targets are an easily identified red, blue, or green area on the target subject, such as an LED on a headstage or color marker.

Relative targets are points expected to always be located in a predictable area relative to a previously defined target, such as a second LED on a headstage. This limits the search area, which reduces processing demands and increases accuracy. The location of the relative target can be used to infer information, such as the orientation of the subject and can be used to more accurately place reference targets.

Reference targets are identified based on the location of previously defined target(s). This is a point that maintains a fixed distance and angular separation from other trackable targets but does not have a trackable marker. An example of this is the nose of a mouse wearing a red/green LED headstage.

During recording, the tracking algorithm searches all areas of the image not defined as a void region and identifies the location of the targets. Data for each target (region, 0, x, y) and reference (region, heading, x, y) are saved in a text file (tracking.txt) during each recording session. For each target or reference, the user defines whether or not information is sent back to the RZ for real-time analysis and/or storage. Information from up to eight targets and/or references can be returned to the RZ. The Return option in the Target Specifications determines if the target or reference target will be returned to the RZ.

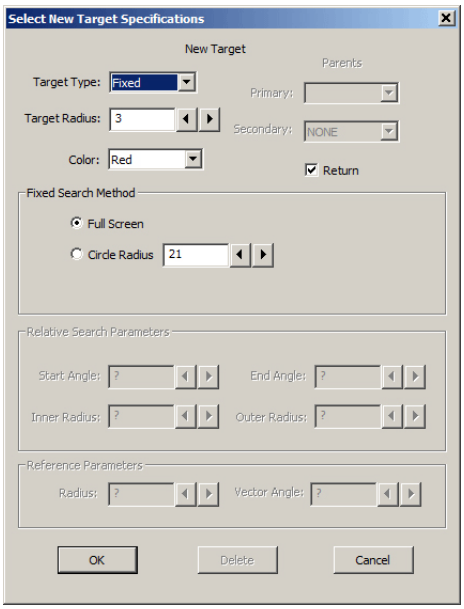
Fixed Targets

At least one fixed target must be placed before any other types of targets.

To place a fixed target:

1. Click the **Target** button on the **Region** toolbar.
2. Click in the image window to place the target.

   The *Select New Target Specifications* dialog opens.

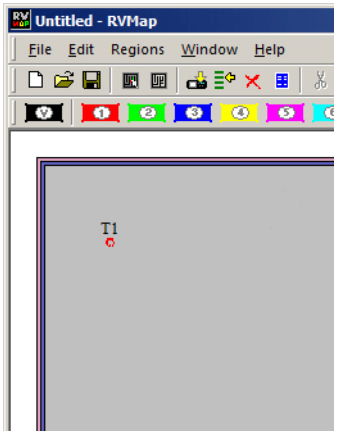


3. Ensure the **Target Type** is set to **Fixed**.
4. In the **Target Radius** box, type a new value to define the target radius (in pixels) or adjust the value using the adjacent arrow buttons.
5. In the **Color** drop-down list, select the desired color or IR/BW for infrared or white light tracking.
6. Select or clear the **Return** checkbox to determine if data from this target will be sent back to the RZ for real-time analysis and/or storage.
7. Under *Fixed Search Method* select the radio button for the desired method.

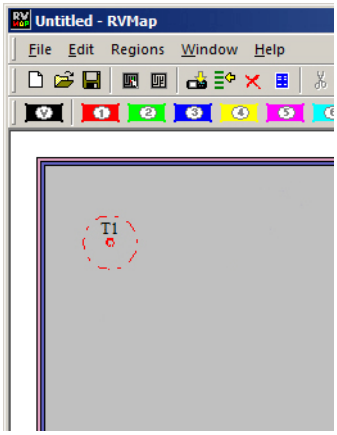
   Full Screen: Search for a target of the defined color and radius in any location in the image window (except Void regions).

   Circle Radius: Search for the target in a particular circle in the image window. If this option is selected, enter the radius in the Circle Radius value box or use the arrows to adjust the value.
8. Click **OK**.

Fixed Target with Full Screen Search



Fixed Target with Circle Radius Search



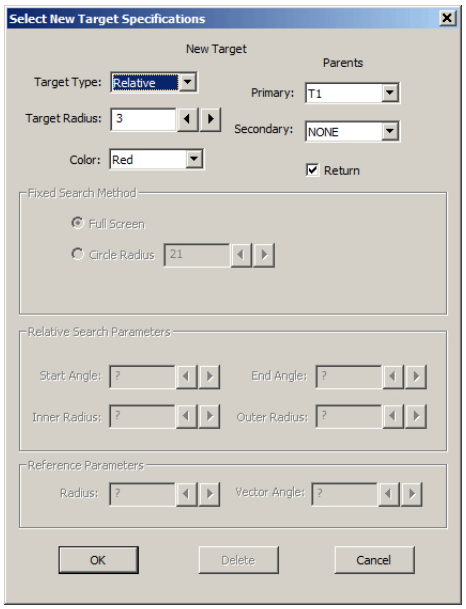
Relative Targets

Once a Fixed target has been placed, a Relative target can be placed. An arc segment around the Fixed target determines a search area for the Relative target.

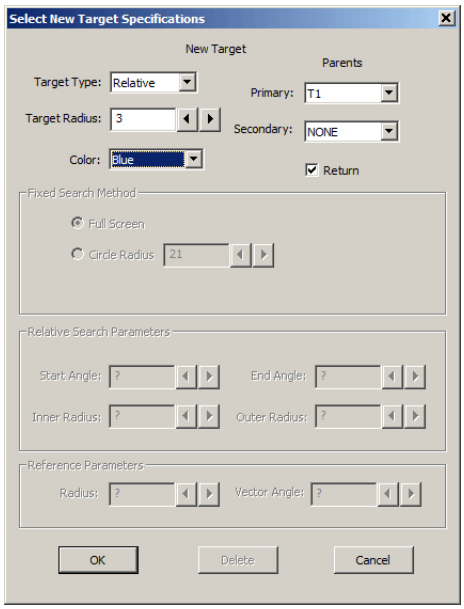
To place a relative target:

1. Click the **Target** button on the **Region** toolbar.
2. Click the target in the image window.

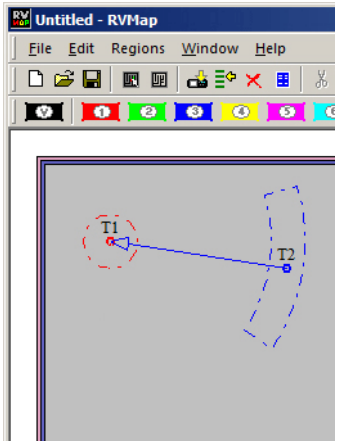
   The *Select New Target Specifications* dialog opens.
3. In the **Target Type** dropdown list, select **Relative**.



4. In the **Target Radius** box, type a new value to define the target radius or adjust the value using the adjacent arrow buttons.
5. In the **Color** drop-down list, select the desired color or IR/BW for infrared or white light tracking.



6. Under *Parents*, select the desired target from the **Primary** and **Secondary** (if there are more than two targets already) drop down lists.
7. Select or clear the **Return** checkbox to determine if data from this target will be returned to the RZ for real-time analysis and/or storage.
8. Click **OK**.

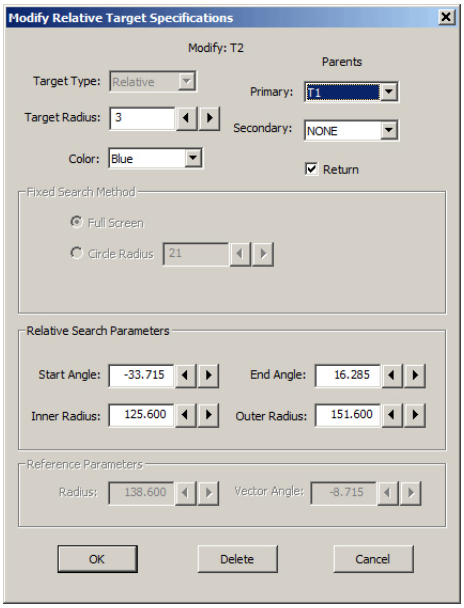


The *Relative Search Parameters* can be modified after the Relative target has been added.

To modify the parameters:

1. Double-click the target.

   The *Modify Relative Target Specifications* dialog box opens.



2. Type values or use the arrow buttons to adjust the values of the search area Start Angle, End Angle, Inner Radius, and Outer Radius. This defines the shape of the arc to look in. Enter -180 and 180 for the Start Angle and End Angle, respectively, to search in a complete circle.
3. To apply the changes, click **OK**.

Reference Targets

Reference targets can be created after one or more *Parent* targets have been place. References can be placed with one or two *Parents*.

When only a *Primary Parent* target is defined, the distance and angle (relative to 0, i.e. the horizontal axis) from *Reference* target to the *Primary* target is preserved.

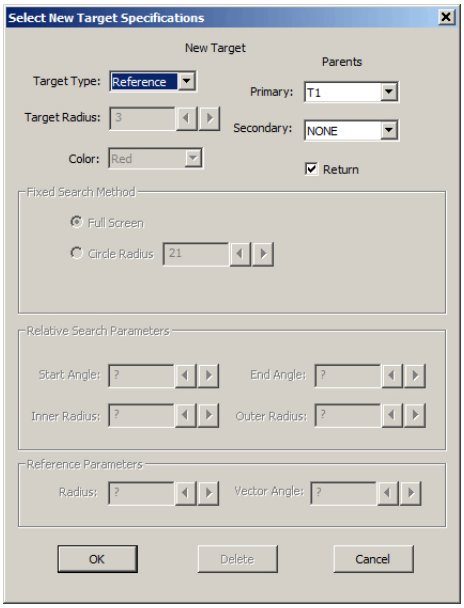
When two *Parent* targets are defined, the distance from the reference to the *Primary* target is preserved, and the angle from the *Secondary Parent* to the *Primary Parent* to the *Reference* target is also preserved.

Example: When a two LED headstage, red and green, is used with a mouse, a reference point may be placed on the nose. There is no LED there, but the distance from primary target to the nose is constant, and so is the angle between the green LED, the red LED and the nose. In this way the nose can be tracked without having to place an LED directly on the nose.

To place a reference target:

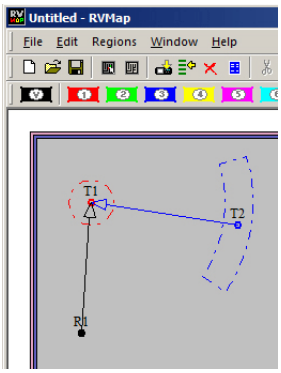
1. Click the **Target** button on the **Region** toolbar.
2. Click the target in the image window.

   The *Select New Target Specifications* dialog opens.
3. In the **Target Type** dropdown list, select **Reference**.



4. Under *Parents*, select the desired target from the **Primary** and **Secondary** (if applicable) drop down lists.
5. Select or clear the **Return** checkbox to determine if data from this target will be returned to the RZ for real-time analysis and/or storage.

6. Click **OK**.



Saving Configurations

The configuration is saved to an RVMap file (*.rvm).

To save the map file:

1. Click the **File** menu and click **Save As**.
2. Browse to the desired location, type a name in the **File name** box, and click **Save**.

To upload to an RV2:

1. Click the **File** menu and click **Send Config to RV2**.

   or

   Click the  button on the toolbar.
2. If prompted, select the hardware.
3. In the Create/Replace Config dialog box, enter a name in the New Config Name box and click **Send**.
4. Verify that the new config is listed as the Current Config on the Live tab of the RV2 interface.

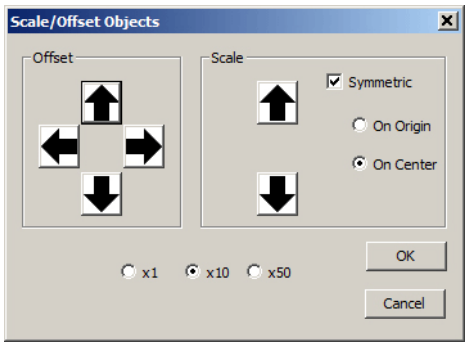
   You are now ready to begin your OpenEx recording.

Scale/Offset Objects

The entire map can be scaled or offset using the Scale/Offset Object tools. These tools simplify adjustments to the map that may be required if the distance or placement of the camera has changed since the map was configured.

To open the Scale/Offset Objects dialog:

- Click the **File** menu and click **Scale/Offset Objects**.

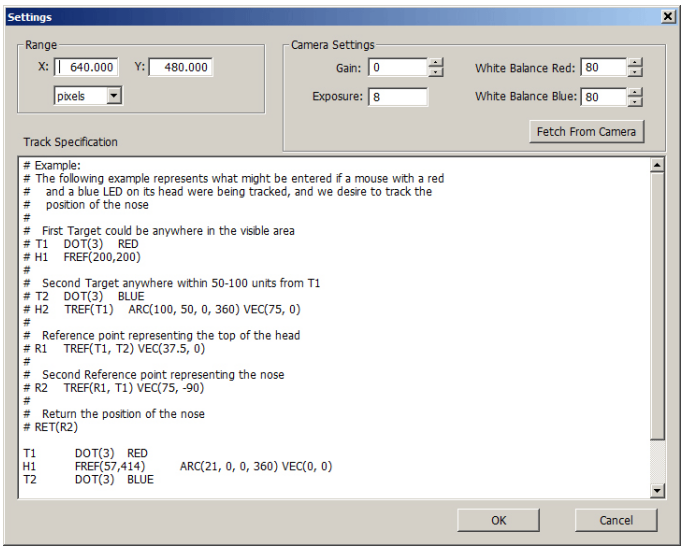


Offset	Click arrows to offset (move) the map in the indicated direction.
Scale	Choose among the options then click the arrows to adjust the size of the map.
Factor	Choose x1, x10, or x50 to determine the factor of adjustments applied when using the scale or offset arrows.
OK	When adjustments are complete, click to close the dialog and apply the changes.
Cancel	Click to discard changes.

Workplace Settings

The workplace settings, including range/units of the display, camera settings, and tracking details can be accessed in the Settings dialog bog.

The Settings dialog can be opened using the  Settings button on the toolbar or from the File menu.

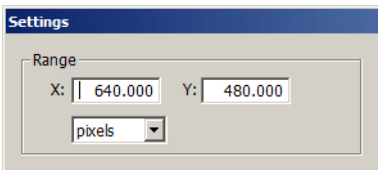


Reference Points and Range

The units/scaling of the workplace and all X, Y coordinate values returned by the tracking algorithm are determined by the following image window *Reference Points*:

red star  blue star 

By default, the red star and blue star Reference Points are positioned, respectively, in the bottom left and top right corners of the image. The red star defines the center point (0,0) and the blue star defines the position of the (X,Y) range value in the Settings dialog.



After the range values have been defined, click OK to apply them to the RVMap settings.

The *Reference Points* can be dragged to a new position, such as the location of a known object in a displayed image, to help define a real-world scale for the image. For example, a ruler might be placed in the camera frame and the Reference Point can be dragged to each end of the ruler so that the X,Y coordinates will be redefined based on the ruler visible in the image.

To select and move the *Reference Points* simultaneously:

- Hold down the CTRL key and click each of the *Reference Points*. They are now both selected and both will move in unison.

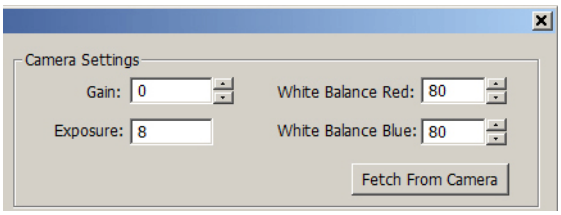
Camera Settings

The Camera Settings area of the Settings dialog box enables user to retrieve settings from the camera so that they can be stored with the configuration and applied each time that configuration is used. The RV2 does not maintain the camera settings after it is rebooted, so it is a good idea to store the current settings in the configuration file. The values you see initially are the default values.

To retrieve the camera settings to be applied each time the configuration is loaded:

- Click **Fetch From Camera**.

The Live tab on the RV2 interface provides an AutoOnce button that tells the camera to perform its own auto-adjustment of exposure, gain and white balance. The Lighter and Darker buttons on the Live tab are used to adjust the exposure time. There is no direct control of gain and white balance on the RV2 interface, so if you want to manipulate those values you will have to adjust them in the Settings dialog and upload the configuration to the RV2 to apply those camera settings. See "Saving Configurations" on page 9-31, for more information on uploading the configuration.



Track Specifications

The Track Specifications area of the Settings dialog box displays details of the current map configurations and can be used to edit and/or enter configurations in a text format.

An example is displayed in the commented text (the lines begin with '#') to provide some description of the structure. Targets can be refined here more precisely than in the GUI. This method is recommended for users who are very familiar with the system and scripting. In general, it is easiest to use the GUI to design the tracking algorithm and visit the Track Specifications textbox later if necessary.

Menu and Toolbar Reference

Menus

File Menu

New	Open a new RV Map file.
Open	Launch the Load RV Map File dialog box.
Close	Close the application.
Save	Save changes to the current RV Map File or launches the Save RV Map file.
Save As	Launch the Save RV Map file.
Load Image	Launch the Specify Image File and enable the user to load a saved snapshot image.
Load Image from RV2	Load a snapshot image from a connected camera. If a default hardware device has not been previously defined, the Load Image From dialog box is launched to prompt hardware selection.
Send Config to RV2	Send the current configuration to the RV2. If a default hardware device has not been previously defined, the Send Config To dialog box is launched to prompt hardware selection.
Use Configs	Retrieve a list of available configuration on the RV2 and allow the user to select a configuration. If a default hardware device has not been previously defined, the Use Config On dialog box is launched to prompt hardware selection.
Purge Configs	Delete the previously saved configurations on the RV2. If a default hardware device has not been previously defined, a dialog box is launched to prompt hardware selection.

Settings	Launch the Settings Window and allow the user to define range, camera, and track specifications.
Exit Manual Mode	If RV2 is manual mode and is NOT recording, a command to exit manual mode is sent. The RV2 will display the message: Remote RvMap User Exited Manual Control.
Page Setup	Enable the user to define specifications for printing the image.
Print	Print the currently displayed image.
Print Preview	Preview how the currently displayed image would be printed.
Recent File	List recently used RV Map files.
Exit	Close the application.

Edit Menu

Undo	Undo the most recent action.
Redo	Redo the most recent action.
Cut	Cut the selection and put on the clipboard.
Copy	Copy the selection and put on the clipboard.
Paste	Insert clipboard contents.
Delete	Delete selection.
Show/Hide Regions	Toggle the region image overlay on or off.
Edit Vertices	Enable click-and-drag editing for a selected region. Drag Vertices to change the shape of the image, or CTRL+click to add/remove vertices along the region boundary.
Scale Objects	Launch the Scale/Offset Objects dialog box.
Change Region	Launch the Change Region Type dialog box and enable the user to change the region label for a selected region.
Lock References	Lock the Reference Points at their current positions.
Reset References	Reset Reference Points to their default positions.
Use Default RV2	Make the currently connected RV2 the default hardware throughout the software.

Regions Menu

Void	Enable multi-click region drawing tool to define a void region.
Region-1	Enable multi-click region drawing tool to define Region-1.
Region-2	Enable multi-click region drawing tool to define Region-2.
Region-3	Enable multi-click region drawing tool to define Region-3.
Region-4	Enable multi-click region drawing tool to define Region-4.
Region-5	Enable multi-click region drawing tool to define Region-5.
Region-6	Enable multi-click region drawing tool to define Region-6.
Region-7	Enable multi-click region drawing tool to define Region-7.
Region-8	Enable multi-click region drawing tool to define Region-8.

Targets	Enable click drawing tool to place a new target.

Window Menu

New Window	Not currently used.
Cascade	Not currently used.
Tile	Not currently used.
Arrange Icons	Not currently used.
Zoom 50%	Display the image in the main window at 50%.
Zoom 100%	Display the image in the main window at 100% (scale 1:1).
Zoom 200%	Display the image in the main window at 200%.

Help Menu

About RVmap	Display program information including version and copyright.

Toolbars

Standard Toolbar

New	Create a new document.
Open	Open an existing document.
Save	Save the active document.
Load Image	Load bitmap image from disk.
Load Image From RV2	Load snapshot from RV2.
Send To Hardware	Send the active configuration to RV2 and set it as the current configuration.
Use Configs	Tell RV2 which rvm file to use.
Purge Configs	Purge unused rvm files from RV2.
Change Settings	Change settings, such as range, camera settings, and tracking details.
Cut	Cut the selection and put on the clipboard.
Copy	Copy the selection and put on the clipboard.
Paste	Insert clipboard contents.

	Show/Hide Regions	Toggle the region image overlay on or off.
	Edit Vertices	Enable click-and-drag editing for a selected region. Drag Vertices to change the shape of the image. CTRL+click to add/remove vertices along region boundary.
	Change Regions	Launch the Change Region Type dialog box and enable the user to change the region label for a selected region.
	Lock Reference Points	Lock the Reference Points at their current positions.
	Reset Reference Points	Reset Reference Points to their default positions.
	Zoom 100%	Zoom to 100% (scale 1:1).
	Zoom 200%	Zoom to 200%
	Print	Print the active document.
	About	Display program information including version and copyright.

Region Toolbar

	Draw Void Region	Select pen to draw void region.
	Draw Region 1	Select pen to draw region 1.
	Draw Region 2	Select pen to draw region 2.
	Draw Region 3	Select pen to draw region 3.
	Draw Region 4	Select pen to draw region 4.
	Draw Region 5	Select pen to draw region 5.
	Draw Region 6	Select pen to draw region 6.
	Draw Region 7	Select pen to draw region 7.
	Draw Region 8	Select pen to draw region 8.
	Draw Targets	Select pen to place a new target.

Part 10: MicroElectrode Array Interface

MZ60 MicroElectrode Array Interface

MZ60 Overview

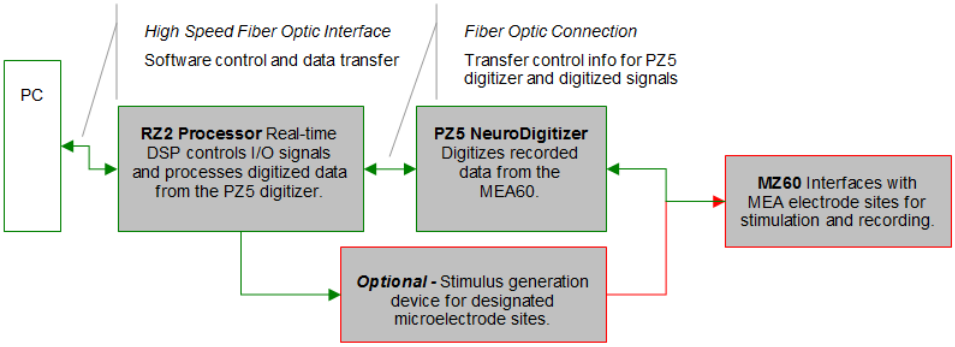
The MZ60 Microelectrode Array (MEA) Interface is used with our RZ2 BioAmp Processor and the PZ5 NeuroDigitizer (or PZ2 Amplifier) as part of a complete solution for high spatio-temporal resolution tissue slice and cell culture recordings.

The interface supports simultaneous stimulation and extracellular in-vitro recording on up to 60 channels. Headstage buffering on the MZ60 provides high signal-to-noise ratio, sensitivity, and stability for long experimental durations.

The MZ60 is compatible with a large selection of MEA plates and both inverted and upright microscopes.

The MEA System

A typical system consists of an RZ2 processor, a PZ5 digitizer and the MZ60 MEA interface. An optional stimulus generation device may also be used and controlled by the RZ2 processor as part of an integrated solution. The diagram below illustrates the function of the components in the system.



MEA System Diagram

The MZ60 acquires analog input signals from cell lines or tissue slices via an MEA plate and sends those signals to the PZ5 digitizer. All channels are digitized on the PZ5 at up to ~50kHz sampling rate per channel. Digitized data is streamed to the RZ2 multiprocessor DSPs on a fiber optic connection and processed data is

transferred to the PC for data storage. A PZ2 amplifier may be substituted for the PZ5 in some cases. A single RZ2 and PZ5 system is capable of interfacing with up to two MZ60's.

Stimulation can be delivered to any of the MZ60's electrode sites while the RZ2 processor simultaneously records from non-stimulus channels and may be provided by the RZ2 processor or an optional stimulus device.

The MEA Interface

The MZ60 is compatible with the standard 49 x 49 mm arrays from NMI or Ayanda Biosystems and can accommodate a wide selection of readily available arrays. The arrays are placed on an aluminum plate and spring loaded connections are secured over the contact pads when the top is lowered and locked using the twist lock mechanism.

A voltage-follower headstage provides a high input impedance and low output impedance with unity-gain. The dynamic range of the MZ60 and PZ5 is 500 mV with a signal resolution of 3 µVolt or less at ~25kHz sampling rate.

The MZ60 channels are organized in four individual 16-channel banks that correspond to banks of channels on the PZ5 digitizer. Each bank transmits 15 analog signals recorded from the MEA to the PZ5 digitizer (the sixteenth channel of each bank is connected to ground and is not used). If any channel is designated for stimulation, it is grounded internally on the PZ5.

Voltage Range

The voltage input range of the PZ5 digitizer is lower than the MZ60 and must be considered the effective range of the system. If using another preamplifier, check the specifications for voltage range. Also keep in mind that the range of the MZ60 varies depending on the power supply provided by the digitizer or preamplifier. the TDT digitizer and preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

Input range when using +/- 1.5 V power source:	Input range when using +/- 2.5 V power source:
+/- 0.9 V	+/- 1.9 V

Hardware Set-up

To insert the MEA into the MZ60:

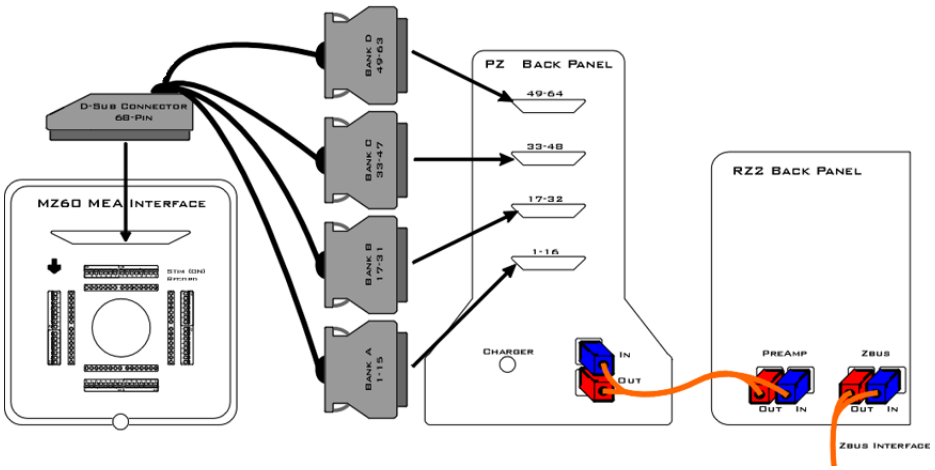
1. Twist the knob on the front edge of the MZ60 counterclockwise to release the hinged top.
2. Lift the top and position the MEA on the aluminum plate.
3. Lower the top and twist the knob clockwise to secure the MEA inside the interface housing.

   Important!: The securing knob on the MEA turns on a screw that allows for pressure adjustment between the MEA plate and the MZ60 interface contact pins. The pressure should be set to achieve only light contact between the spring loaded contact pins and the MEA plate (enough pressure to visually depress the spring contacts). Excessive pressure may cause damage to the device or MEA plate.

Refer to the vendor's specifications of the chosen MEA plate regarding the MEA pinouts and technical specifications of the electrodes.

To connect the system hardware:

1. Ensure that the TDT drivers, PC interface, and device chassis are installed, setup, and configured according to the System 3 Installation Guide provided with your system.
2. Connect the MZ60 Interface to the PZ5 digitizer via the MZ60 interface cable provided. Attach the 68-pin D-Sub connector on the interface cable to the corresponding connector on the MZ60.
3. Attach each of the labeled Mini-DB26 connectors to the corresponding channel bank connector on the PZ5 digitizer.
4. Connect the PZ5 digitizer to the RZ2 processor using the provided fiber optic cable. The fiber optic wires are keyed and color coded to reduce connection errors.
5. Power on the RZ2 processor and PZ5 digitizer.
6. If using the system with other devices, such as a third party stimulus device or preamplifiers, see the documentation for those devices for hardware connection information.



Setup of the MEA System

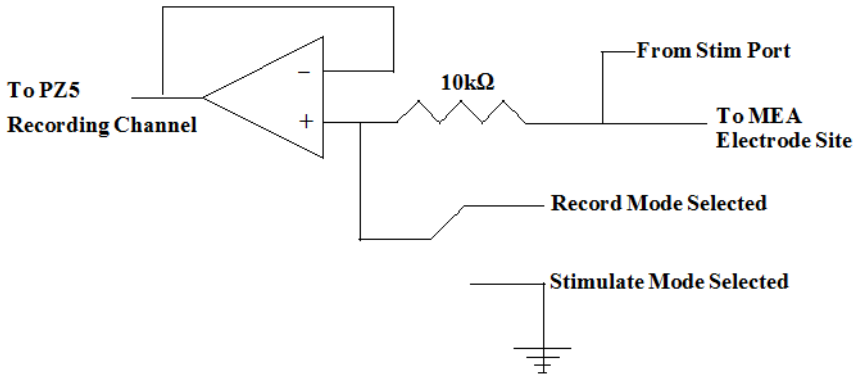
MEA Interface Features

Analog Input and Output

The MZ60 supports MEAs containing up to 60 electrode sites. Any of these analog channels may be configured for recording or stimulus presentation using top panel stimulus switches.

Stimulus Switches

A DIP-style switch for each of the 60 analog input channels controls whether the channel is in Stimulate mode (**ON**) or Record mode (**OFF**).



MZ60 Single Channel Circuit Diagram

Each of the sixty channels can be configured in one of two states:

Record: Channels in record mode are connected to a PZ5 digitizer input channel when the corresponding DIP-switch is in the **OFF** position.

Stimulate: Channels in stimulate mode allow current to pass through the electrode to ground when the corresponding DIP-switch is in the **ON** position. Stimulating channels are not connected to the PZ5 and will not saturate the input to the PZ5 digitizer nor are they connected to the REF line on the MZ60. A common ground pin is available on the MEA Interface.

WARNING! Channels designated for recording are still connected to the corresponding stim port located on the MZ60. To avoid damage to the MZ60 headstage, DO NOT attempt to present stimulus signals to channels configured for record mode.

MZ60 Interface Cable Connector

An interface cable is provided to connect the MZ60 to the PZ5 digitizer. The cable features four mini-DB26 connectors which connect to four banks on the back of the PZ5.

Common Ground Pin

A single ground pin is attached to the MZ60 and serves as the common ground for both stimulating and recording channels on the MZ60. The PZ5 digitizer ground and reference pins for each bank are tied to this pin internally when the PZ5 and MZ60 are connected.

Some MEA plates have an internal reference pin integrated into dish. Please review the MEA dish manufacturer specifications for proper grounding.

Troubleshooting

This section is provided to address common issues that may be encountered when using the MZ60 MEA Interface. If you need assistance beyond the scope of this guide, contact tech support at 1.386.462.9622 or support@tdt.com.

General Tips

When recording signals make sure that the PZ5 digitizer is not connected to the charger as this will induce mains interference in your recordings.

Make sure there are no power strips or AC power sources anywhere near the MZ60 setup. Power strips will induce mains interference into your recordings. Also minimize electrical interference from other electrical devices (50-60 Hz and their harmonics). We recommend that the MZ60 and PZ5 are approximately 1 meter from computers, oscilloscopes, RZ and RX devices and other electronic equipment.

Make sure there is no liquid on the MEA plate contacts. Clean the contacts gently with isopropyl alcohol to assure a clean connection.

Make sure the MZ60 knob is oriented in the correct position. If the MZ60 top is not tight enough, open the MZ60 and ensure that the MEA plate is seated correctly in the MZ60 housing. As you close the MZ60 top ensure that all of the gold pins are touching the MEA electrode dish contacts.

Make sure that all of the spring-loaded contact pins are not stuck in a compressed position. If a pin becomes stuck, use a pair of forceps or small pliers to gently pull the pin out.

MZ60 Noise Floor is Too High

If 50-60 Hz hum (caused by mains voltage sources) is prevalent in your recordings, make sure that the common ground wire is making contact with the liquid in the MEA.

Noisy Single Electrode Channels

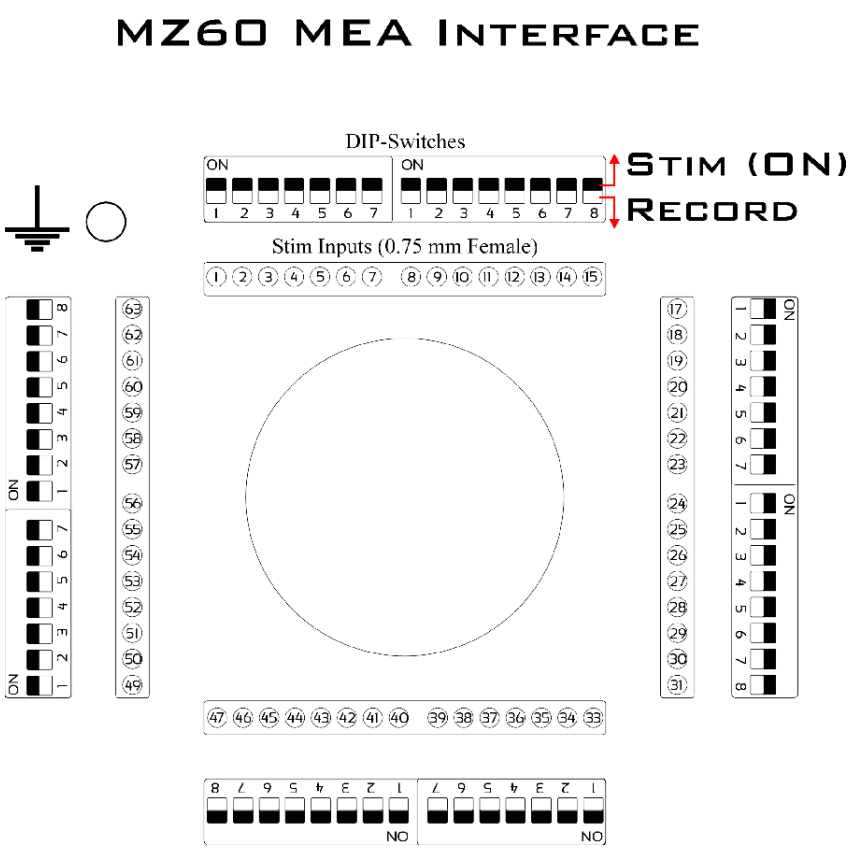
Large noise signals may be a sign of a bad electrode contact or pin. To test the electrode contact, rotate the MEA plate and see if the noise follows the MZ60 channel or the electrode.

If the electrode contact is affected you may remedy the problem by cleaning the MEA contact sites with a cotton swab and some pure alcohol (100%). If the problem persists after cleaning the MEA electrode contacts, the contacts are damaged beyond repair and the MEA plate must then be replaced.

MZ60 Technical Specifications

Stimulus Input Channels	Up to 60 (0.75 mm female input pin)
Analog Input Channels	Up to 60
Input Impedance	10^{14} Ohms
Gain	Unity
Compatible MEAs	Standard MEA Arrays 49 x 49 mm

MEA Connector Pinouts



Stimulate/Record Switching Banks

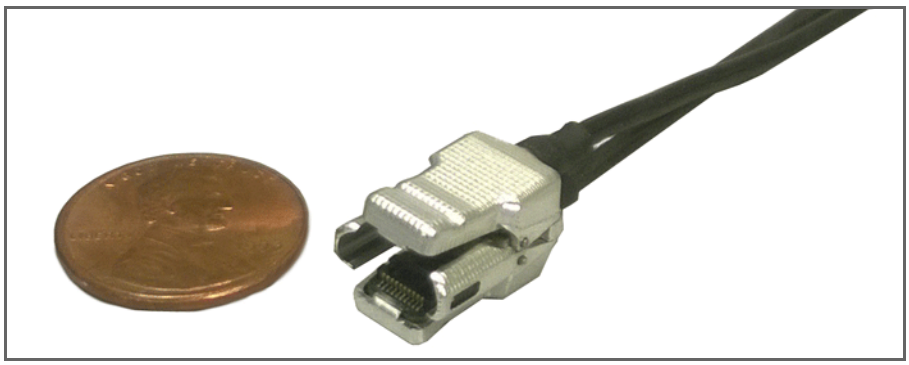
A DIP-switch bank is located on each of the four sides of the MZ60 and toggles between stimulate or record modes for 15 electrode sites. Stimulating inputs accept 0.75 mm male pins.

Pinouts are shown looking into the connector and reflect the digitizer channels assuming the MZ60 is used with a PZ5-64 in Local, None, or Shared reference mode. For higher channel count channel numbers may be offset depending on the MZ60-PZ5 connections.

Note: Channels 16, 32, 48, and 64 are grounded on the digitizer.

Part 11: High Impedance Headstages

ZIF-Clip® Analog Headstages



32-Channel ZIF-Clip® Headstage

ZIF-Clip® ZC Overview

ZIF-Clip® standard headstages are analog headstages recommended for use with probe impedance that range from 20 Kohm to 5 Mohm. They are designed to connect directly to a PZ preamplifier/neurodigitizer but may be connected to an RA16PA with the use of an adapter. Analog signal are buffered inside the headstage and digitized on the preamplifier/neurodigitizer for transfer to a base station processor, such as the RZ2 or RZ5.

By default, ground and reference are separate on all ZIF-Clip® headstages yielding a referential configuration. Reference and ground may be tied together on the headstage adapter or ZIF-Clip® microwire array for single-ended configurations.

The ZIF-Clip® headstage (Patent No. 7540752) features an innovative, hinged headstage design that ensures quick, easy headstage connection with almost no insertion force applied to the subject. ZIF-Clip® headstage contacts seat inside the probe array and snap in place, firmly locking the headstage and probe with very little applied pressure. These self-aligning headstages provide long lasting low insertion performance for a variety of channel number and electrode configurations. An aluminum finish provides increased durability.

Part Numbers:

ZC16 – 16-channel Aluminum ZIF-Clip® headstage

ZC32 – 32-channel Aluminum ZIF-Clip® headstage

ZC64 – 64-channel Aluminum ZIF-Clip® headstage

ZC96 – 96-channel Aluminum ZIF-Clip® headstage

ZC128 – 128-channel Aluminum ZIF-Clip® headstage

ZIF-Clip® Passive Headstages

ZIF-Clip passive headstages contain no active electronics. They provide passive cabling in 16, 32, 64, 96, 128 channel ZIF-Clip form factors.

Part Numbers:

ZC16-P – 16 channel ZIF-Clip® passive headstage

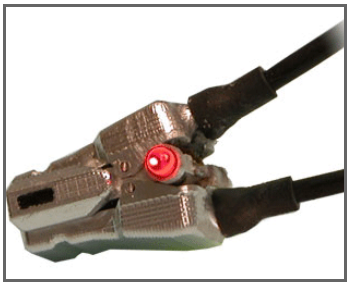
ZC32-P – 32 channel ZIF-Clip® passive headstage

ZC64-P – 64 channel ZIF-Clip® passive headstage

ZC96-P – 96 channel ZIF-Clip® passive headstage

ZC128-P – 128 Channel ZIF-Clip® passive headstage

ZIF-Clip® LED Headstages



ZIF-Clip LED headstages have built-in red and green LEDs on each side. The LEDs provide an ample amount of light for tracking test subjects and are available for 16, 32 and 64-channel ZIF-Clip standard headstages.

Note: ZIF-Clip headstage LEDs cannot be added to existing non-LED headstages.

Part Numbers:

ZC16-LED – 16-channel ZIF-Clip® headstage with LEDs

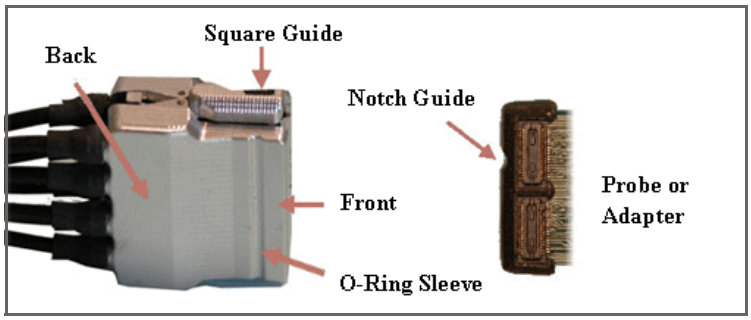
ZC32-LED – 32-channel ZIF-Clip® headstage with LEDs

ZC64-LED – 64-channel ZIF-Clip® headstage with LEDs

Adapter and Probe Connection

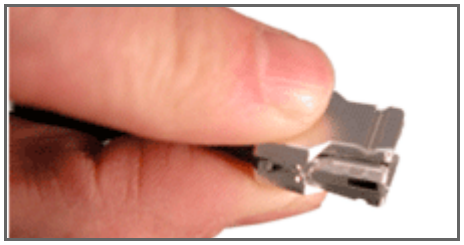
The headstage has sensitive electronics. Always ground yourself before handling.

ZIF-Clip® headstages are designed to automatically position the high density connectors on the headstage and probe (or adapter).

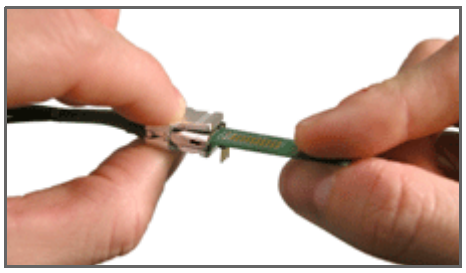


Standard ZIF-Clip® Headstage

Connect probes and adapters to the headstage as described below.

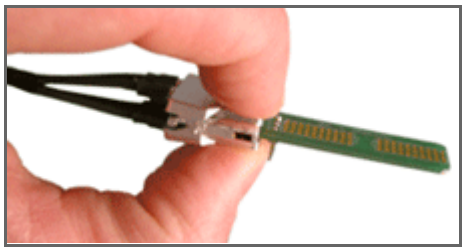


Firmly press and hold the **back** to open the headstage.



Align the **notch guide** of connector to the **black square guide** of the fully opened headstage then move headstage into position.

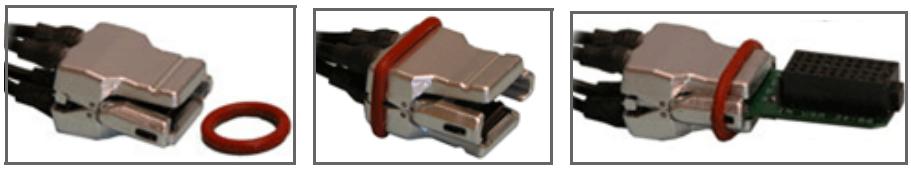
WARNING! The ZIF-Clip® headstage must be held in the fully open position while being slid into position. The headstage should only be closed when fully engaged. Sliding the headstage into position while applying pressure to the tip will **permanently damage** the ZIF-Clip® headstage and micro connectors.



Press the **front** of the headstage together as shown to lock the connector in place. You should hear an audible click when the locking mechanism is engaged.

ZIF-Clip® Headstage O-Rings

All ZIF-Clip® headstages are shipped with two o-rings for additional connection security. Gently slip the o-ring onto the headstage sleeve and then roll the o-ring towards the back of the headstage. Connect the probe or adapter to the headstage as described above. Once the connection is secure, roll the o-ring forward until it settles into the sleeve on the front of the headstage.



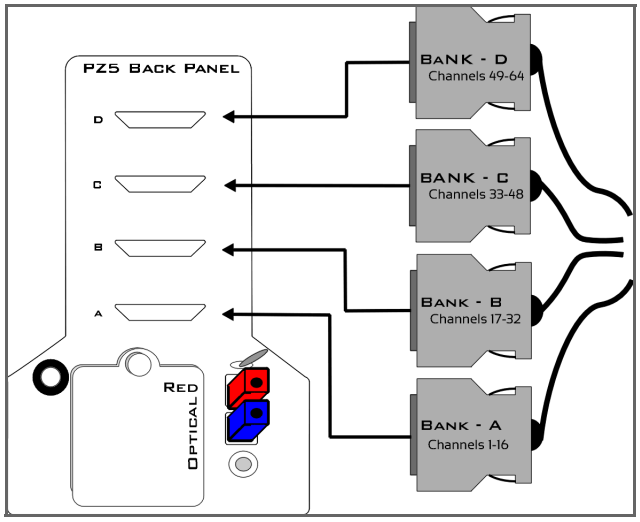
O-Ring Use and Positioning

ZIF-Clip® Headstages to Amplifier Connection

One or more MiniDB26 connectors are used to connect the ZIF-Clip® standard headstage to a PZ5 or PZ2 preamplifier depending on the number of channels in the headstage. Each MiniDB26 connector carries 16 channels and is labeled with a bank letter that corresponds to its matching bank on the preamplifier. For example the MiniDB26 connector labeled "Bank A" should connect to bank A on the PZ5 or bank 1 on the PZ2 and will carry channels 1-16. Subsequently, "Bank B" corresponds to the next 16 channels of the headstage, etc. Below is a table which shows the Bank labels along with their matching PZ5 bank.

ZIF-Clip® Headstage	Bank Label on MiniDB26	Connect to PZ5 Bank
ZC16 (Connects Bank A)	Bank - A	A (Channels 1 - 16)
ZC32 (Connects Banks A - B)	Bank - B	B (Channels 17 - 32)
ZC64 (Connects Banks A - D)	Bank - C	C (Channels 33 - 48)
ZC96 (Connects Banks A - F)	Bank - D	D (Channels 49 - 64)
ZC128 (Connects Banks A - H)	Bank - E	E (Channels 65 - 80)
	Bank - F	F (Channels 81 - 96)
	Bank - G	G (Channels 97 - 112)
	Bank - H	H (Channels 113 - 128)

The diagram below illustrates the connection of a ZC64 ZIF-Clip® headstage to the PZ5. Note that the bank channel numbering matches on both the preamplifier and headstage MiniDB26 connectors.



Headstages to NeuroDigitizer Connection

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier (PZ5, PZ2, RA16PA) is typically lower than the headstage and must be considered the effective range of the system. Also keep in mind that the output range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5V or less. The table below

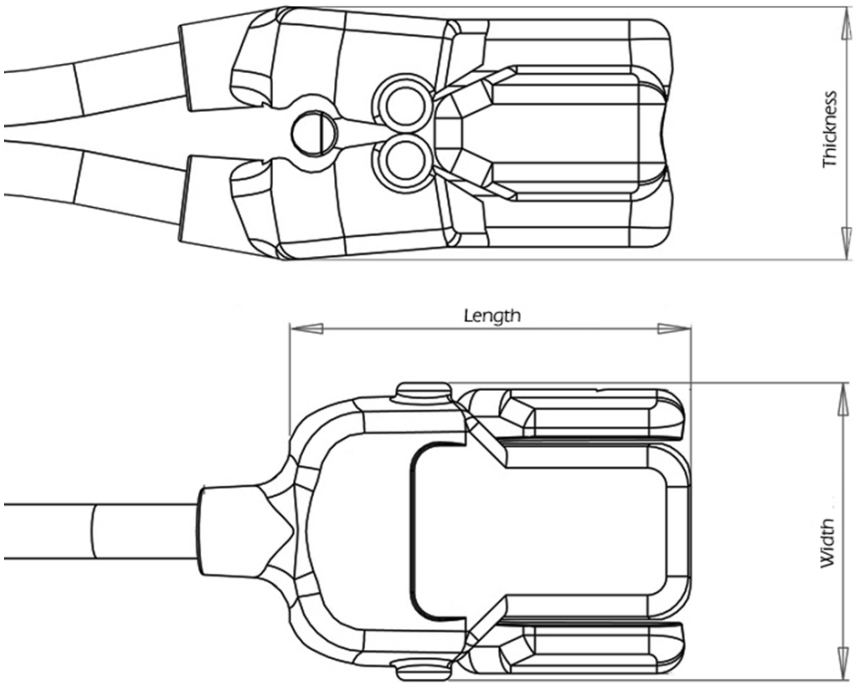
lists the input voltage ranges for the ZIF-Clip® standard headstage for either +/- 1.5V or +/- 2.5V power sources.

	Headstage input range when using +/- 1.5V DC power source	Headstage input range when using +/- 2.5V DC power source
ZIF-Clip® standard headstage	+/- 1.48 V	+/- 2.49 V

ZIF-Clip® ZC Headstages Technical Specifications

Input referred noise	3 µVRMS bandwidth 300-3000 Hz 6 µVRMS bandwidth 30-8000 Hz
Headstage Gain	Unity (1x)
Frequency Response	DC - 25 kHz
Input Impedance	1e14 ohms

Dimensions (Approx.)



Headstage	Length Open	Length Closed	Width	Thickness Open	Thickness Closed	Mass
ZC16/ZC32*	14.401 mm	14.300 mm	10.500 mm	10.255 mm	10.051 mm	2.6 g
ZC64	16.461 mm	16.400 mm	15.500 mm	10.328 mm	10.051 mm	4.8 g
ZC96	17.452 mm	17.400 mm	19.000 mm	10.015 mm	10.051 mm	6.5 g
ZC128	17.948 mm	17.900 mm	25.500 mm	10.212 mm	10.051 mm	9.9 g

* Form factor for both the ZC16 and ZC32 is the same.

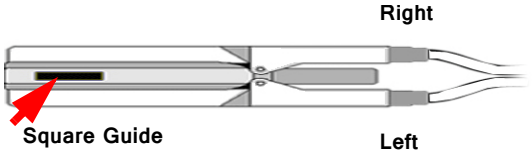
Important! When using multiple headstages, ensure that a single ground is used for all headstages. This will avoid unnecessary noise contamination in recordings. See “Headstage Connection Guide” on page 7-97, for more information.

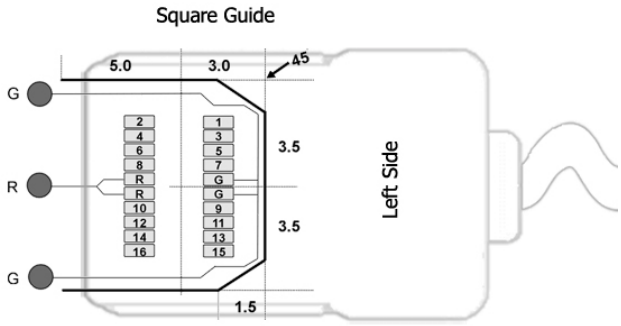
ZIF-Clip® Headstage Pinouts

If you are interested in using a third party electrode see “ZIF-Clip® Headstage Adapters” on page 13-3. If there is no adapter offered for the desired electrode, the following diagrams show the headstage pinouts (channel connections to the amplifier) and board dimensions for connectors to match ZIF-Clip® headstages. A black square guide is used to align the headstage to ZIF-Clip® compatible connectors and can be used in the diagrams below to orient “left” and “right” sides of the headstage shell.

16- and 32-Channel Headstage Pinouts

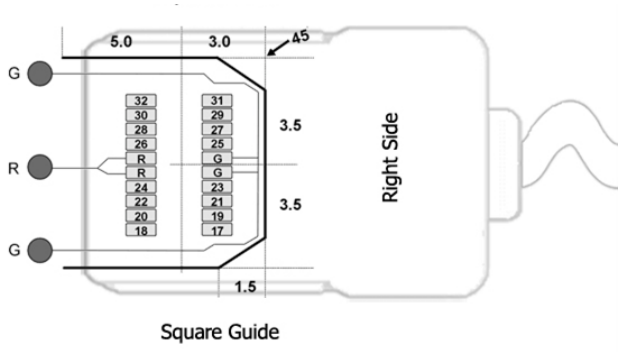
Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.





G Common/Ground Connection

R Reference Connection



Note: The 16-channel ZIF-Clip® headstage does not have any pins connected on the right side of the headstage; the Hirose connector is there for mechanical support. See Hirose specification for recommended footprint.

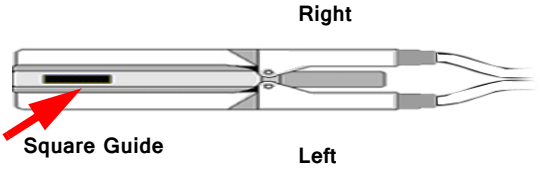
Hirose Connectors:

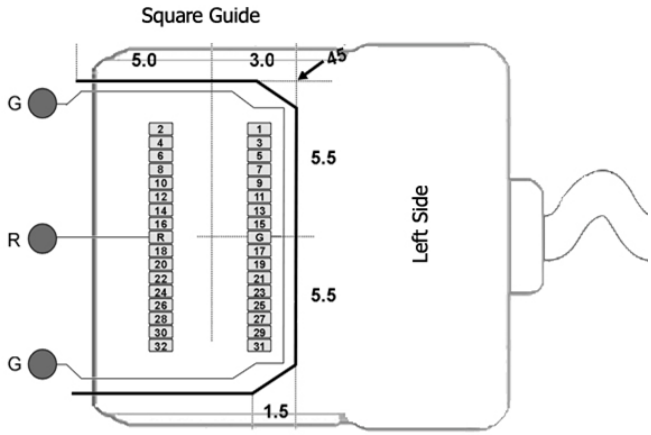
ZC16 - DF30FC-20DS-0.4V x 1

ZC32 - DF30FC-20DS-0.4V x 2

64-Channel Headstage Pinouts

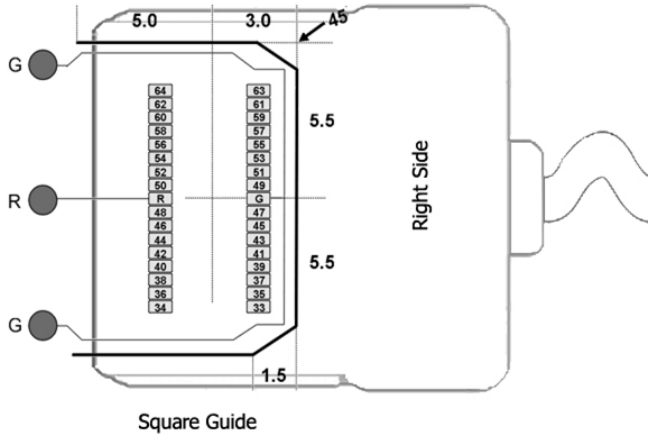
Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.





G Common/Ground Connection

R Reference Connection



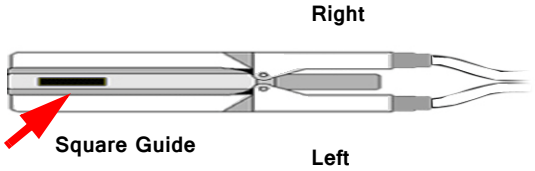
See Hirose specification for recommended footprint.

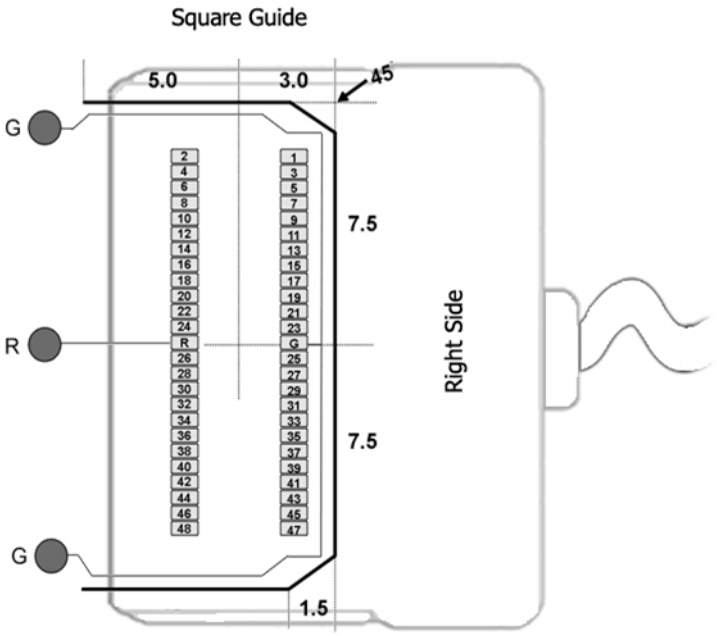
Hirose Connectors:

ZC64 - DF30FC-34DS-0.4V x 2

96-Channel Headstage Pinouts

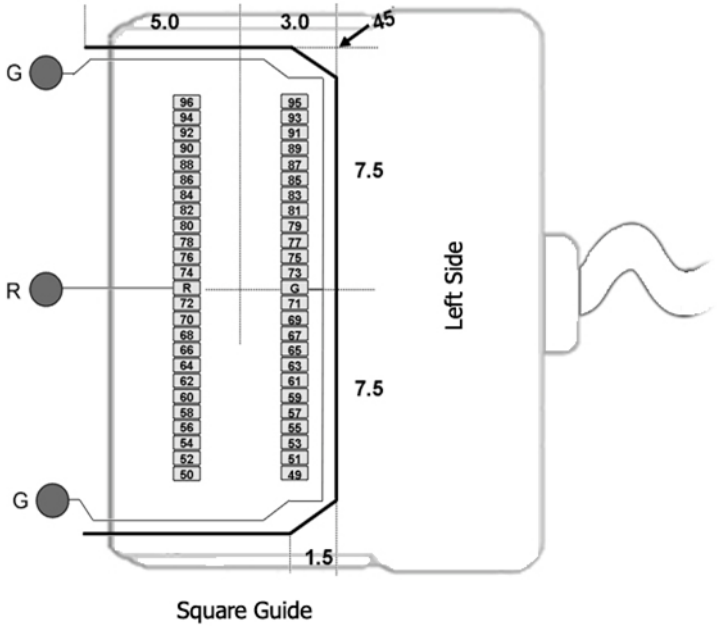
Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.





G Common/Ground Connection

R Reference Connection



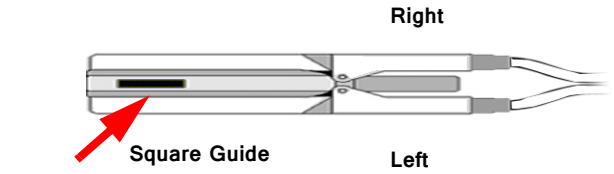
See Hirose specification for recommended footprint.

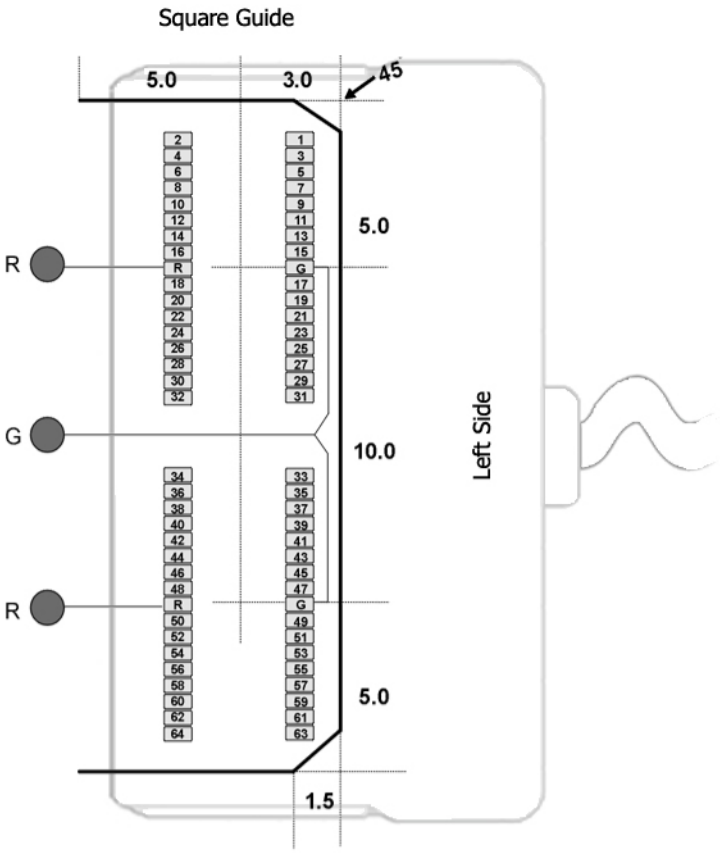
Hirose Connectors:

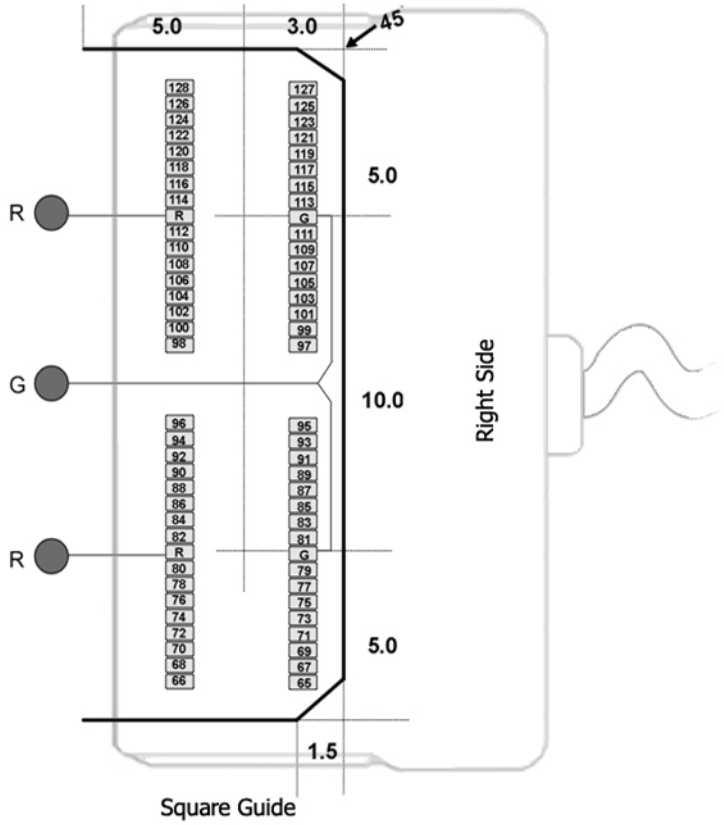
ZC96 - DF30FC-50DS-0.4V x 2

128-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.







G Common/Ground Connection

R Reference Connection

See Hirose specification for recommended footprint.

Hirose Connectors:

ZC128 - DF30FC-34DS-0.4V x 4

ZIF-Clip® ZD Digital Headstages

ZIF-Clip® ZD Overview

ZD ZIF-Clip® digital headstages use Intan RHD2000 amplifier chips to digitize physiological recordings directly inside the headstage. Digitized signals are routed to a PZ5 or Subject Interface (SIM) with a digital input board for transfer to an RZ base station. A single PZ5/SIM digital input board can support up to 128 channels via a direct connection to any of the ZD headstage form factors (32, 64, 96, or 128 channels). The headstage cable is detachable for easy, low-cost replacement.

The ZIF-Clip® headstage (Patent No. 7540752) features an innovative, hinged headstage design that ensures quick, easy headstage connection with almost no insertion force applied to the subject. ZIF-Clip® headstage contacts seat inside the probe array and snap in place, firmly locking the headstage and probe with very little applied pressure. These self-aligning headstages provide long lasting low insertion performance for a variety of channel number and electrode configurations. An aluminum finish provides increased durability.

These headstages are recommended for use with probe that have an impedance in the range of 20 Kohm to 2 Mohm. By default, ground and reference are separate on all ZIF-Clip® headstages yielding a referential configuration. Reference and ground may be tied together on the headstage adapter or ZIF-Clip® microwire array for single-ended configurations.

Part Numbers:

ZD32 32 – channel Digital ZIF-Clip® headstage

ZD64 64 – channel Digital ZIF-Clip® headstage

ZD96 96 – channel Digital ZIF-Clip® headstage

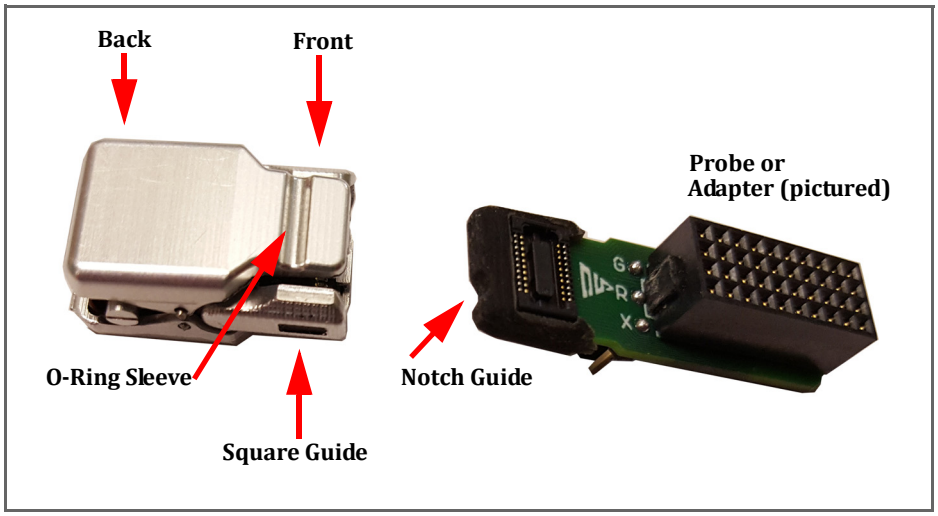
ZD128 128 – channel Digital ZIF-Clip® headstage

ZD-CBL – digital headstage cable

Adapter and Probe Connection

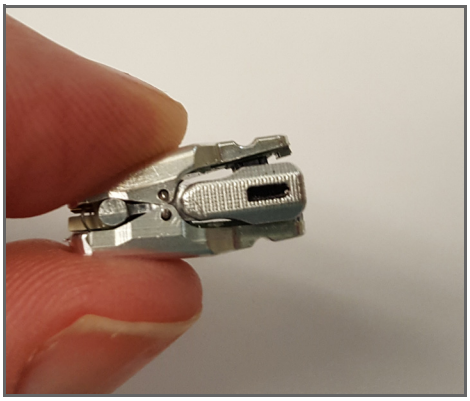
The headstage has sensitive electronics. Always ground yourself before handling.

ZIF-Clip® headstages are designed to automatically position the high density connectors on the headstage and probe (or adapter).

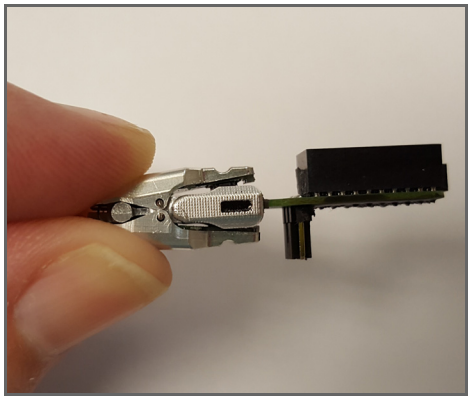


ZIF-Clip® Connection (ZD32 headstage and ZCA-NN32 adapter)

Connect probes and adapters to the headstage as described below.

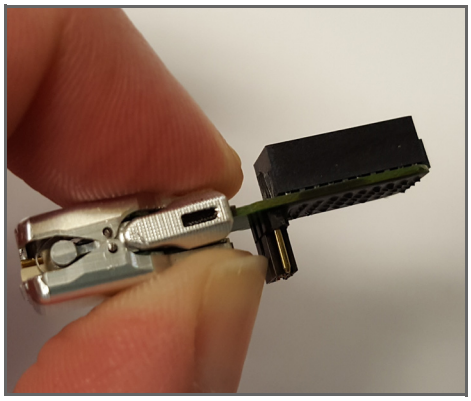


Firmly press and hold the **back** to open the headstage.



Align the **notch guide** of connector to the **black square guide** of the fully opened headstage then move headstage into position.

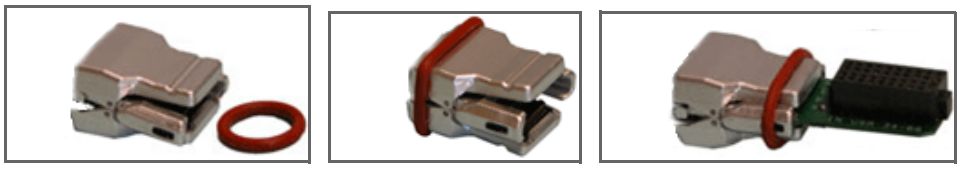
WARNING! The ZIF-Clip® headstage must be held in the fully open position while being slid into position. The headstage should only be closed when fully engaged. Sliding the headstage into position while applying pressure to the tip will **permanently damage** the ZIF-Clip® headstage and micro connectors.



Press the **front** of the headstage together as shown to lock the connector in place. You should hear an audible click when the locking mechanism is engaged.

ZIF-Clip® Headstage O-Rings

All ZIF-Clip® headstages are shipped with two o-rings for additional connection security. Gently slip the o-ring onto the headstage sleeve and then roll the o-ring towards the back of the headstage. Connect the probe or adapter to the headstage as described above. Once the connection is secure, roll the o-ring forward until it settles into the sleeve on the front of the headstage.

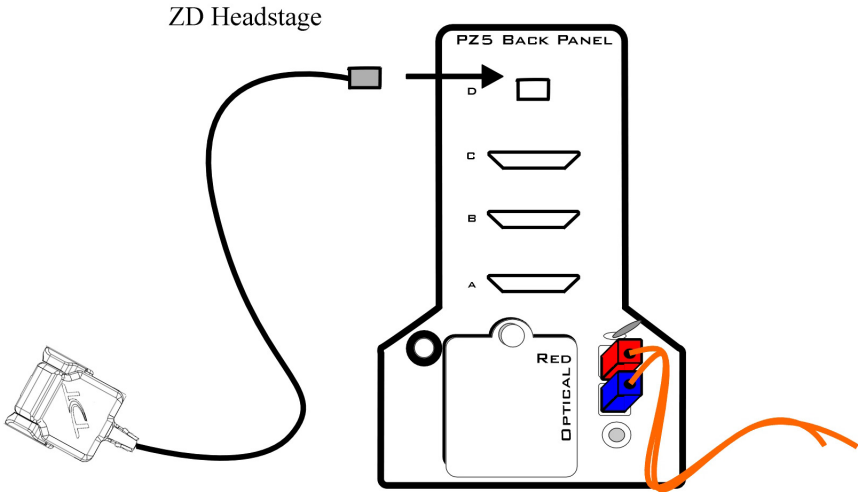


O-Ring Use and Positioning

ZIF-Clip® Digital Headstages PZ5 Connection

The ZD ZIF-Clip® digital headstage uses a single detachable SPI Interface Cable that transmits all channels to a digital input board, housed in a PZ5 neurodigitizer. The PZ5 will automatically detect the number of channels in the headstage. If more

than one headstage is used, all channels will be concatenated together, starting with connector "-A-", to create the output signal to the RZ base station. The total channel count of all connected headstages cannot exceed the maximum channel count for the PZ5. See "PZ5 NeuroDigitizer" on page 7-3, for more information.

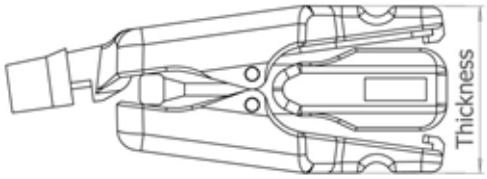


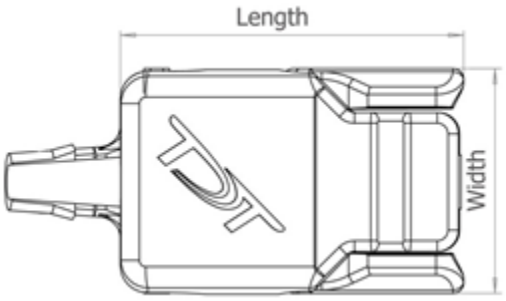
ZIF-Clip® ZD Digital Headstage to Preamplifier Connection Diagram

ZIF-Clip® Digital Headstage Technical Specifications

Input referred noise	2.4 μV_{RMS} Typical. Varies slightly (< 15%) with amplifier bandwidth
Input Impedance	1300 Mohm, 10Hz 13 Mohm, 1kHz TDT recommends using less than 2 Mohm electrodes
A/D	Up to 128 channels, 16-bit successive-approximation
A/D Sample Rate	Up to 24414.0625 Hz
Maximum Voltage In	+/- 5 mV
Frequency Response	3 dB: 0.1 Hz – 10 kHz
Anti-Aliasing Filter	3rd order low-pass (-18 dB per octave)
Distortion (typical)	< 0.8%

Dimensions (Approx.)





Headstage	Length Open	Length Closed	Width	Thickness Open	Thickness Closed
ZD32	16.107 mm	16.050 mm	10.500 mm	8.137 mm	7.400 mm
ZD64	16.446 mm	16.497 mm	15.500 mm	12.760 mm	10.400 mm
ZD96	17.469 mm	17.562 mm	19.000 mm	12.577 mm	10.499 mm

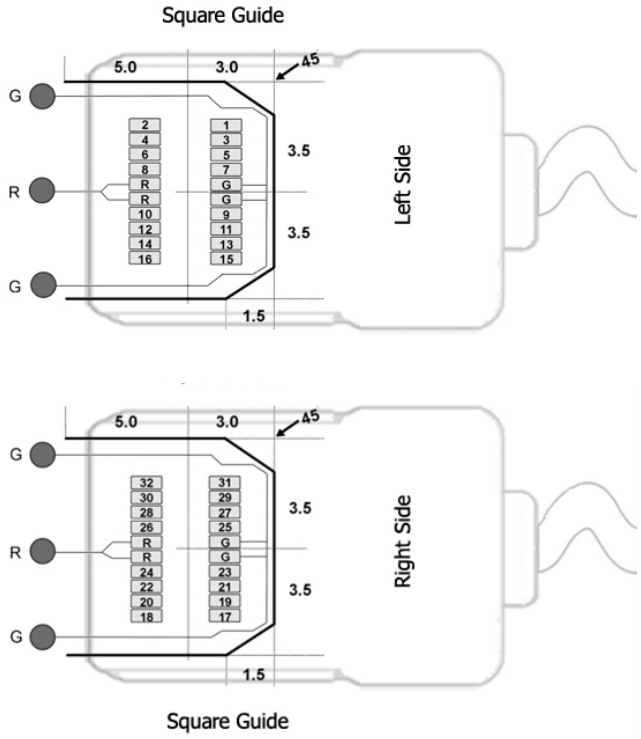
Important! When using multiple headstages, ensure that a single ground is used for all headstages. This will avoid unnecessary noise contamination in recordings. See “Headstage Connection Guide” on page 7-97, for more information.

ZIF-Clip® Headstage Pinouts

If you are interested in using a third party electrode see "ZIF-Clip® Headstage Adapters" on page 13-3. If there is no adapter offered for the desired electrode, the following diagrams show the headstage pinouts (channel connections to the amplifier) and board dimensions for connectors to match ZIF-Clip® headstages. A black square guide is used to align the headstage to ZIF-Clip® compatible connectors and can be used in the diagrams below to orient "left" and "right" sides of the headstage shell.

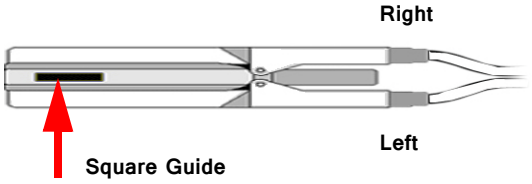
16- and 32-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.



G Common/Ground Connection

R Reference Connection



Note: The 16-channel ZIF-Clip® headstage does not have any pins connected on the right side of the headstage; the Hirose connector is there for mechanical support. See Hirose specification for recommended footprint.

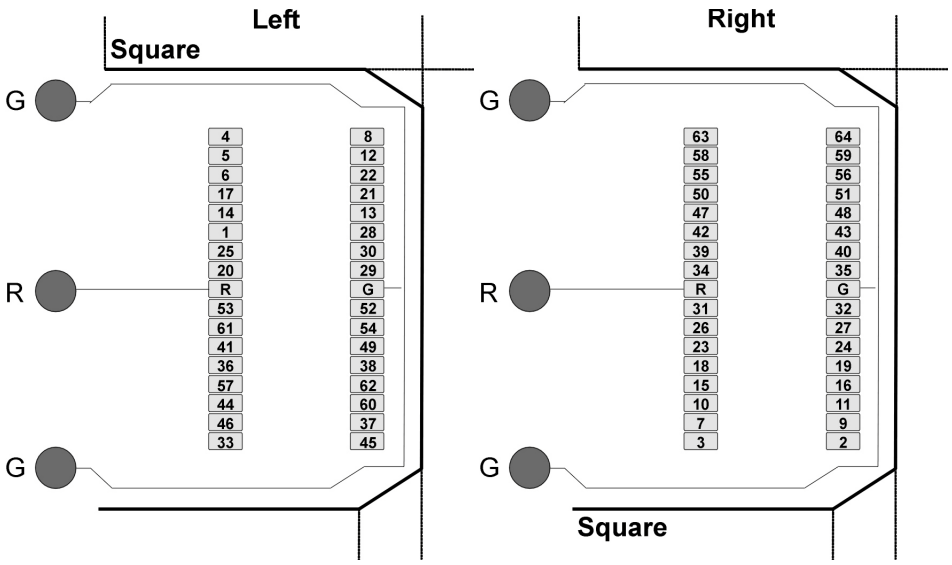
Hirose Connectors:

ZD16 - DF30FC-20DS-0.4V x 1

ZD32 - DF30FC-20DS-0.4V x 2

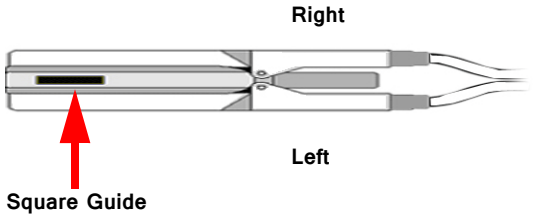
64-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.



G Common/Ground Connection

R Reference Connection



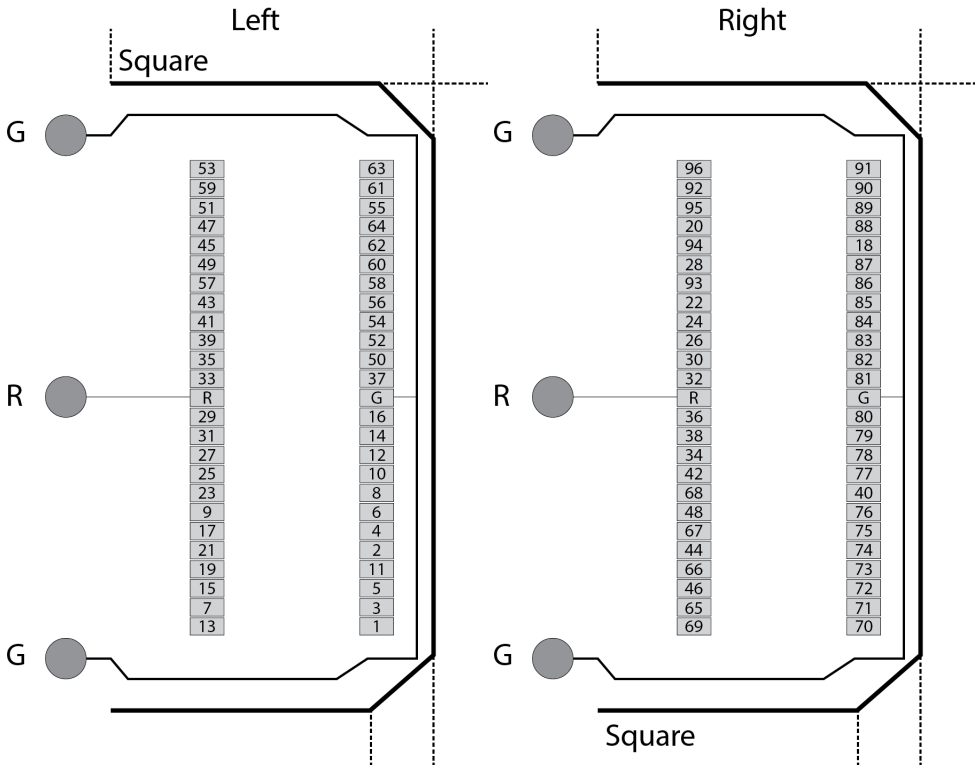
See Hirose specification for recommended footprint.

Hirose Connectors:

ZD64 - DF30FC-34DS-0.4V x 2

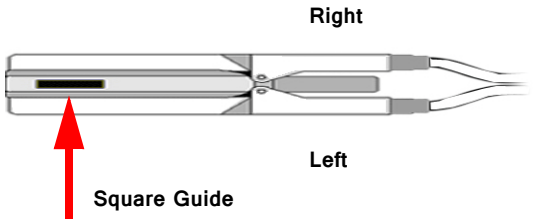
96-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.



G Common/Ground Connection

R Reference Connection



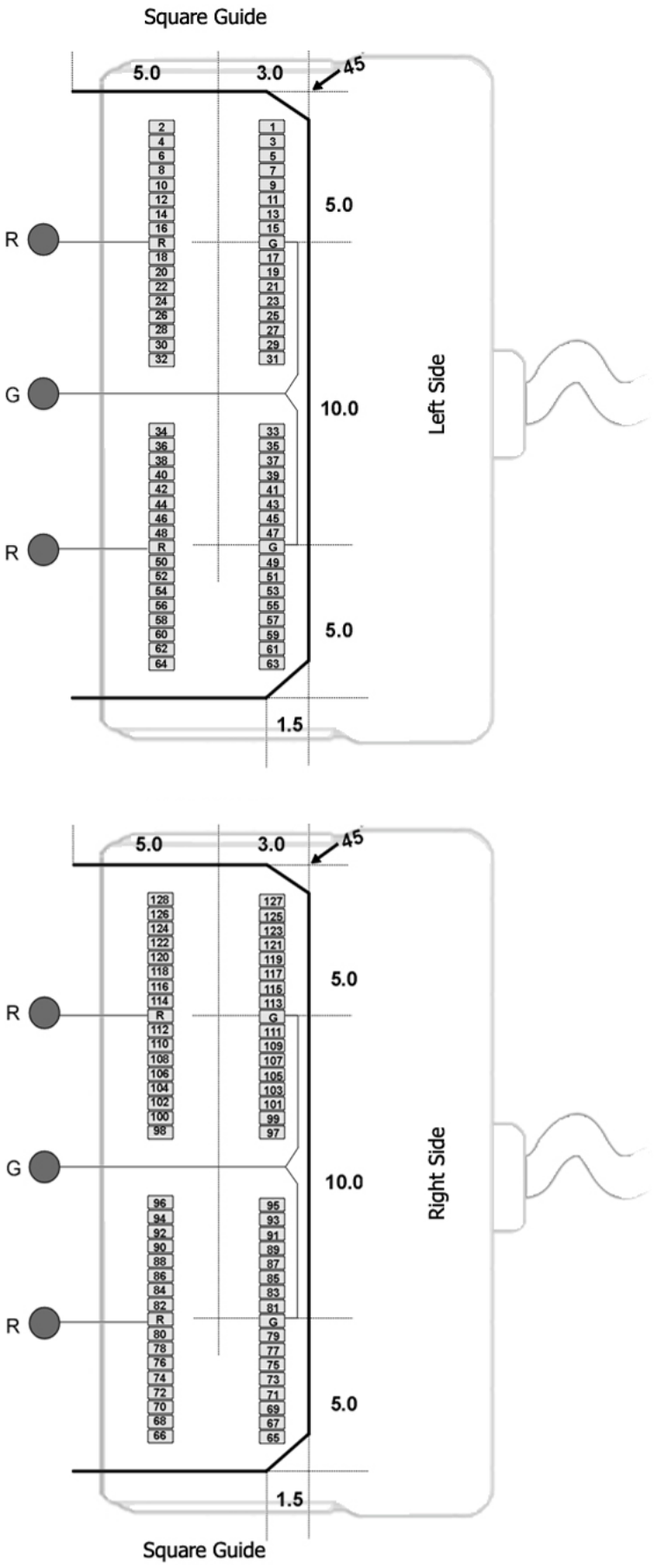
See Hirose specification for recommended footprint.

Hirose Connectors:

ZD96 - DF30FC-50DS-0.4V x 2

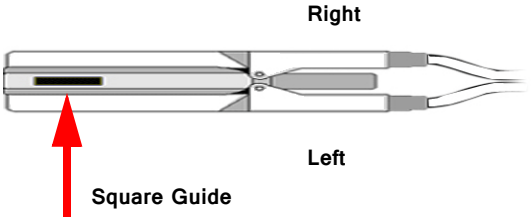
128-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.

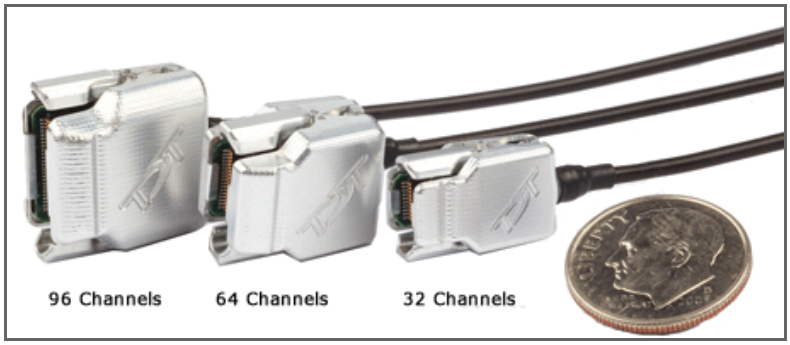

Square Guide
5.0
3.0
45
5.0
10.0
5.0
1.5
R
G
R
Left Side
Right Side
Square Guide

G Common/Ground Connection

R Reference Connection



ZIF-Clip® ZCD Digital Headstages



ZCD Digital Headstages

ZIF-Clip® ZCD Overview

ZIF-Clip® digital headstages use an Intan amplifier chip to digitize physiological recordings directly inside the clip. Digitized signals are routed to a PZ4 headstage manifold through a single cable for transfer to an RZ base station.

The ZIF-Clip® headstage (Patent No. 7540752) features an innovative, hinged headstage design that ensures quick, easy headstage connection with almost no insertion force applied to the subject. ZIF-Clip® headstage contacts seat inside the probe array and snap in place, firmly locking the headstage and probe with very little applied pressure. These self-aligning headstages provide long lasting low insertion performance for a variety of channel number and electrode configurations. An aluminum finish provides increased durability.

The headstages are recommended for use with probe impedance that range from 20 Kohm to 2 Mohm. By default, ground and reference are separate on all ZIF-Clip® headstages yielding a referential configuration. Reference and ground may be tied together on the headstage adapter or ZIF-Clip® microwire array for single-ended configurations.

Part Numbers:

ZCD32 – 32-channel Digital ZIF-Clip® headstage

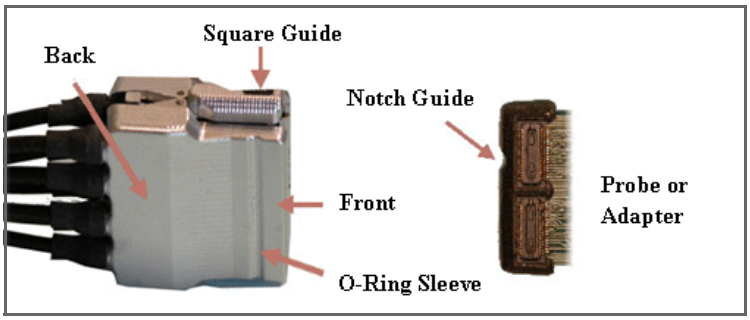
ZCD64 – 64-channel Digital ZIF-Clip® headstage

ZCD96 – 96-channel Digital ZIF-Clip® headstage

Adapter and Probe Connection

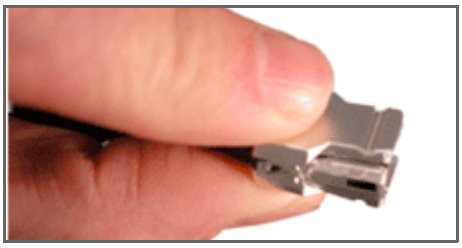
The headstage has sensitive electronics. Always ground yourself before handling.

ZIF-Clip® headstages are designed to automatically position the high density connectors on the headstage and probe (or adapter).

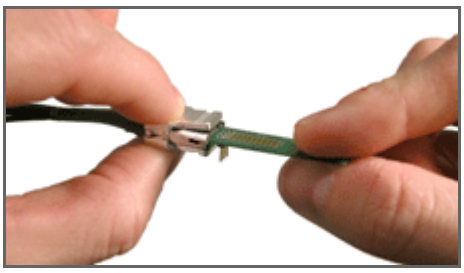


ZIF-Clip® Connection (Analog Headstage Pictured)

Connect probes and adapters to the headstage as described below.

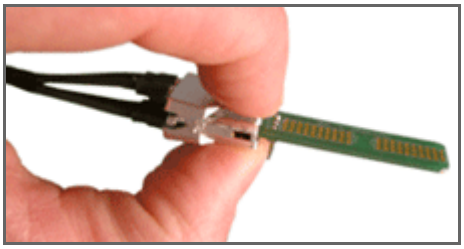


Firmly press and hold the **back** to open the headstage.



Align the **notch guide** of connector to the **black square guide** of the fully opened headstage then move headstage into position.

WARNING! The ZIF-Clip® headstage must be held in the fully open position while being slid into position. The headstage should only be closed when fully engaged. Sliding the headstage into position while applying pressure to the tip will **permanently damage** the ZIF-Clip® headstage and micro connectors.



Press the **front** of the headstage together as shown to lock the connector in place. You should hear an audible click when the locking mechanism is engaged.

ZIF-Clip® Headstage O-Rings

All ZIF-Clip® headstages are shipped with two o-rings for additional connection security. Gently slip the o-ring onto the headstage sleeve and then roll the o-ring towards the back of the headstage. Connect the probe or adapter to the headstage as described above. Once the connection is secure, roll the o-ring forward until it settles into the sleeve on the front of the headstage.

O-Ring Use and Positioning

ZIF-Clip® Digital Headstage Manifold Connection

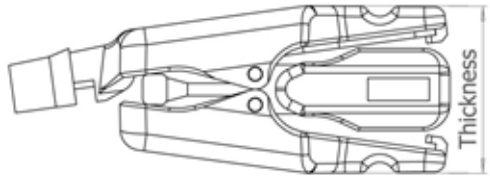
The ZIF-Clip® digital headstage has one MiniDB26 connector that transmits all channels for that headstage. Up to four ZIF-Clip® digital headstages can be connected to a PZ4 Digital Headstage Manifold. The PZ4 will automatically detect the number of channels in each headstage. All channels will be concatenated together, starting with connector "-A-", to create the output signal to the RZ base station. The total channel count of all connected headstages cannot exceed the maximum channel count for the PZ4. See "PZ4 Digital Headstage Manifold" on page 7-77, for more information.

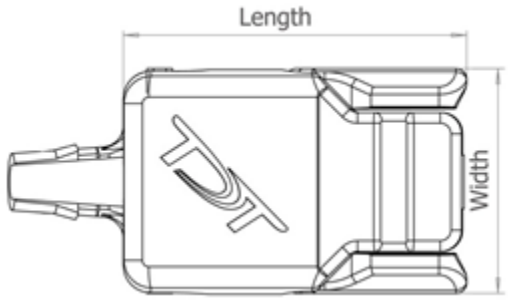
ZIF-Clip® ZCD Digital Headstage Technical Specifications

Input referred noise	4 μV_{RMS} bandwidth 300-3000 Hz 7 μV_{RMS} bandwidth 30-8000 Hz
Headstage Gain	Unity (1x)
Input Impedance	1300 Mohm, 10Hz 13 Mohm, 1kHz TDT recommends using less than 2 Mohm electrodes
A/D	Up to 96 channels, 16-bit PCM
A/D Sample Rate	Up to 24414.0625 Hz
Maximum Voltage In	+/- 5 mV
Frequency Response	0.3 Hz to 7.5 kHz(3dB)

Anti-Aliasing Filter	3rd order low-pass (-18 dB per octave)
Distortion (typical)	< 1%
Channel Cross Talk	-75 dB

Dimensions (Approx.)





Headstage	Length Open	Length Closed	Width	Thickness Open	Thickness Closed
ZCD32	16.107 mm	16.050 mm	10.500 mm	8.137 mm	7.400 mm
ZCD64	16.446 mm	16.497 mm	15.500 mm	12.760 mm	10.400 mm
ZCD96	17.469 mm	17.562 mm	19.000 mm	12.577 mm	10.499 mm

Important! When using multiple headstages, ensure that a single ground is used for all headstages. This will avoid unnecessary noise contamination in recordings. See "Headstage Connection Guide" on page 7-97, for more information.

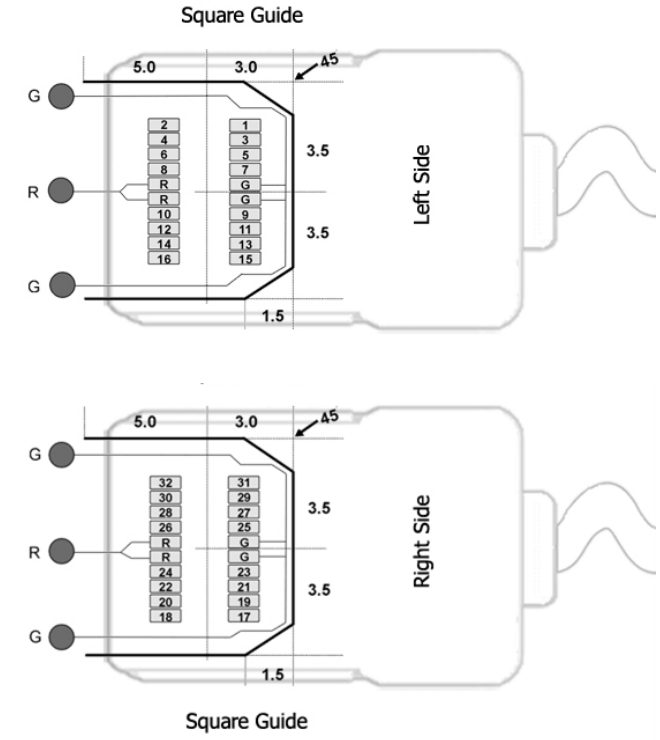
ZIF-Clip® Headstage Pinouts

If you are interested in using a third party electrode see "ZIF-Clip® Headstage Adapters" on page 13-3. If there is no adapter offered for the desired electrode, the following diagrams show the headstage pinouts (channel connections to the amplifier) and board dimensions for connectors to match ZIF-Clip® headstages. A black square guide is used to align the headstage to ZIF-Clip® compatible connectors and can be used in the diagrams below to orient "left" and "right" sides of the headstage shell.

Channel numbers are relative to the manifold connection to which they are connected.

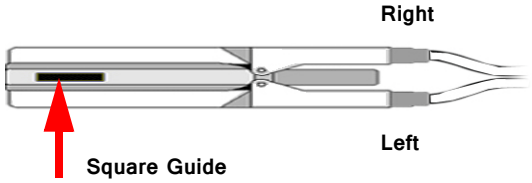
16- and 32-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.



G Common/Ground Connection

R Reference Connection



Note: The 16-channel headstage does not have any pins connected on the right side of the headstage; the Hirose connector is there for mechanical support. See Hirose specification for recommended footprint.

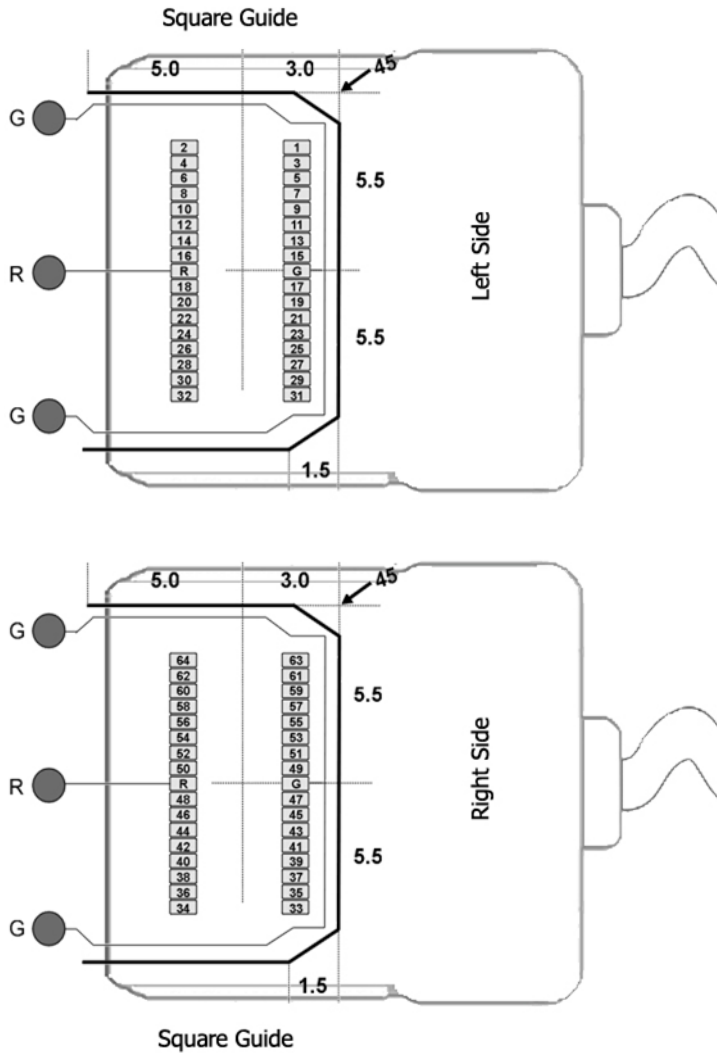
Hirose Connectors:

ZCD16 - DF30FC-20DS-0.4V x 1

ZCD32 - DF30FC-20DS-0.4V x 2

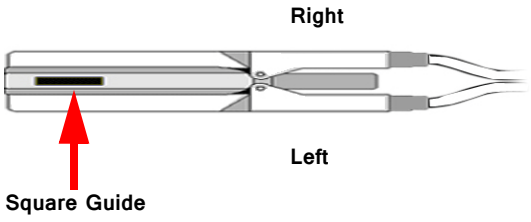
64-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.



G Common/Ground Connection

R Reference Connection



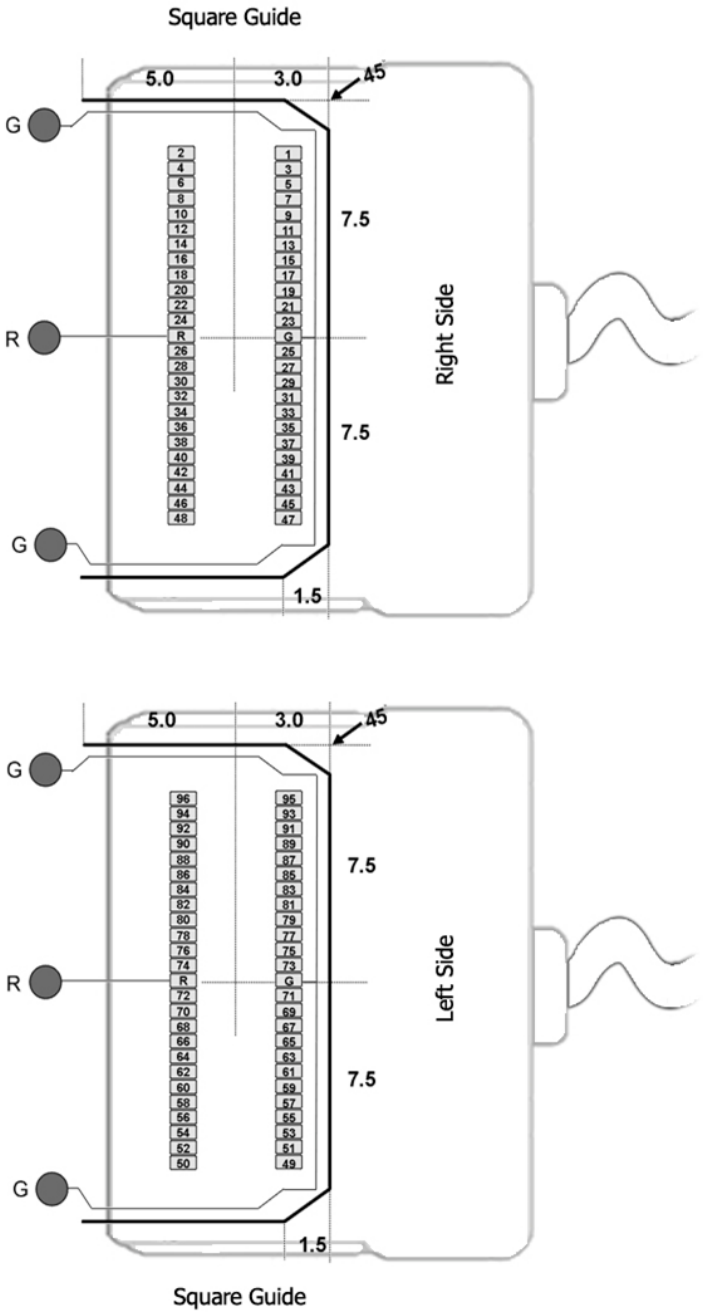
See Hirose specification for recommended footprint.

Hirose Connectors:

ZCD64 - DF30FC-34DS-0.4V x 2

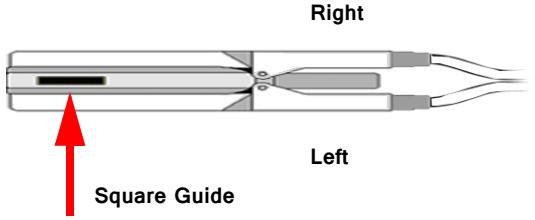
96-Channel Headstage Pinouts

Images are not to scale. Pinouts are looking through the headstage shell (or into a matching board connector). All board dimensions are in millimeters and are identical for both sides, board thickness is 0.75 mm, and connectors are centered as shown.



G Common/Ground Connection

R Reference Connection



See Hirose specification for recommended footprint.

Hirose Connectors:

ZCD96 - DF30FC-50DS-0.4V x 2

ZIF-Clip® Headstage Holders

The ZIF-Clip® headstage holders securely hold your analog or digital ZIF-Clip headstages during electrode insertion and can be used with most micromanipulators. The headstage holders, including the stabilizing rod, are approximately 4.5" in length. The stabilizing rod is 3" in length and has a 3/32" diameter. An aluminum lock pin ensures the ZIF-Clip does not open during insertion.

Each holder is designed for use with the corresponding ZIF-Clip® or Digital ZIF-Clip® headstage.

Part Numbers:

Z-ROD32 16 or 32-channel analog ZIF-Clip® headstage holder (for ZC32)

Z-ROD64 64-channel analog ZIF-Clip® headstage holder (for ZC64 and ZD64)

Z-ROD96 96-channel analog ZIF-Clip® headstage holder (for ZC96 and ZD96)

Z-ROD128 128-channel analog ZIF-Clip® headstage holder (for ZC128)

ZCD-ROD32 32-channel digital ZIF-Clip® headstage holder (for ZCD32 and ZD32)

ZCD-ROD64 64-channel digital ZIF-Clip® headstage holder (for ZCD64)

ZCD-ROD96 96-channel digital ZIF-Clip® headstage holder (for ZCD96)

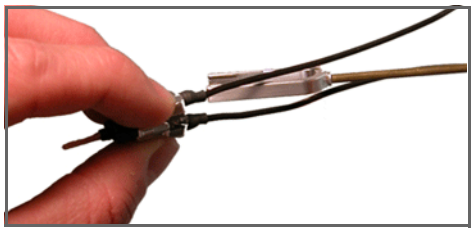
Using the Holder with ZIF-Clip® Headstages

Each holder is sized to fit a particular headstage and with the exception of the ZCD-ROD32 (see below), they all can be fitted to the headstage in the same way.

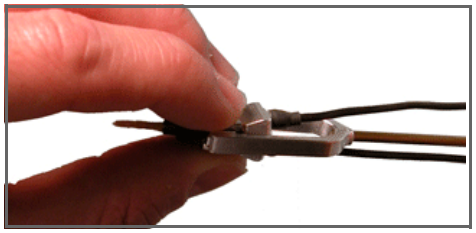
First, connect the probe or adapter to your ZIF-Clip® headstage BEFORE putting the headstage in the holder (the square guide provided to ensure the probe or adapter is connected with the correct polarity is hidden from view when the headstage is in the holder). See the "Adapter and Probe Connection" section on "ZIF-Clip® Headstage Adapters" on page 13-3, for more information.

Next, gently slide the ZIF-Clip® headstage onto the holder until it is completely secure as shown in the images below.

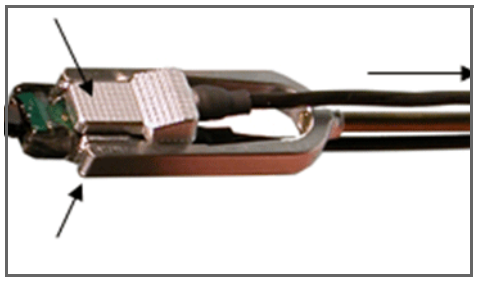
Finally, secure the lock pin to the headstage holder.



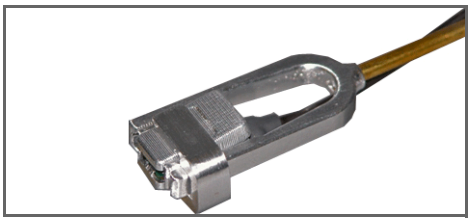
Gently slide the headstage onto the holder (with probe or adapter already connected).



Position the headstage holder between the cables of the ZIF-Clip® headstage. The headstage should be completely secured in the holder.



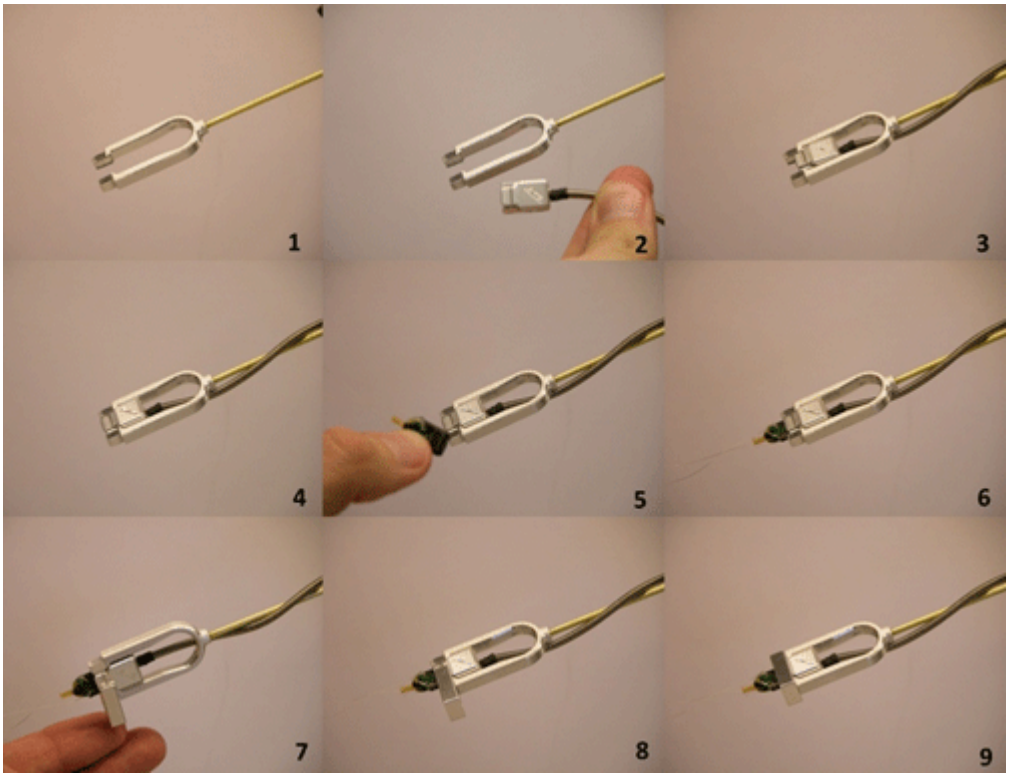
To remove, grip the top and bottom of the headstage and gently slide the holder away.



The U-shaped lock pin secures the connection and prevents the ZIF-Clip® from opening and releasing the probe.

Using the ZCD-ROD32

The ZCD-ROD32 has a unique design that requires a different insertion procedure.



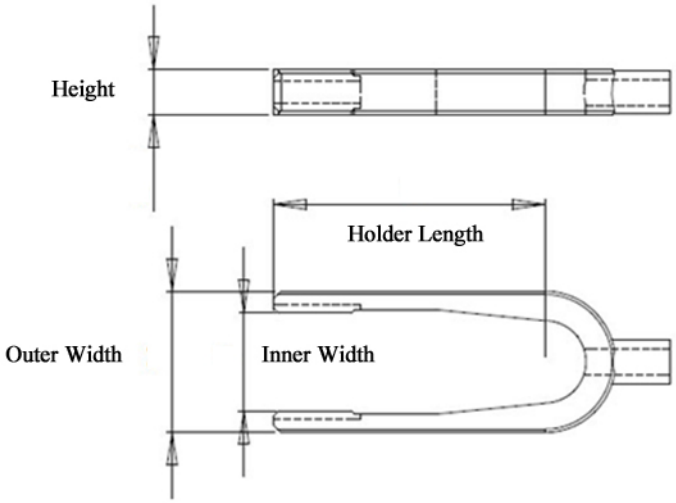
To use the headstage holder:

1. Set the ZCD32 headstage inside the base (or U) of the holder and slide it forward until it is stopped by the interior flange (Image 1-4).
2. After the clip is in place, insert the probe (Image 5-6) and then slide the provided lock pin over the ZCD32 (Image 7-9).

The lock pin prevents the clip from opening and releasing the probe, and also from sliding backward during insertion.

The lock pin has small ridges that should be aligned with the grooves on the face of the clip. If you have trouble connecting the lock pin, make sure that the clip has been pushed in completely and that the ridges and grooves are properly aligned (Image 7).

Holder Dimensions



Z-ROD Dimensions (for analog and digital headstages)

Form Factor	16/32-channel ZC16 / ZC32	64-channel ZC64 / ZD64	96-channel ZC96 / ZD96	128-channel ZC128
Height	4.10 mm (9.62 mm with lock pin)			
Inner Width	9 mm	14 mm	17.50 mm	24 mm
Outer Width	13 mm (16 mm with lock pin)	18 mm	21.50 mm	28 mm
Holder Length	25 mm	28 mm	28 mm	28 mm
Rod Length	stabilizing rod is 76.2 mm with a 2.29 mm diameter			

ZCD-ROD Dimensions (for digital headstages)

Form Factor	32-channel ZCD32 / ZD32	64-channel ZCD64	96-channel ZCD96
Height	5.5 mm (11.50 mm with lock pin)	4.10 mm (15.30 mm with lock pin)	4.10 mm
Inner Width	11.10 mm	14.39 mm	17.50 mm
Outer Width	18.50 mm (18.50 mm with lock pin)	17.79 mm (21.5 mm with lock pin)	21.50 mm
Holder Length	31.50 mm	25.36 mm	25.36 mm
Rod Length	stabilizing rod is 76.2 mm with a 2.29 mm diameter		

Acute (Non-ZIF) Headstages

NN64AC 64-Channel Acute Headstage

The 16 Channel acute The 64 Channel Acute headstage is recommended for extracellular neurophysiology using silicon electrodes, metal microelectrodes or microwire arrays with input impedance from 20 kOhm to 5 Mohm.

The headstage features two 40-pin connectors designed for use with NeuroNexus Acute 64-channel probes. The headstage connects to a PZ series preamplifier via four mini 26-pin connectors or with System 3 Medusa preamplifiers (such as four RA16PAs) via four DB25 connectors. In either case, each connector carries the signals for 16 channels, power and ground. Therefore, each connector can be connected independently. The connector labeled Bank-1 carries channels 1-16, Bank-2 carries 17-32, etc.

Part Numbers:

NN64AC—64 Channel Acute Headstage for Medusa PreAmps

NN64AC-Z—64 Channel Acute Headstage for Z-Series (PZ) PreAmps

The headstage has sensitive electronics. Always ground yourself before handling.

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

The table below lists the input voltage ranges for the NN64AC and NN64AC-Z headstages for either a +/- 1.5 V or +/- 2.5 V power source.

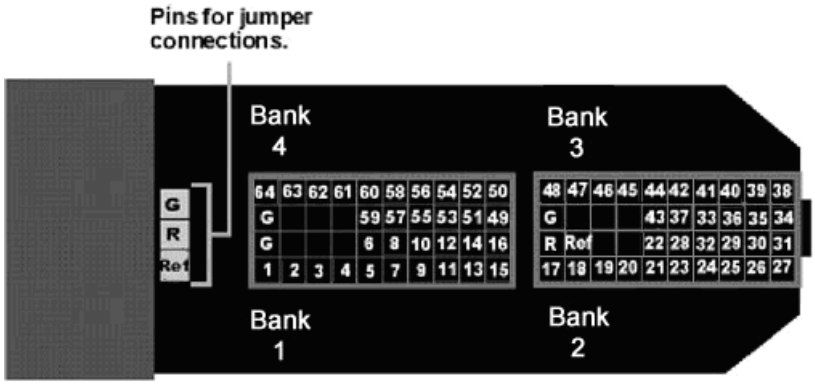
Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
+/- 0.9 V	+/- 1.9 V

Technical Specifications

WARNING! When using multiple headstages ensure that all ground pins are connected to a single common node. See "Headstage Connection Guide" on page 7-97, for more information.

Input Referred Noise	rms 3 µV bandwidth 300-3000 Hz rms 6 µV bandwidth 30-8000 Hz
Headstage Gain	Unity (1x)
Input Impedance	10^{14} Ohms

Pinout Diagram



(looking into connections)

The numbers in the diagram above show the channel connections to the amplifier. The headstage also features jumper locations to short G, R and Ref refers to the built-in reference site on the NeuroNexus probe). The ground channel (G) should either be tied to an external ground or to the reference (R) for a single ended input.

Important! When using the NN64AC with the NeuroNexus Acute 64-channel probe, keep in mind that there are several versions of the probe. Check the NeuroNexus Website for pin diagrams. Also, see "MCMap" in the *RPvdsEx Manual*, for a description and examples on how to re-map channel numbers.

Jumper Configuration

The following table describes the jumper configurations and associated requirements.

Jumper Connections	Operation	Requirements
G R Ref	Shorts headstage Ground and Reference inputs together, yielding single-ended amplification of signals relative to ground.	Connect common Ground/Reference wire to the headstage or electrode.

Jumper Connections	Operation	Requirements
G R Ref	Shorts headstage Reference input to the pin labeled Ref (a low impedance site on the probe) yielding referential amplification of signals relative to the voltage of the Ref site.	Connect Ground wire to the headstage or electrode.
G R Ref	Headstage Ground and Reference separated and Ref pin is not used, yielding referential amplification of signals relative to the voltage of the Reference.	Connect both a Ground wire and a Reference wire to the headstage or electrode.

NN32AC - 32 Channel Acute Headstage

The 32 Channel Acute headstage is recommended for extracellular neurophysiology using silicon electrodes, metal microelectrodes or microwire arrays with input impedance from 20 kOhm to 5 Mohm. The headstage features a 40-pin connector designed for use with the NeuroNexus Acute 32-channel probe. The headstage connects to a PZ series preamplifier via two mini 26-pin connectors or to two RA16PA preamplifiers via two 25-pin connectors. For either headstage, Connector A carries the signals for channels 1-16, power and ground. This connector must be connected whether you are acquiring data from one of these channels or not.

Part Numbers:

NN32AC—32 Channel Acute Headstage for Medusa PreAmps

NN32AC-Z—32 Channel Acute Headstage for Z-Series (PZ) PreAmps

The headstage has sensitive electronics. Always ground yourself before handling.

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

The table below lists the input voltage ranges for the NN32AC and NN32AC-Z for either a +/- 1.5 V or +/- 2.5 V power source.

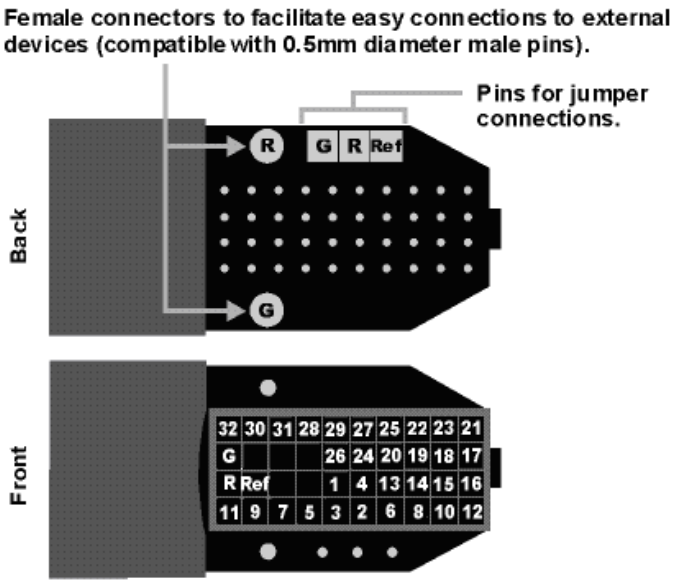
Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
+/- 0.9 V	+/- 1.9 V

Technical Specifications

WARNING! When using multiple headstages ensure that all ground pins are connected to a single common node. See "Headstage Connection Guide" on page 7-97, for more information.

Input Referred Noise	rms 3 µV bandwidth 300-3000 Hz rms 6 µV bandwidth 30-8000 Hz
Headstage Gain	Unity (1x)
Input Impedance	10^{14} Ohms

Pinout Diagram



(looking into connections)

Important! When using the NN32AC with the NeuroNexus Acute 32-channel probe, keep in mind that there are several versions of the probe and the NN32AC was designed to correspond to the NeuroNexus rev 3 probe. Check the NeuroNexus Website for pin diagrams. Also, see "MCMap" in the *RPvdsEx Manual*, for a description and examples on how to re-map channel numbers.

The numbers in the diagram above show the channel connections to the amplifier.

The surfaced connections on the back of the headstage include female connectors to simplify connections to external devices and jumper locations to short G, R and Ref refers to the built-in reference site on the NeuroNexus probe). The ground channel(G) should either be tied to an external ground or to the reference (R) for a single ended input.

Jumper Configuration

The following table describes the jumper configurations and associated requirements.

Jumper Connections	Operation	Requirements
G R Ref	Shorts headstage Ground and Reference inputs together, yielding single-ended amplification of signals relative to ground.	Connect common Ground/Reference wire to the headstage or electrode.
G R Ref	Shorts headstage Reference input to the pin labeled Ref (a low impedance site on the probe) yielding referential amplification of signals relative to the voltage of the Ref site.	Connect Ground wire to the headstage or electrode.
G R Ref	Headstage Ground and Reference separated and Ref pin is not used, yielding referential amplification of signals relative to the voltage of the Reference.	Connect both a Ground wire and a Reference wire to the headstage or electrode.

RA16AC - 16 Channel Acute Headstage

The 16 Channel acute headstages is recommended for extracellular neurophysiology using silicon electrodes, metal microelectrodes or microwire arrays with recommended input impedance from 20 kOhm to 5 Mohm unless otherwise noted.

The 16 channel acute headstage has an 18-pin DIP connector that can be used with standard high impedance metal electrodes. The pinout of the RA16AC matches the wiring of NeuroNexus electrodes to allow for direct connection to the headstage. TDT recommends connecting electrodes to an 18-pin socket and then connecting the socket to the headstage to protect the headstage from unnecessary wear and tear. The RA16AC4 provides 4x gain and is used with electrodes with a recommended impedance range of 20 kOhm to 300 kOhm.

The headstage connects to a System 3 Medusa preamplifier (such as the RA16PA) via a DB25 connector or to a PZ series preamplifier via a mini 26-pin connector.

Part Numbers:

RA16AC—16 Channel Acute Headstage for Medusa PreAmps, with unity (1x) gain

RA16AC4—16 Channel Acute Headstage for Medusa PreAmps, with 4x gain

RA16AC-Z—16 Channel Acute Headstage for Z-Series (PZ) PreAmps, with unity (1x) gain


The headstage has sensitive electronics. Always ground yourself before handling.

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range

of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

The table below lists the input voltage ranges for RA16AC headstages for either a +/- 1.5 V or +/- 2.5 V power source.

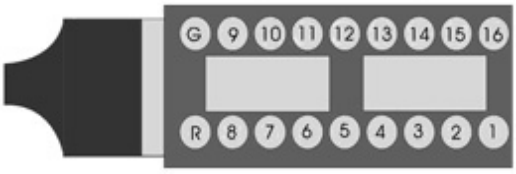
	Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
RA16AC4	+/- 0.37 V	+/- 0.62 V
RA16AC	+/- 0.9 V	+/- 1.9 V

Technical Specifications

Warning! When using multiple headstages ensure that all ground pins are connected to a single common node. See "Headstage Connection Guide" on page 7-97, for more information.

Input referred noise	rms 3 µV bandwidth 300-3000 Hz rms 6 µV bandwidth 30-8000 Hz
Headstage Gain	RA16AC - Unity (1x) RA16AC4 - 4x RA16AC-Z - Unity (1x)
Input Impedance	10^{14} Ohms

Pinout Diagram



(looking into connections)

The numbers in the diagram above show the channel connections to the amplifier. The electrode connector accepts 0.5 mm diameter male pins.

For pinouts for the preamplifier connector, see the corresponding preamplifier.

RA4AC - 4 Channel Acute Headstage

The 4 Channel Acute headstages are recommended for extracellular neurophysiology using silicon electrodes, metal microelectrodes, or microwire arrays with input impedance from 20 kOhm to 5 MOhm.

The RA4AC1 and RA4AC4 headstages have a low-profile 6-pin connector. The RA4AC1 provides unity gain (1x). The RA4AC4 provides 4x gain and is used with electrodes with a recommended impedance range of 20 kOhm to 300 kOhm. The 25-pin connector connects to the RA4PA 4-channel Medusa preamplifier.

Part Numbers:

RA4AC1—4 Channel Acute Headstage for Medusa PreAmps, with unity (1x) gain

RA4AC4—4 Channel Acute Headstage for Medusa PreAmps, with 4x gain

The headstage has sensitive electronics. Always ground yourself before handling.

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

The table below lists the input voltage ranges for the RA4AC and RA4AC4 headstages for either a +/- 1.5 V or +/- 2.5 V power source.

	Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
RA4AC4	+/- 0.37 V	+/- 0.62 V
RA4AC	+/- 0.9 V	+/- 1.9 V

Technical Specifications

WARNING! When using multiple headstages ensure that all ground pins are connected to a single common node. See "Headstage Connection Guide" on page 7-97, for more information.

Input Referred Noise	3 µVrms bandwidth 300-3000 Hz 6 µVrms bandwidth 30-8000 Hz
Headstage Gain	RA4AC1 - Unity (1x) RA4AC4 - 4x
Input Impedance	10^{14} Ohms

Pinout Diagram

The numbers in the above diagram show the channel connections to the amplifier. The electrode connector accepts 0.76 mm diameter male pins.

The RA4AC1/RA4AC4 is also provided with a 6-pin male connector with flying leads. When connecting to the headstage, note that the silver dots marking channel 1 line up.

Channel 1 marked with a dot on probe head

(looking into connections)

The colors of the lead wires correspond to the headstage channels as follows:

Color	Channel
Black	1
Red	2
Orange	3
Yellow	4
Blue	Reference
Green	Ground

Chronic (Non-ZIF) Headstages

LP32CH-Z - 32 Channel Chronic Headstage

The 32 channel chronic headstage is recommended for extracellular neurophysiology using silicon electrodes, metal microelectrodes or microwire arrays with input impedance from 20 kOhm to 5 MOhm. The headstage uses a female Omnetics connector to mate with chronic electrodes.

The LP32CH-Z uses an Omnetics 36 socket female dual row nano connector (0.025"/0.64mm) with 4 guide posts. The LP32CH-ZNF uses non-ferrous materials, including a non-ferrous female Omnetics connector with the same size and pinout as the LF32CH. It can be used for recording single-unit electrophysiology during fMRI neuroimaging.

Part Numbers:

LP32CH-Z: 32-Channel Chronic Low Profile Headstage for Z-Series (PZ) PreAmps

LP32CH-ZNF: 32-Channel Non-Ferrous, Chronic Low Profile Headstage for Z-Series (PZ) Preamps

The headstages have sensitive electronics. Always ground yourself before handling.

Headstage Voltage Range

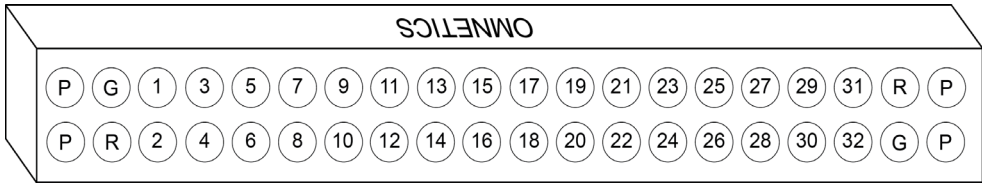
When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

	Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
LP32CH, LP32CH-Z, LP32CH-ZNF	+/- 1.48 V	+/- 2.49 V

Technical Specifications

Input Referred Noise	rms 3 µV bandwidth 300-3000 Hz rms 6 µV bandwidth 30-8000 Hz
Headstage Gain	Unity (1x)
Input Impedance	10^{14} Ohms
Connector	Omnetics 36 socket female dual row nano connector (.025"/.64mm) with 4 guide posts

Pinout



P=Guide Pins R=Reference G=Ground
Looking into connector, numbers reflect preamplifier channels.

The numbers on the pinout diagram above show the channel connections to the amplifier. By default, the headstage inputs are single ended, with Reference and Ground tied together by a jumper. To make the inputs referential, cut the jumper pictured below.

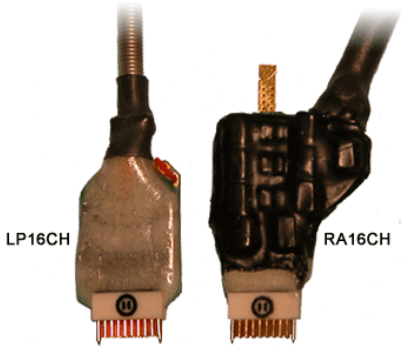
LP32CH:

WARNING! When using multiple headstages ensure that all ground pins are connected to a single common node. See "Headstage Connection Guide" on page 7-97, for more information.

RA16CH/LP16CH/LP16CH-ZNF - 16 Channel Chronic Headstage

The 16 channel chronic headstages are recommended for extracellular neurophysiology using silicon electrodes, metal microelectrodes or microwire arrays with input impedance from 20 kOhm to 5 MOhm. They come in three configurations: standard profile, low profile, and non-ferrous low profile.

The RA16CH and LP16CH (low profile) use a female Omnetics 18 socket female dual row nano connector (0.025"/0.64mm) with 2 guide posts that is compatible with TDT microwire arrays, NeuroNexus chronic electrodes, and a wide variety of connectors. Users can also request a matching male Omnetics connector (OMCON_ML_HB) from TDT for custom built electrode arrays. The low profile LP16CH provides a smaller footprint than the RA16CH for better clearance in tight applications.



The LP16CH-ZNF uses non-ferrous materials, including a non-ferrous Omnetics connector with the same size and pinout as the RA16CH and LP16CH headstages. It can be used for recording single-unit electrophysiology during fMRI neuroimaging.

Part Numbers:

LP16CH: 16-Channel Chronic Low Profile Headstage for Medusa PreAmps

LP16CH-Z: 16-Channel Chronic Low Profile Headstage for Z-Series (PZ) PreAmps

LP16CH-ZNF: 16-Channel Non-Ferrous, Chronic Low Profile Headstage for Z-Series (PZ) Preamps

RA16CH: 16-Channel Chronic Headstage for Medusa PreAmps

RA16CH-Z: 16-Channel Chronic Headstage for Z-Series (PZ) PreAmps

The headstages have sensitive electronics. Always ground yourself before handling.

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

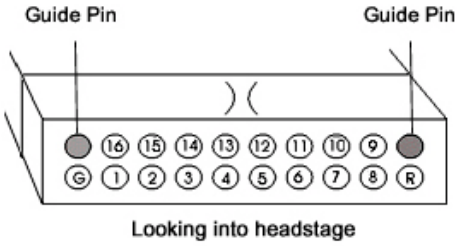
The table below lists the input voltage ranges for the 16 channel chronic headstages for either a +/- 1.5 V or +/- 2.5 V power source.

	Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
LP16CH, LP16CH-ZNF	+/- 1.48 V	+/- 2.49 V
RA16CH	+/- 0.9 V	+/- 1.9 V

Technical Specifications

Input Referred Noise	rms 3 µV bandwidth 300-3000 Hz rms 6 µV bandwidth 30-8000 Hz
Headstage Gain	Unity (1x)
Input Impedance	10^{14} Ohms
Connector	Omnetics 18 socket female dual row nano connector (.025"/.64mm) with 2 guide posts

Pinout



Looking into headstage

The numbers on the pinout diagram above show the channel connections to the amplifier. By default, the headstage inputs are single ended, with Reference and Ground tied together by a jumper. To make the inputs referential, cut the jumper pictured below.

RA16CH:

LP16CH/LP16CH-ZNF:

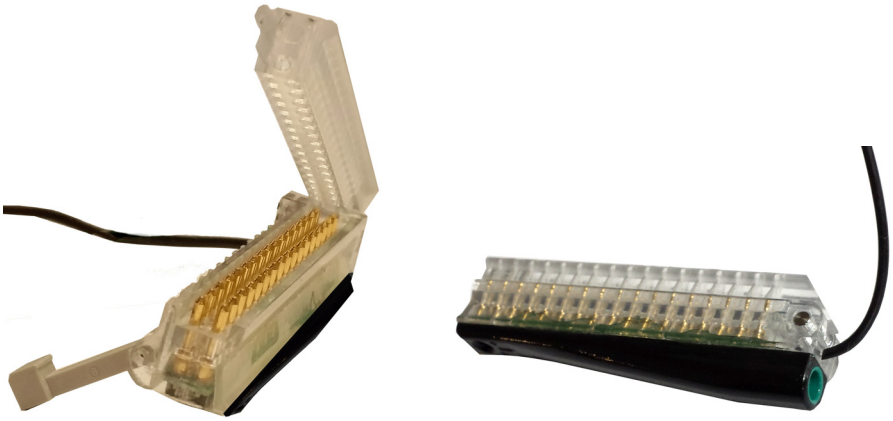
WARNING! When using multiple headstages ensure that all ground pins are connected to a single common node. See "Headstage Connection Guide" on page 7-97, for more information.

ECoG Headstages

CB16-PMT - 16 Channel ECoG Headstage

The 16 Channel ECoG headstages are recommended for 13 gauge tunneling needle/ inline tail probes with impedance ranging from 20 kOhm to 5 Mohm. The headstage includes a Touch Proof connector for optional reference input and a locking bar for secure connection of probe to headstage.

The CB16-PMT is available as a passive or active headstage.



CB16-PMT Connector - Open / Closed, View from Bottom

Part Numbers:

CB16-PMT - 16 Channel Active Headstage for Z-Series (PZ) PreAmps

CB16P-PMT - 16 Channel Passive Headstage for Z-Series (PZ) PreAmps

The headstage has sensitive electronics. Always ground yourself before handling.

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5

V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

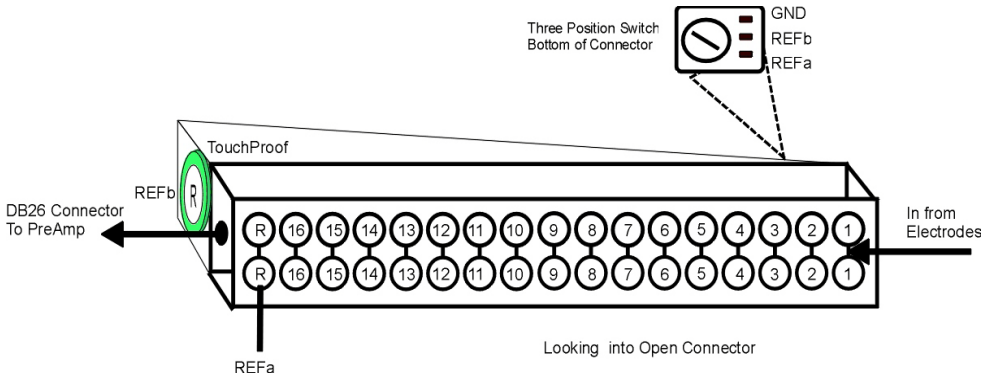
The table below lists the input voltage ranges for the 16 channel ECoG headstages for either a +/- 1.5 V or +/- 2.5 V power source.

	Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
CB16-PMT	-1.5 to 1.4 V	-2.5 to 2.4 V

Technical Specifications

Input Referred Noise	rms 3 µV bandwidth 300-3000 Hz rms 6 µV bandwidth 30-8000 Hz
Headstage Gain	Unity (1x)
Input Impedance	10^{13} Ohms

Pinout



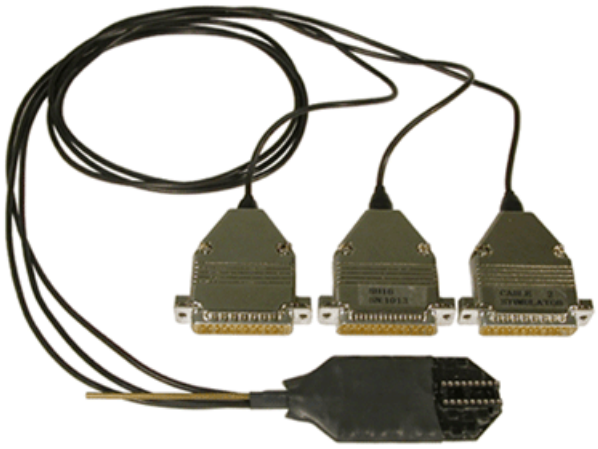
The numbers on the pinout diagram above show the channel connections to the amplifier.

A three position switch is used to connect either REFa, REFb, or GND to the REF line on the DB26 PreAmplifier/Digitizer connector.

The headstage does not provide access to ground and instead relies on the use of the external ground on the preamplifier/digitizer.

SH16 Switchable Headstages

SH16 - Switchable Acute Headstage



The SH16/SH16-Z/SH16-IZ is a 16 channel acute headstage containing recording circuitry that can be bypassed for selected channels and connected to the stimulus isolator. It features high voltage, low leakage solid-state relays to allow for remote switching.

Note: The SH16 provides unity gain (1x) for its recording channels.

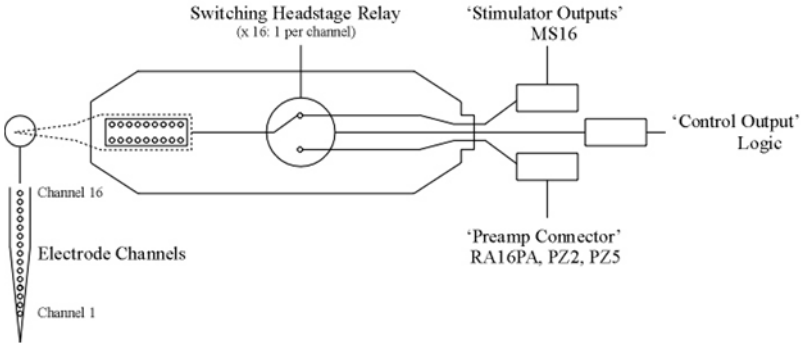
The minimum switching time for the SH16/SH16-Z is dependent on the length of time it takes to send the 24-bit serial control bit pattern (see "Creating the Serial Control Bit Pattern" on page 11-51, for more information) that defines which channels are switched plus an inherent 2 ms delay associated with the solid state relay switches.

The minimum switching time can be calculated as follows:

[Number of bits in serial control pattern (24)] ÷ [Serial data transfer Rate (939 Hz Max)] + 2 ms

Serial Transfer Rate (Hz)	Minimum SH16 Switching Time (ms)
939	28
469	53

The diagram below illustrates how the relays are used to switch channels for recording (to RA16PA) or stimulation (from MS16).



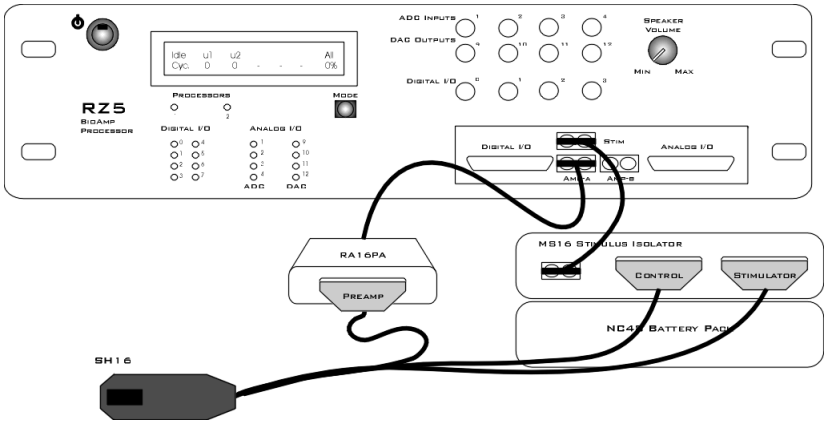
Switchable Headstage Diagram

The 16 channel switchable acute headstage has an 18-pin DIP connector that can be used with standard high impedance metal electrodes. The pinout of the SH16 matches the wiring of NeuroNexus electrodes, allowing direct connection to the headstage. TDT recommends connecting electrodes to an 18-pin DIP socket and then connecting the socket to the headstage to protect the headstage from unnecessary wear and tear.

Important! When using the headstage with the NeuroNexus probes, keep in mind that there may be several versions of the probe. Check the NeuroNexus Website for pin diagrams. Also, see MCMap for a description and examples on how to re-map channel numbers.

Connection Diagram

When using the SH16/SH16-Z with a microstimulator system, connect the system as shown. The diagram below shows a system configuration featuring the RZ5 BioAmp Processor, an MS16 Stimulus Isolator, and RA16PA Medusa PreAmp. Connections are much the same when using the RX7 in place of the RZ5.

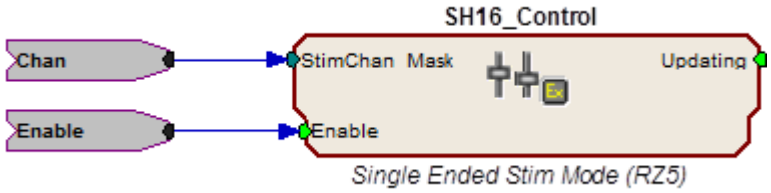


SH16 to MicroStimulator Connection Diagram

Switchable Headstage Operation

When using the SH16/SH16-Z switching headstage with an RZ5 or RX7 processor and an MS4/MS16 Stimulus Isolator, TDT recommends using the SH16_Control macro to set stimulation channels and mode of operation. Based on the macro settings, all necessary control signals are sent from the base station to the headstage via the MS4/MS16 Control output port.

Setup parameters determine which channels are used for stimulation and whether the headstage will be operated in single ended or differential mode.



See the Help text in the macro's properties dialog box for more information about this macro.

Note: The SH16/SH16-Z requires at least 10ms in order to initialize its control bits for use. If you are trying to trigger the enable input you must either use a trigger signal that is delayed 10ms from the point the circuit is run or use a manual trigger method to begin acquisition.

Operating the Switching Headstage without Using the Macro

The SH16_control macro (above) greatly simplifies control of the switching headstage. If the macro cannot be used, the SH16/SH16-Z can be controlled directly from RPvdsEx using the following information.

The SH16/SH16-Z is controlled using the digital I/O (digital control lines) on the MS4/MS16, which are in turn set by writing an integer value directly to memory (poke address values vary depending on the processor used). Channels 1 - 3 of the digital I/O (bits 0-2) are used to send a serial pattern that controls the state of all channels to the SH16/SH16-Z.

Transmitting this data to the headstage from the MS4/MS16 is accomplished using the following 3 digital output lines.

Bit Number	Name	Description	Pin # (Control DB25)
2	DO2	Serial Clock Line	19
1	DO1	Serial Data Line	6
0	DO0	Load/Latch Signal	18

DO0 (Bit 0) is the load/latch signal. This bit is pulsed for a minimum pulse width of 100 nanoseconds to latch the data to the relays on the headstage after the data has been transmitted.

DO1 (Bit 1) is the serial data line. The 24-bit mask must be sent most significant bit (MSB) first. In other words, bit 23 is sent first, then bit 22, bit 21, etc.

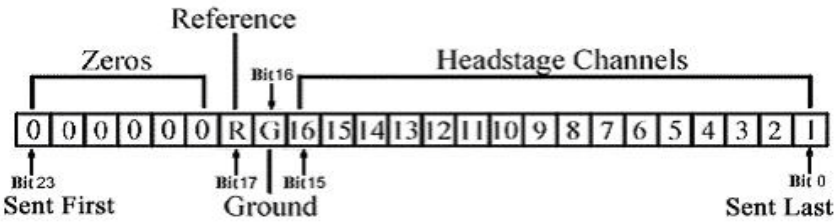
DO2 (Bit 2) is the serial clock signal. When the SH16/SH16-Z is being controlled through a System 3 device such as the MS4/MS16, then the maximum rate for serial data transfer is 939 Hz.

Creating the Serial Control Bit Pattern

Channel setup and control are programmed by serially transmitting a 24-bit pattern to the headstage on the serial data line (DO1). The first bits in the pattern control the

connection of a given channel to the Stimulus Isolator. Bit 16 controls the ground and bit 17 controls the record reference line. Bits 18-23 are not used and are always sent as zeros. By default, all channels are set in the record mode (disconnected from the stimulator). To connect a given electrode to the output of the stimulus isolator, send a binary '1' on the appropriate bit of the pattern. Sending a binary '0' on the appropriate bit will disconnect that electrode from the stimulus isolator and connect it to the recording preamp.

To disconnect the stimulator ground from the record ground during stimulation, a '1' is sent in the mask at bit location 16. To disconnect the record reference line from the headstage and leave it floating during stimulation, a '1' is sent at bit location 17.



Serial Control Bit Pattern

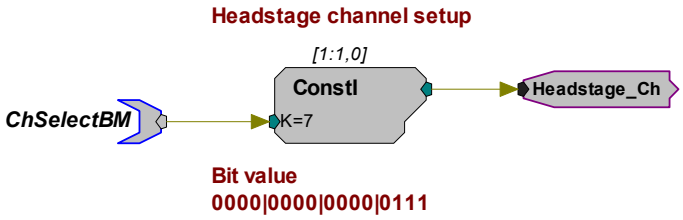
For example, to stimulate on channels 1 (1), 3 (4) and 4 (8), the following serial bit pattern with an integer value of 13 (1 + 4 + 8) should be sent to the headstage. Notice that bits 16 and 17 are not set (1), allowing non-stimulating channels to record using a preamplifier.

0000	0000	0000	0000	0000	1101

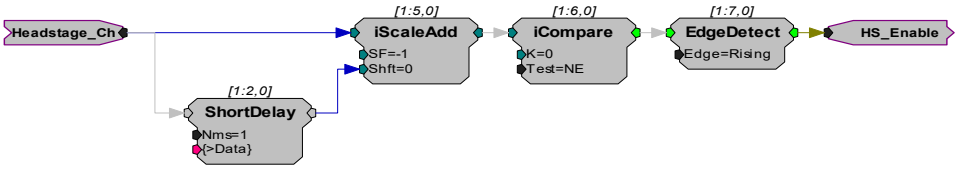
RPvdsEx Circuit

The following circuit illustrates the headstage channel setup and serial data load for the SH16/SH16-Z using an MS4/MS16 and RZ5 or RX7 processor.

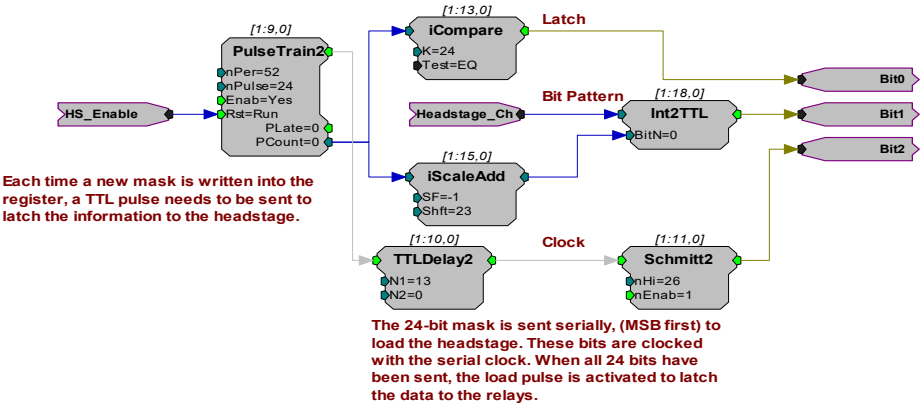
The first figure shows the headstage channel setup. The ChSelectBM parameter tag sets the value of the ConstI with an integer representing the serial control bit pattern discussed above.



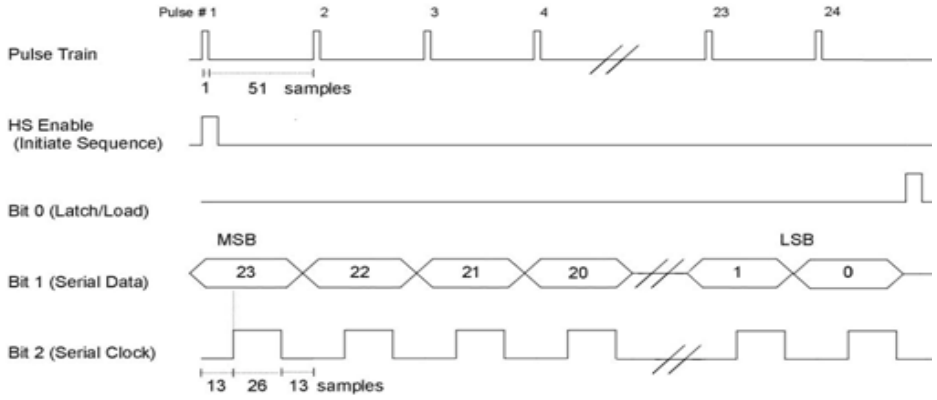
The next segment of the circuit detects a change to the headstage setup and generates a pulse that will reset the serial data transmission to send the new channel selection and control logic.



The third segment of the chain uses a pulse train to send the 24-bit pattern serially (MSB first) to the headstage. After all 24 bits have been sent; the data is latched to the relays.

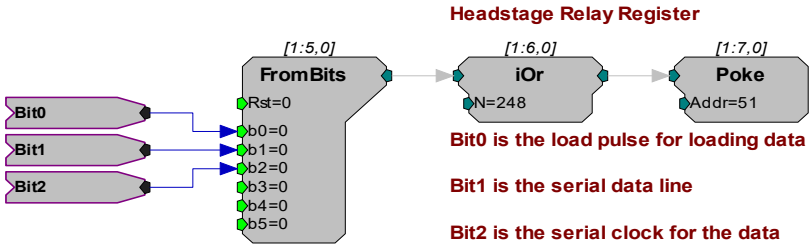


With the sampling rate set to 25 kHz in RPvdsEx and 'nPer' equal to 52 in the PulseTrain2 component, the serial clock (Bit 2) will run at 469 Hz. Setting 'nPer' equal to 26, will allow the clock to run at 939 Hz. The figure below (not to scale) shows the 25kHz pulse rate of 52 samples (1 sample high, 51 samples low) as well as the serial clock rate of 13 samples low, 26 samples high, and 13 samples low.



For headstages with serial numbers >2000, the headstage needs digital high voltages on the input lines of the control connector to power its circuits.

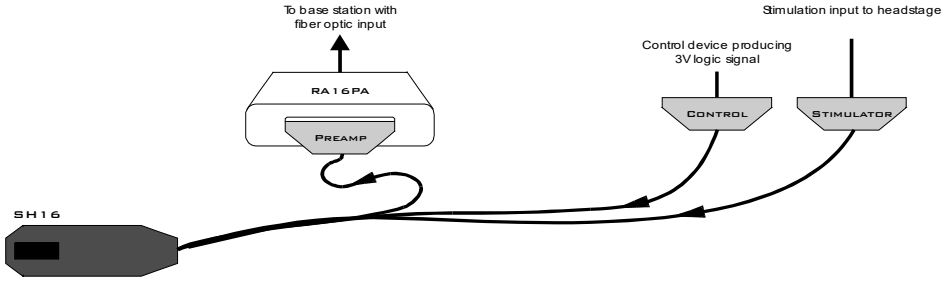
Power the headstage circuits by writing a logic '1' (high) to the MS16 control bitss 3-7). In the circuit segment below, the latch, data, and clock lines are fed directly to bits 0, 1, and 2 respectively on the FromBits component and bits 3-7 are set high by ORing the value from the FromBits component with the value 248 (binary: 0000 0000 1111 1000).



A poke component is used to send the resulting value to memory address 51 on the RZ5 processor or memory address 3 on the RX7. The Poke RPvdsEx component writes values to a specific device memory location and should be used with care.

Using the Switching Headstage with Other Devices

When using the SH16/SH16-Z with hardware other than a microstimulator system, connect as follows:



The Serial Control Bit Pattern that controls connection of a given channel to the Stimulus Isolator can be sent using any 3 digital logic lines that will produce a +3V logic signal. Circuit design is similar to the example above, designed for use with the RZ5 and RX7 processors, but must be modified by routing Bit 0, Bit 1, and Bit 2 to the appropriate digital outputs of the device (instead of using the Poke component).

Note: The serial clock (Bit 2) on the SH16/SH16-Z can be run at a maximum rate of 5 MHz for other devices.

Technical Specifications

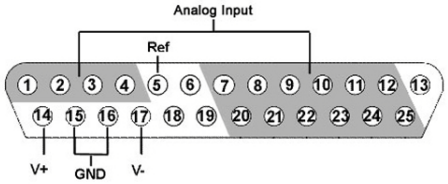
Headstage Gain	Unity (1x)
Input Impedance	10^{14} Ohms

SH16/SH16-Z Pinout Diagrams

PreAmp Connector

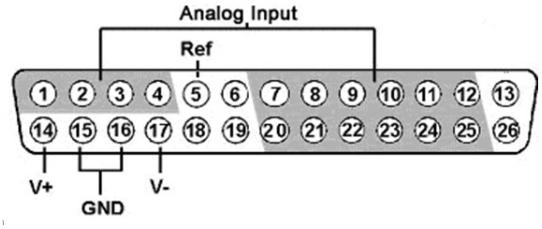
For SH16 headstages with serial numbers <2000, the DB25 connector labeled Preamp must be connected as it supplies power to the headstage. For headstages with serial numbers >2000, this connector does not need to be connected if the user is not recording on the non-stimulating channels.

DB25 Pinout Connections for use with Medusa PreAmps



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channel Number Ch 1-4		14	V+	Positive Voltage
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17	V-	Negative Voltage
5	REF	Reference Pin		18	NA	Not Used
6	NA	Not Used		19	NA	Not Used
7	A5	Analog Input Channel Number Ch 5, 7, 9, 11, 13, and 15		20	A6	Analog Input Channel Number Ch 6, 8, 10, 12, 14, and 16
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	NA	Not Used				

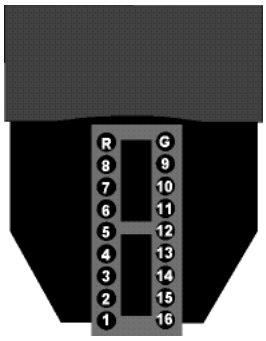
Mini DB26 Pinout Connections for use with PZ PreAmps



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channel Number Ch 1-4		14	V+	Positive Voltage
2	A2			15	GND	Ground
3	A3			16	GND	Ground
4	A4			17	V-	Negative Voltage
5	REF	Reference Pin		18	NA	Not Used
6	NA	Not Used		19	NA	Not Used
7	A5	Analog Input Channel Number Ch 5, 7, 9, 11, 13, and 15		20	A6	Analog Input Channel Number Ch 6, 8, 10, 12, 14, and 16
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	NA	Not Used		26	NA	Not Used

Headstage Pinout

The numbers in the diagram to the right refer to the channel connections to the preamp connector or stimulator connector.



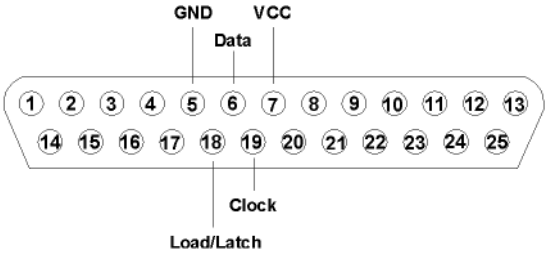
"G" on the diagram to the right is connected to the reference pin (Ref) on the stimulator connector and can also connect to the ground pin (GND) of the preamp connector through a switchable relay in the SH16/SH16-Z.

"R" on the diagram to the right is connected to a switchable relay that can connect to the "Ref" pin of the preamp connector.

The connector accepts 0.5 mm diameter male pins.

The headstage has sensitive electronics. Always ground yourself before handling.

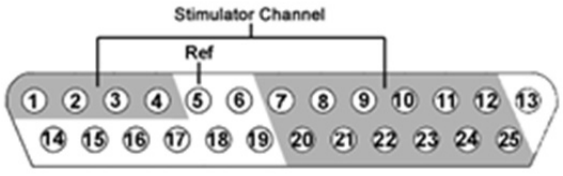
DB25 Control Connector



The connector can be connected to any control device that produces a 3 V logic signal. For headstages, serial numbers >2000, this connector supplies power to the headstage and must be connected.

Note: Pins that are not labeled are not connected.

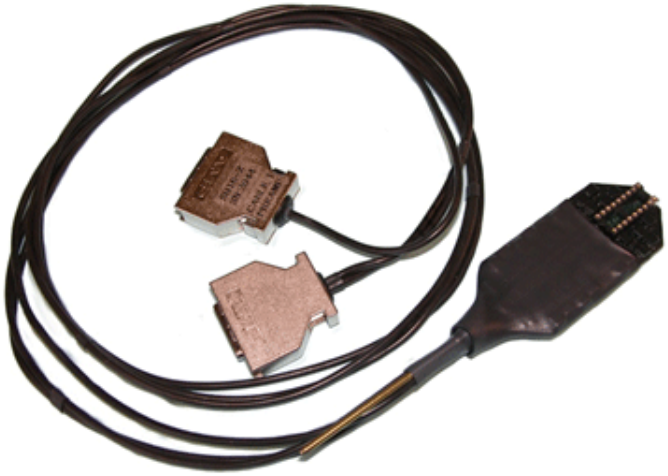
DB25 Stimulator Connector



Note: The global reference (Ref) is connected to the SH16/SH16-Z ground pin (G of headstage pinout).

Pin	Name	Description		Pin	Name	Description
1	S1	Stimulator Channels Ch 1-4		14	NA	Not Used
2	S2			15		
3	S3			16		
4	S4			17		
5	Ref	Reference		18		
6	NA	Not Used		19		
7	S5	Stimulator Channels Ch 5, 7, 9, 11, 13, and 15		20	S6	Stimulator Channels Ch 6, 8, 10, 12, 14, and 16
8	S7			21	S8	
9	S9			22	S10	
10	S11			23	S12	
11	S13			24	S14	
12	S15			25	S16	
13	NA	Not Used				

SH16-IZ - 16 Channel Switchable Acute Headstage



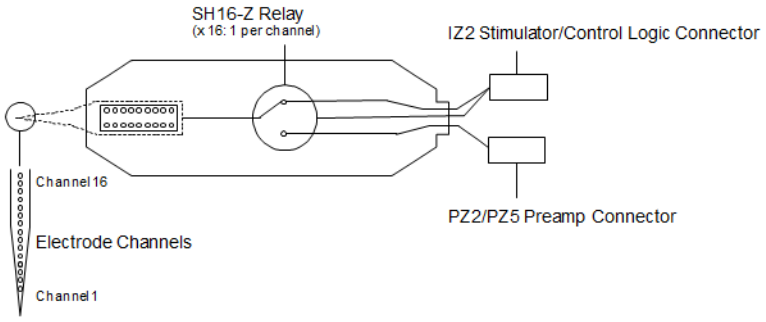
The SH16-IZ is a 16 channel acute headstage containing programmable relays that connect selected channels to the IZ2 stimulator and leave unselected channels connected to the PZ2. It features high voltage, low leakage solid-state relays to allow for remote switching.

Note: The SH16-IZ switching headstage provides unity gain (1x) for its recording channels.

Channel selection is handled within the IZ2_Control macro which generates a 24-bit serial control bit pattern to control SH16-Z channel switching. The minimum switching time is dependent on the length of time it takes to receive the control bit pattern plus an inherent 2 ms delay associated with the solid state relay switches. Typical switching times are shown in the table below.

Sampling Rate	Minimum SH16-Z Switching Time (ms)
50 kHz and above	28
25 kHz	53

The diagram below illustrates how the relays are used to switch channels for recording (to PZ2) or stimulation (from IZ2).



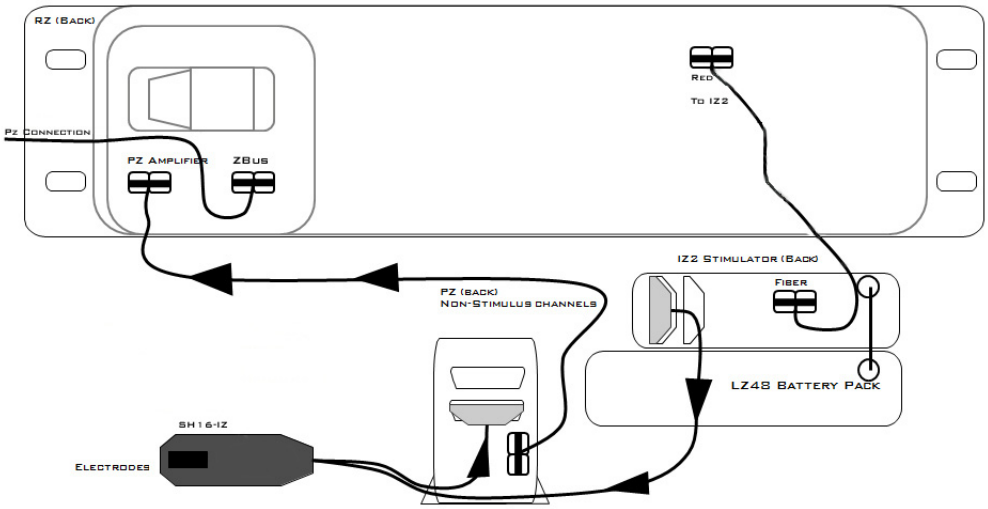
Switchable Headstage Diagram

The 16 channel switchable acute headstage has an 18-pin DIP connector that can be used with standard high impedance metal electrodes. The pinout of the SH16-IZ matches the wiring of NeuroNexus electrodes, allowing direct connection to the headstage. TDT recommends connecting electrodes to an 18-pin DIP socket and then connecting the socket to the headstage to protect the headstage from unnecessary wear and tear.

Important! When using the headstage with the NeuroNexus probes, keep in mind that there may be several versions of the probe. Check the NeuroNexus Website for pin diagrams. Also, see MCMap for a description and examples on how to re-map channel numbers.

Connection Diagram

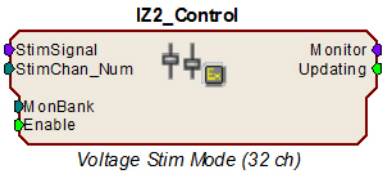
When using the SH16-IZ with a microstimulator system, connect the system as shown. The diagram below shows a system configuration featuring the RZ Processor, an IZ2 Stimulator, and PZ2 preamp or PZ5 digitizer. The IZ2 connects to the front panel of an RZ5D and the back panel of all other RZ devices.



SH16-IZ to MicroStimulator Connection Diagram

Switchable Headstage Operation

When using the SH16-IZ switching headstage it should be enabled in the IZ2_Control macro.



Voltage Stim Mode (32 ch)

The StimChan parameter input is used to set the stimulation channels. Based on the macro settings, you either specify a single channel to open for stimulation or send a channel mask if stimulating on more than one channel. All necessary control signals are sent from the base station to the headstage via the IZ2 output port. To use an electrode as the stimulus return path, make sure that channel is open for stimulation and send an inverted stimulus signal to that channel.

Multiple SH16-IZs can be used with a single IZ2. The MonBank input determines which SH16-IZ is updated when the StimChan value is changed.

See the Help text in the IZ2_Control macro's properties dialog boxes for more information about this macro.

Note: The SH16-IZ Headstage requires at least 10 ms to initialize its control bits for use. If you are trying to trigger the enable input you must either use a trigger signal that is delayed 10 ms from the point the circuit is run or use a manual trigger method to begin acquisition.

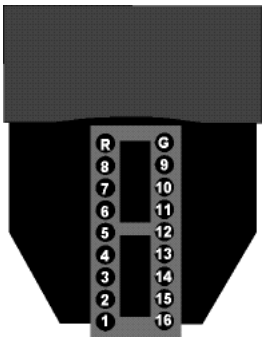
Technical Specifications

Headstage Gain	Unity （1x）
Input Impedance	10^{14} Ohms

SH16-IZ Pinout Diagrams

Headstage Pinout

The numbers in the diagram to the right refer to the channel connections to the preamp connector or stimulator connector.



"G" on the diagram to the right is connected to the ground pin （GND） on the stimulator connector and can also connect to the ground pin （GND） of the preamp connector through a switchable relay in the SH16-IZ.

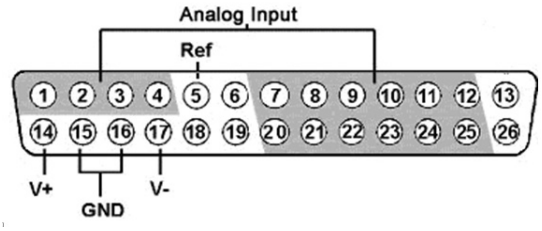
"R" on the diagram to the right is connected to a switchable relay that can connect to the "Ref" pin of the preamp connector.

The electrode connector accepts 0.5 mm diameter male pins.

The headstage has sensitive electronics. Always ground yourself before handling.

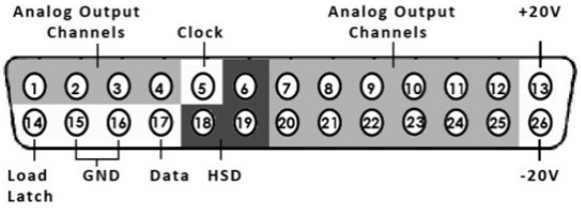
PreAmp Connector

For SH16-IZ headstages, this connector does not need to be connected if the user is not recording on the non-stimulating channels.



Pin	Name	Description	Pin	Name	Description
1	A1	Analog Input Channel Number Ch 1-4	14	V+	Positive Voltage
2	A2		15	GND	Ground
3	A3		16	GND	Ground
4	A4		17	V-	Negative Voltage
5	REF	Reference Pin	18	NA	Not Used
6	NA	Not Used	19	NA	Not Used
7	A5	Analog Input Channel Number Ch 5, 7, 9, 11, 13, and 15	20	A6	Analog Input Channel Number Ch 6, 8, 10, 12, 14, and 16
8	A7		21	A8	
9	A9		22	A10	
10	A11		23	A12	
11	A13		24	A14	
12	A15		25	A16	
13	NA	Not Used	26	NA	Not Used

DB26 Stimulator Connector



Pin	Name	Description	Pin	Name	Description
1	S1	Stimulator Channels Ch 1-4	14	LL	Load/Latch
2	S2		15	GND	Ground
3	S3		16	GND	Ground
4	S4		17	Data	Digital Data
5	Clock	Digital Clock	18	HSD	Stimulator Detect
6	HSD	Stimulator Detect	19	HSD	Stimulator Detect
7	S5	Stimulator Channels Ch 5, 7, 9, 11, 13, and 15	20	S6	Stimulator Channels Ch 6, 8, 10, 12, 14, and 16
8	S7		21	S8	
9	S9		22	S10	
10	S11		23	S12	
11	S13		24	S14	
12	S15		25	S16	
13	+20V	+20V	26	-20V	-20V

Part 12: Low Impedance Headstages

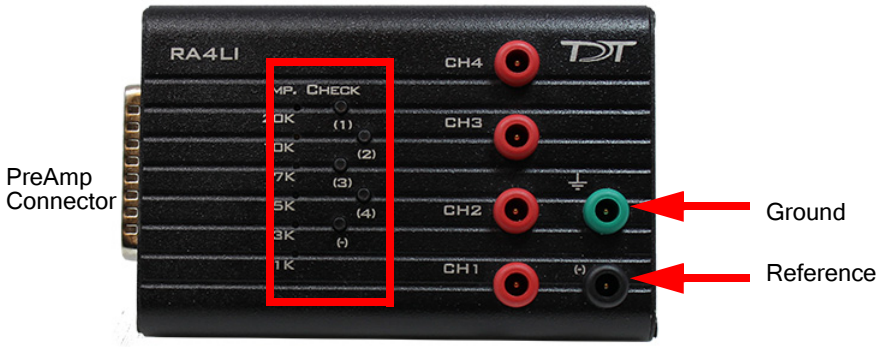
Low Impedance Headstages

RA4LI - Four Channel Headstage

The RA4LI headstage is designed for low impedance electrodes with input impedance between <1 kOhm and 20 kOhm. Electrode connectors are standard 1.5 mm safety connectors making it easy to connect to standard needle and surface electrodes for recording evoked potentials and EEG's. The headstage connects directly to the RA4PA Medusa preamplifier's 25-pin connector. A built in impedance checker can be used to test each channel and the reference. Additional 20x gain on the headstage improves signal-to-noise of low voltage signals.

Impedance Checking with the Low-Impedance Headstage

The Impedance checker on the RA4LI provides a simple check of the channel impedance relative to ground. To check the impedance level, press the button next to the channel indicator. The highest-level light indicates the maximum impedance between the channel and the ground. If all impedance lights are illuminated it is likely that one of the channels is not properly connected. The (-) impedance button checks the impedance between the reference and the ground.



Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range. Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

The table below lists the input voltage ranges for the RA4LI headstage for either a +/- 1.5 V or +/- 2.5 V power source.

Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
+/- 33 mV	+/- 80 mV

Headstage Technical Specifications

Warning! When using multiple headstages ensure that all ground pins are connected to a single common node. See “Headstage Connection Guide” on page 7-97, for more information.

Input Referred Noise	rms 0.1 µV bandwidth 300-3000 Hz 0.3 µ Vbandwidth 2-8000 Hz
Headstage Gain	20x
Highpass Filter	2.2 Hz
Lowpass Filter	7.5 kHz
Input Impedance	10^6 Ohm

RA16LI - 16 Channel Headstage

The sixteen channel low impedance headstage (RA16LI) is a high quality, low-impedance headstage designed for recording high channel count EEG's.

The RA16LI headstage is designed for low impedance electrodes and electrode caps with input impedance between <1 kOhm and 20 kOhm. Either headstage unit connects to the Medusa preamplifier's 25-pin connector. The simple interface to the RA16PA preamplifier makes it easy to connect your electrodes to our system.

An adapter is also available to connect a low impedance headstage to a PZ preamplifier. See “Preamplifier Adapters” on page 13-35, for more information. A built in impedance checker can be used to test each channel and the reference. Additional 20x gain on the headstage improves signal-to-noise of low voltage signals.

PreAmp Connector

Electrode Connector

Impedance Checking with the Low-Impedance Headstage

The Impedance checker on the RA16LI provides a simple check of the channel impedance relative to ground. To check the impedance level, press the button next to the channel indicator. The highest-level light indicates the maximum impedance between the channel and the ground. If all impedance lights are illuminated it is likely that one of the channels is not properly connected. The (-) impedance button checks the impedance between the reference and the ground.

Headstage Voltage Range

When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range.

Also keep in mind that the range of the headstage varies depending on the power supply provided by the preamplifier. TDT preamplifiers supply +/- 1.5 V, but third party preamplifiers may vary. TDT recommends using preamplifiers which deliver +/- 2.5 V or less. Check the preamplifier voltage input and power supply specifications and headstage gain to determine the voltage range of the system.

The table below lists the input voltage ranges for the RA16LI headstage for either a +/- 1.5 V or +/- 2.5 V power source.

Headstage input range when using +/- 1.5 V power source	Headstage input range when using +/- 2.5 V power source
+/- 33 mV	+/- 80 mV

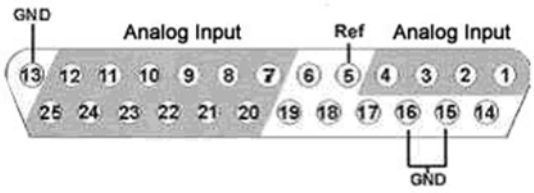
Headstage Technical Specifications

WARNING! When using multiple headstages ensure that all ground pins are connected to a single common node. See “Headstage Connection Guide” on page 7-97, for more information.

Input Referred Noise	rms 0.1 µV bandwidth 300-3000 Hz 0.3 µV bandwidth 2-8000 Hz
Headstage Gain	20x
Highpass Filter	2.2 Hz
Lowpass Filter	7.5 kHz
Input Impedance	10^6 Ohm

Electrode Connector Pinout

The electrode connector is a 25-pin connector. Information on the pin inputs is provided below.



Note: Pins 6, 14, 17, 18 and 19 are not connected.

Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		14	NA	Not Used
2	A2			15	GND	Ground
3	A3			16	GND	
4	A4			17	NA	Not Used
5	Ref	Reference		18	NA	
6	NA	Not Used		19	NA	
7	A5	Analog Input Channels		20	A6	Analog Input Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	GND	Ground				

RA16LI-D - 16 Channel Headstage with Differential

The RA16LI-D headstage is designed for fully differential recordings from low impedance electrodes and electrode caps with input impedance between <1 kOhm and 20 kOhm. It connects to the Medusa preamplifier's 25-pin connector. The simple interface to the RA16PA preamplifiers makes it easy to connect your electrodes to our system. An adapter is also available to connect a low impedance headstage to a PZ preamplifier. See "DBF-MiniDBM Low Impedance Headstage to PZ Preamplifier (16-channels)" on page 35, for more information.

The differential inputs allow for improved common mode rejection on all channels. Because of the increased complexity of the circuitry, the RA16LI-D does not have impedance checking. The headstage connector is a DB44. The pin out diagram is shown below.

Headstage Voltage Range

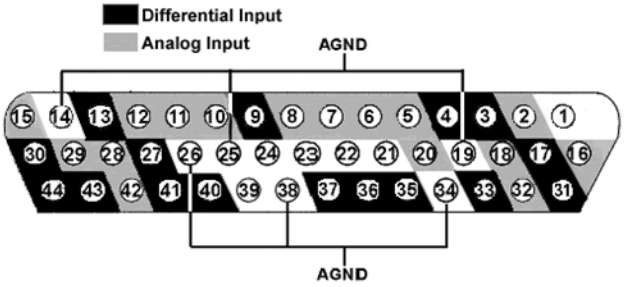
When using a TDT preamplifier the voltage input range of the preamplifier is typically lower than the headstage and must be considered the effective range of the system. Check the specifications of your amplifier for voltage range.

Headstage Technical Specifications

WARNING! When using multiple headstages ensure that all ground pins are connected to a single common node. See “Headstage Connection Guide” on page 7-97, for more information.

Input Referred Noise	rms 0.1 µ V bandwidth 300-3000 Hz 0.3 µ V bandwidth 2-8000 Hz
Headstage Gain	20x
Highpass Filter	2.2 Hz
Lowpass Filter	7.5 kHz
Input Impedance	10^6 Ohm

Pinout Diagram



Note: Pins 1, 21-24 and 39 are not connected.

Pin	Name	Description	Pin	Name	Description
1	NA	Not Used	25	AGND	Analog Ground
2	A2	Analog Input	26	AGND	
3	D3	Differential Input	27	D12	Differential Input
4	D5		28	A14	Analog Input
5	A5	Analog Input	29	A15	
6	A7		30	D16	Differential Input
7	A8		31	D1	
8	A9		32	A3	Analog Input
9	D9	Differential Input	33	D4	Differential Input
10	A10	Analog Input	34	AGND	Analog Ground
11	A11		35	D6	Differential Input
12	A12		36	D7	
13	D13	Differential Input	37	D8	
14	AGND	Analog Ground	38	AGND	Analog Ground
15	A16	Analog Input	39	NC	
16	A1		40	D10	Differential Input
17	D2	Differential Input	41	D11	
18	A4	Analog Input	42	A13	Analog Input
19	AGND	Analog Ground	43	D14	Differential Input
20	A6	Analog Input	44	D15	
21	NA	Not Used			
22	NA				
23	NA				
24	NA				

Part 13: Adapters and Connectors

ZIF-Clip® Headstage Adapters

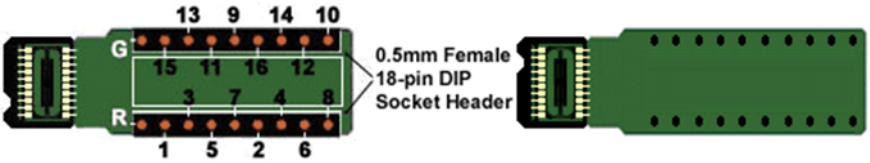
ZIF-Clip® headstage adapters are available for use with a variety of electrode styles. When using adapters, keep in mind that standard operation (referential vs single-ended) may vary for acute and chronic preparations. Carefully note and understand the use of the ground (G) and reference (R) connections provided on each adapter.

Standard operation for ZIF-Clip® headstages is referential. Headstage adapters can be configured for single-ended operation by tying ground (G) and reference (R) connections together on the adapter (if available). Refer to the electrode manufacturer's documentation for information on single-ended or referential configurations.

Note: When using these adapters with NeuroNexus, Gray Matter, or CyberKinetics probes, keep in mind that there may be updates to pin configurations. Check the suppliers' website for pin diagrams. Also see the Channel Mapper gizmo in Synapse for a description and examples on how to re-map channel numbers.

ZCA-DIP16 ZIF-Clip® Headstage to Acute Probe (16 Channels)

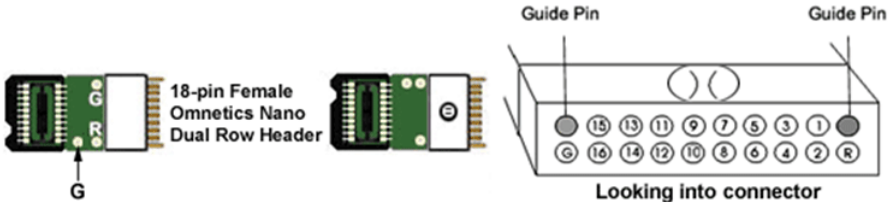
The ZCA-DIP16 adapter allows the user to connect a 16-channel acute probe (such as NeuroNexus) to a 16-channel ZIF-Clip® headstage. Ground and reference pins are located on the DIP connector and may be tied together for single-ended operation.



Pinouts are looking into the connector and reflect the preamplifier channels

ZCA-OMN16 ZIF-Clip® Headstage to Chronic Probe (16 Channels)

The ZCA-OMN16 adapter connects a 16-channel chronic Omnetics based probe to a 16-channel ZIF-Clip® headstage. Ground and reference pins may be tied together for single-ended operation with a jumper wire between the G and R pads. Otherwise the adapter operates in referential mode.

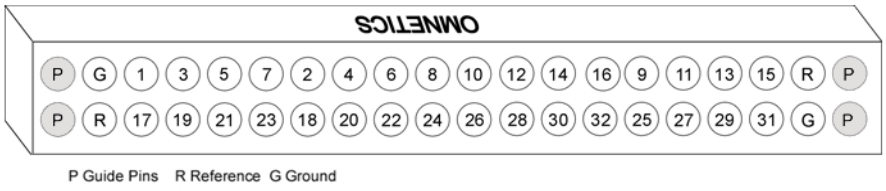


Pinouts are looking into the connector and reflect the preamplifier channels

ZCA-OMN32 ZIF-Clip® Headstage to Chronic Probe (32 Channels)

The ZCA-OMN32 adapter connects a 32-channel chronic Omnetics based probe to a 32-channel ZIF-Clip® headstage.

Ground and reference pins may be tied together for single-ended operation with a jumper wire between the G and R pads. Otherwise the adapter operates in referential mode.



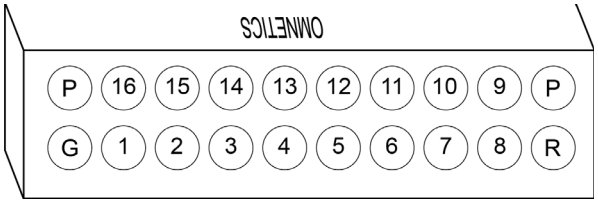
Pinouts are looking into the connector and reflect the preamplifier channels

ZCA-FLEX-OMNX2 ZIF-Clip® Headstage to Chronic Probe (2 x 16 Channels)

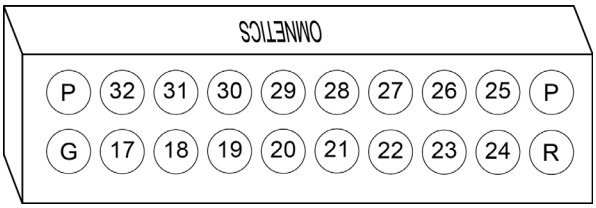
The ZCA-FLEX-OMNX2 adapter connects two 16-channel chronic Omnetics based probe to a 32-channel ZIF-Clip® headstage with flex cable.

ZCA-FLEX-OMNX2 (Side A on top, Side B on bottom)

The standard cable length is two inches. The reference pins on each connector are shared on the PCB. The ground pins are also shared. The ground and reference are independent and can only be shorted on the probe or by choosing the 'None' reference option on the PZ5/SIM amplifier if using an analog ZIF headstage.



Side A pinouts are looking into the connector and reflect the preamplifier channels



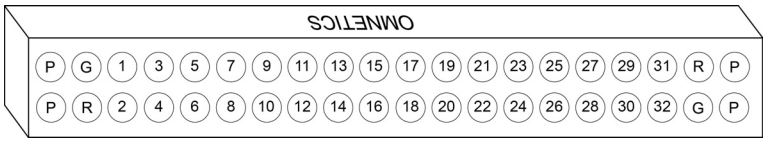
Side B pinouts are looking into the connector and reflect the preamplifier channels

ZCA32-FLEX-OMN ZIF-Clip® Headstage to Chronic Probe (32 Channels)

The ZCA32-FLEX-OMN adapter connects a 32-channel chronic Omnetics based probe to a 32-channel ZIF-Clip® headstage with flex cable.

ZCA32-FLEX-OMN (Side A shown)

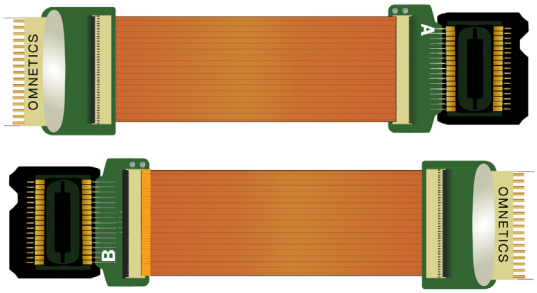
The standard cable length is two inches. A jumper location on the PCB can be used to short ground and reference together for single-ended operation. Otherwise the adapter operates in referential mode.



Pinouts are looking into the connector and reflect the preamplifier channels

ZCA64-FLEX-OMN ZIF-Clip® Headstage to Chronic Probe (2 x 32 Channels)

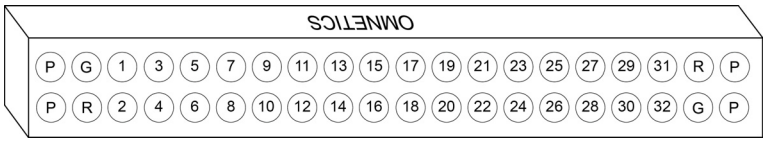
The ZCA64-FLEX-OMN adapter connects two 32-channel chronic Omnetics based probe to a 64-channel ZIF-Clip® headstage with flex cable.



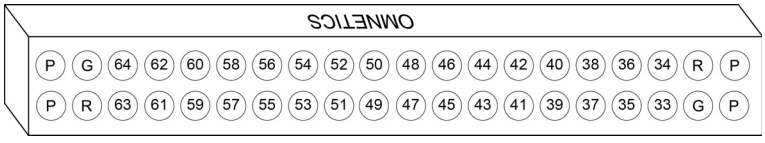
ZCA64-FLEX-OMN (Side A on top, Side B on bottom)

The standard cable length is two inches. The reference pins on each connector are shared on the PCB. A jumper location on the PCB can be used to short ground and reference together for single-ended operation. Otherwise the adapter operates in referential mode.

Important! The pinouts below are for the ZC64 analog headstages only. If you are using a ZD64 digital headstage, please refer to the ZD64 headstage section of this manual for the pinout.



Side A pinouts are looking into the connector and reflect the preamplifier channels



Side B pinouts are looking into the connector and reflect the preamplifier channels

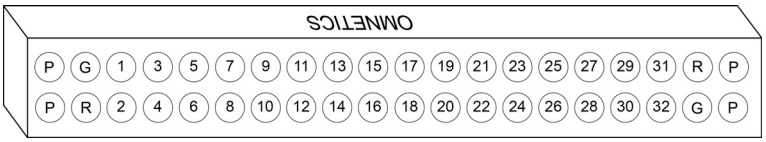
ZCA96-FLEX-OMN ZIF-Clip® Headstage to Chronic Probe (3 x 32 Channels)

The ZCA96-FLEX-OMN adapter connects three 32-channel chronic Omnetics based probe to a 96-channel ZIF-Clip® headstage with flex cable.

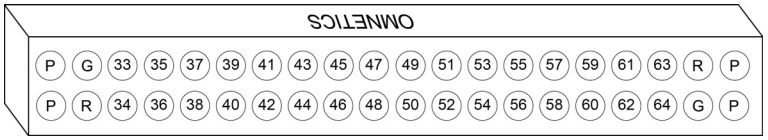
ZCA96-FLEX-OMN (Side A on top, Side B on bottom)

The standard cable length is two inches. The reference pins on each connector are shared on the PCB. A jumper location on the PCB can be used to short ground and reference together for single-ended operation. Otherwise the adapter operates in referential mode.

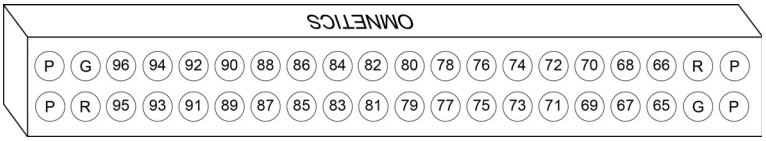
Important! The pinouts below are for the ZC96 analog headstages only. If you are using a ZD96 digital headstage, please refer to the ZD96 headstage section of this manual for the pinout.



Side A 1-32 pinout looking into the connector, reflects the preamplifier channels



Side A 33-64 pinout looking into the connector, reflects the preamplifier channels

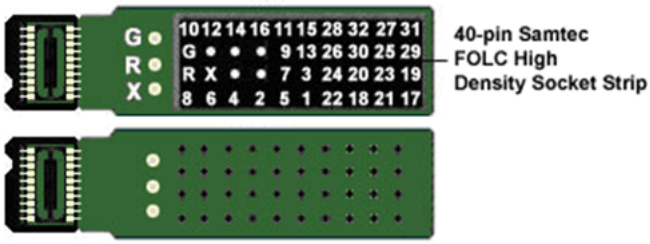


Side B 65-96 pinout looking into the connector, reflects the preamplifier channels

ZCA-NN32 ZIF-Clip® Headstage to 32 Channel Acute Probe)

The ZCA-NN32 adapter connects a 32-channel acute NeuroNexus probe to a 32-channel ZIF-Clip® headstage.

Note: X (Ref) is a reference pin that is connected from the adapter to the probe only. See the jumper configuration below for more information.



Pinouts are looking into the connector and reflect the preamplifier channels.

ZCA-EIB16 ZIF-Clip® Headstage to Electrode Interface Board (16 Channels)

The ZCA-EIB16 adapter allows the user to connect 16 channels of electrode wire to a 16-channel ZIF-Clip® headstage plus ground and reference.

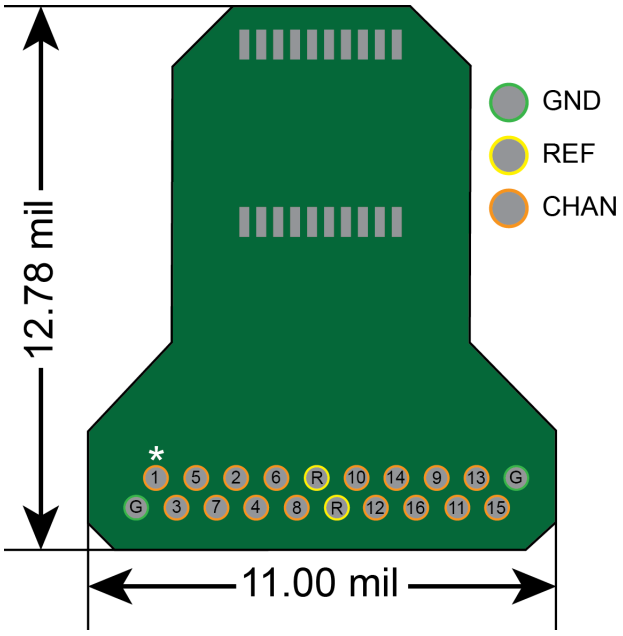
Wires can be soldered to holes or connected using EIB pins, such as the large EIB tapered pins available from NeuraLynx.

To guard against noise pickup, the lengths of any additional wires should be minimized and the wires should be bundled together to avoid creating open loops that can pick up inductive interference.

Specifications:

Hole diameter: .3 mm

Row Spacing: 0.69 mm from center to center



ZCA-EIB16 Pinout and Dimensions Diagram

ZCA-EIB32 ZIF-Clip® Headstage to Electrode Interface Board (32 Channels)

The ZCA-EIB32 adapter allows the user to connect 32 channels of electrode wire to a 32-channel ZIF-Clip® headstage plus ground and reference.

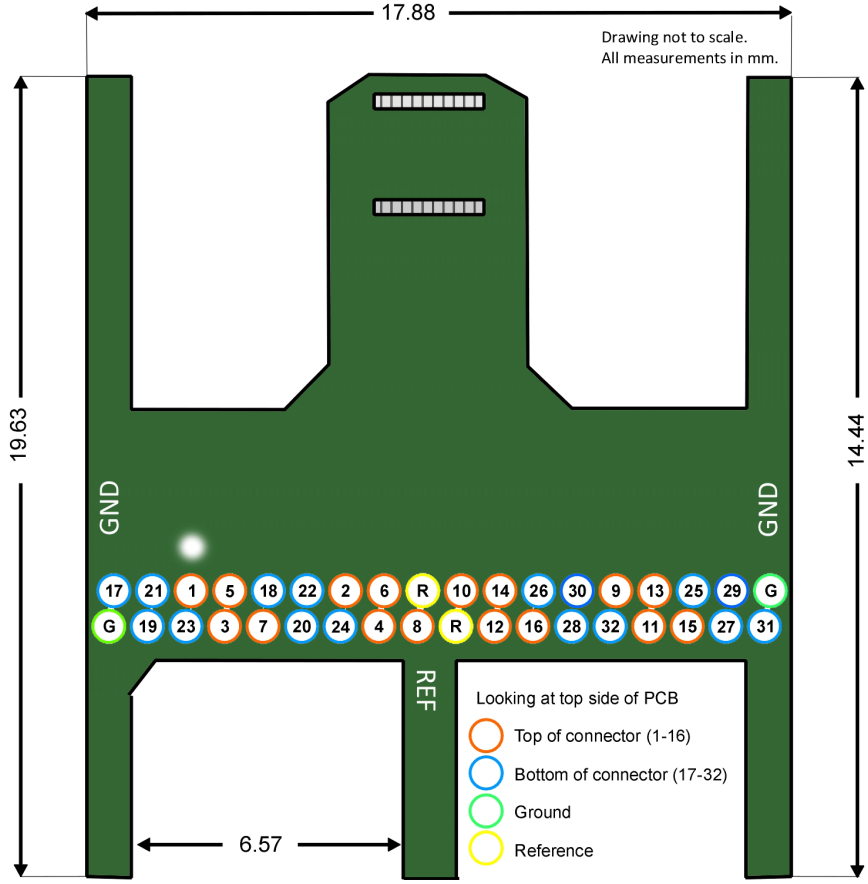
Wires can be soldered to holes or connected using EIB pins, such as the large EIB tapered pins available from NeuraLynx.

To guard against noise pickup, the lengths of any additional wires should be minimized and the wires should be bundled together to avoid creating open loops that can pick up inductive interference.

Specifications:

Hole diameter: .3 mm

Row Spacing: 0.69 mm from center to center



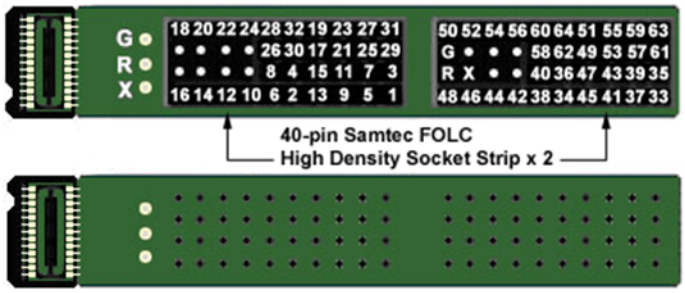
ZCA-EIB32 Pinout and Dimensions Diagram

ZCA-NN64 ZIF-Clip® Headstage to 64 Channel Acute Probe)

The ZCA-NN64 adapter connects a 64-channel acute NeuroNexus probe to a 64-channel ZIF-Clip® headstage.

Important! The pinout below is for the ZC64 analog headstages only. If you are using a ZD64 digital headstage, please refer to the ZD64 headstage section of this manual for its pinout.

Note: X (Ref) is a reference pin that is connected from the adapter to the probe only. See the jumper configuration below for more information.



Pinouts are looking into the connector and reflect the preamplifier channels.

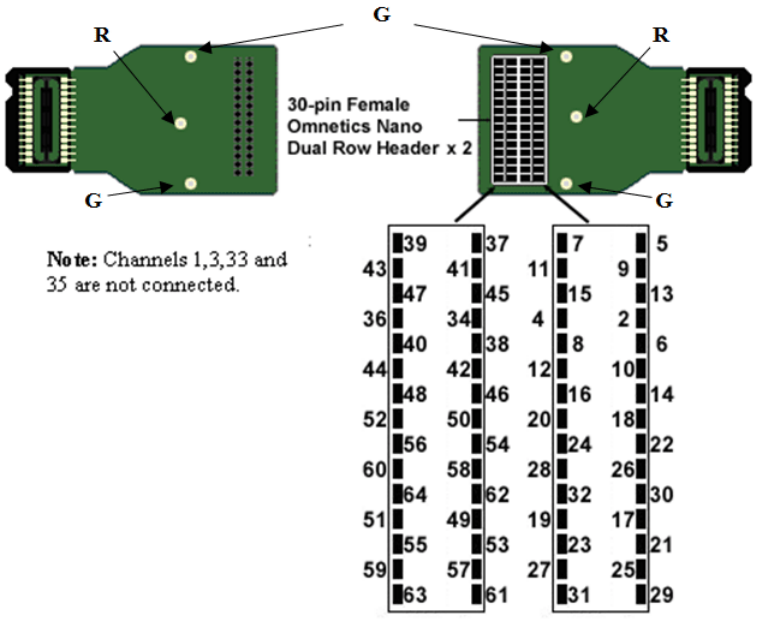
Jumper Configuration

The following table describes the jumper configurations for both the ZCA-NN32 and ZCA-NN64.

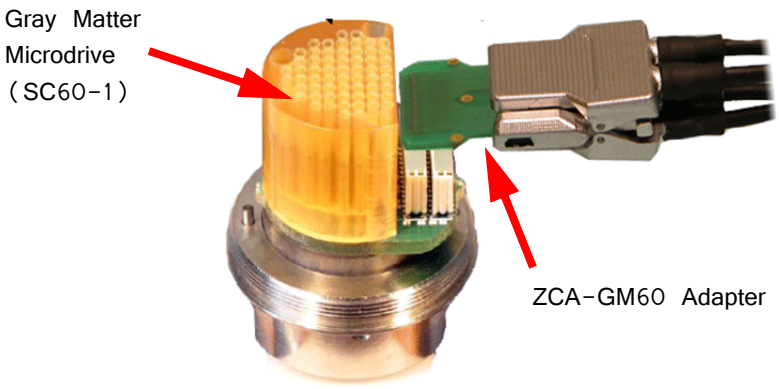
Jumper Connections	Operation
G R X (Ref)	Shorts headstage Ground and Reference inputs together, yielding single-ended amplification of signals relative to ground.
G R X (Ref)	Shorts headstage Reference input to the pin labeled X (a low impedance site on the probe) yielding referential amplification of signals relative to the voltage of the X (Ref) site.
G R X (Ref)	Headstage Ground and Reference separated and X (Ref) pin is not used, yielding referential amplification of signals relative to the voltage of the Reference

ZCA-GM60 ZIF-Clip® Headstage to 60-Channel Chronic Probe

The ZCA-GM60 adapter connects a 60-channel chronic Gray Matter microdrive (SC60-1) to a 64-channel ZIF-Clip® headstage. Ground and reference pins are located on the adapter for access to single-ended and referential modes of operation. See the diagram below for connection details.



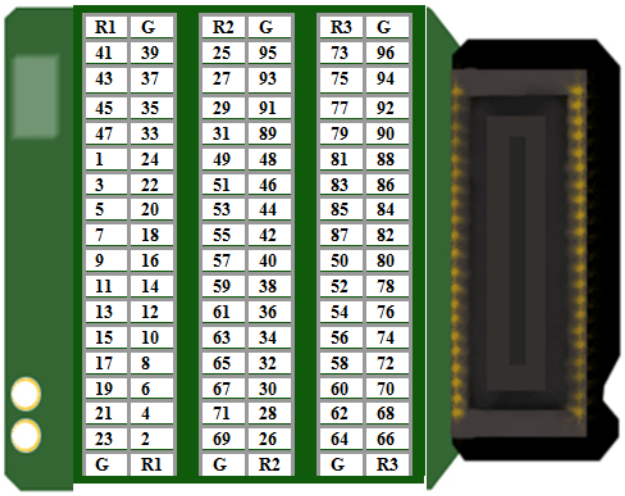
Pinouts are looking into the connector and reflect the preamplifier channels.



ZCA-GM60 Connection Diagram

ZCA-OMN96 ZIF-Clip® Headstage to 96-Channel Omnetics Probe

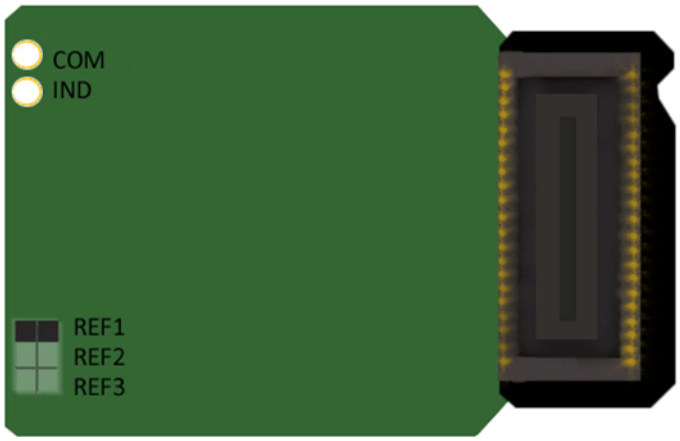
The ZCA-OMN96 adapter connects a 96-channel chronic Omnetics connector to a 96-channel ZIF-Clip® headstage. For single-ended operation, tie COM (ground) and IND (indifferent reference) together. IND is the global headstage reference.



R1	G	R2	G	R3	G
41	39	25	95	73	96
43	37	27	93	75	94
45	35	29	91	77	92
47	33	31	89	79	90
1	24	49	48	81	88
3	22	51	46	83	86
5	20	53	44	85	84
7	18	55	42	87	82
9	16	57	40	50	80
11	14	59	38	52	78
13	12	61	36	54	76
15	10	63	34	56	74
17	8	65	32	58	72
19	6	67	30	60	70
21	4	71	28	62	68
23	2	69	26	64	66
G	R1	G	R2	G	R3

R1 Probe Reference 1
R2 Probe Reference 2
R3 Probe Reference 3
G Ground

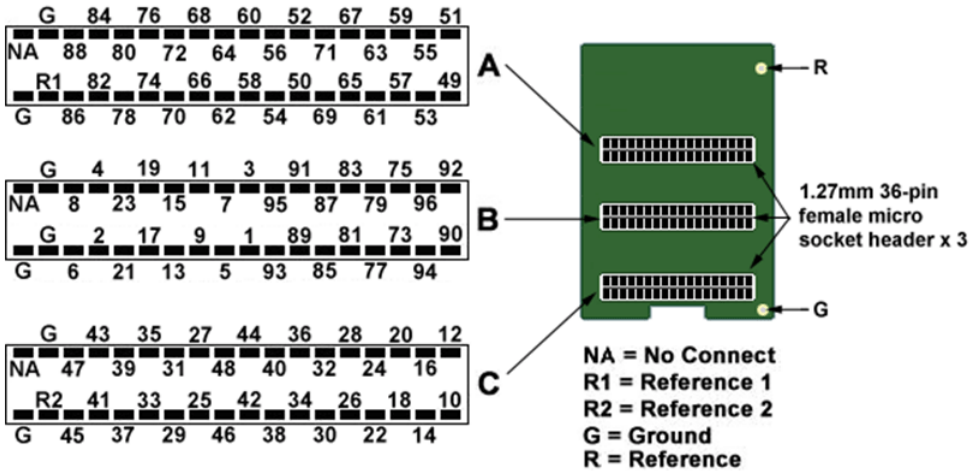
Pinouts are looking into the connector and reflect the preamplifier channels.



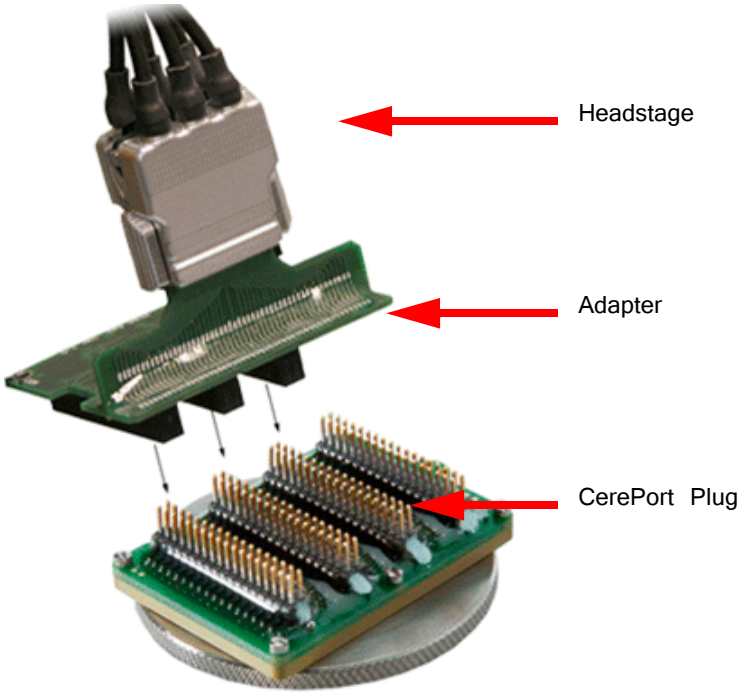
Use jumper to choose which reference (R1, R2, R3) to use for all channels. Only one reference may be selected.

ZCA-CK96A ZIF-Clip® Headstage to 96-Channel Chronic Probe

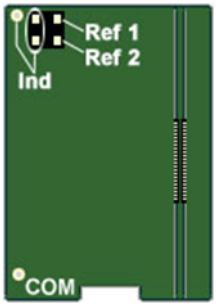
The ZCA-CK96A adapter connects a 96-channel chronic CyberKinetics CerePort connector to a 96-channel ZIF-Clip® headstage. For single-ended operation, tie the ground and reference pins (shown in diagram) together.



Pinouts are looking into the connector and reflect the preamplifier channels.



ZCA-CK96A Connection Diagram.



A four-pin header located on the backside of the adapter is provided for access to two probe reference pins. These pins are separate references and are connected internally to the adapter.

Connecting a jumper between the headstage reference pins (Ind) and either of the probe reference pins (Ref1 or Ref2) connects the headstage reference to the desired probe reference (see table below for more information).

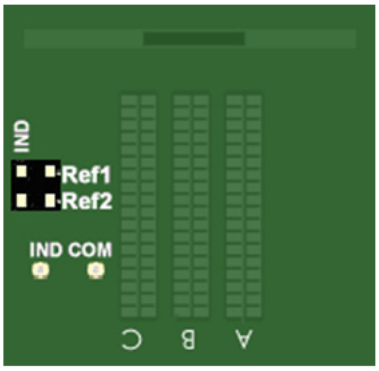
Jumper Configuration

The following table describes the jumper configurations for the ZCA-CK96A.

Jumper Connections	Operation
Ind Ref_1 Ind Ref_2	Headstage Ground and Reference separated and Ref_1, Ref_2 pins are not used, yielding referential amplification of signals relative to the voltage of the Reference (Ind). An external connection for the headstage reference (Ind) must be used for referential amplification.
Ind Ref_1 Ind Ref_2	Shorts headstage Reference input (Ind) to the pin labeled Ref_1 (a low impedance site on the probe) yielding referential amplification of signals relative to the voltage of the Ref_1 site.
Ind Ref_1 Ind Ref_2	Shorts headstage Reference input (Ind) to the pin labeled Ref_2 (a low impedance site on the probe) yielding referential amplification of signals relative to the voltage of the Ref_2 site.

ZCA-ICS96 ZIF-Clip® Headstage to 96-Channel Chronic Probe

The ZCA-ICS96 adapter connects a 96-channel acute CyberKinetics ICS-96 connector to a 96-channel ZIF-Clip® headstage. Banks A, B and C are labeled on the adapter and can be matched with the ICS-96 electrode sockets for correct alignment when plugging the two together.



A four-pin header located on the top of the adapter is provided for access to the REF1 and REF2 probe reference pins used by the ICS-96. Connecting a jumper between the **headstage** reference pins (IND) and either of the **probe** reference pins (REF1 or REF2) connects the headstage reference to the desired probe reference (see table below for more information).

For single-ended operation, solder the headstage ground (COM) and headstage reference (IND) solder points together.

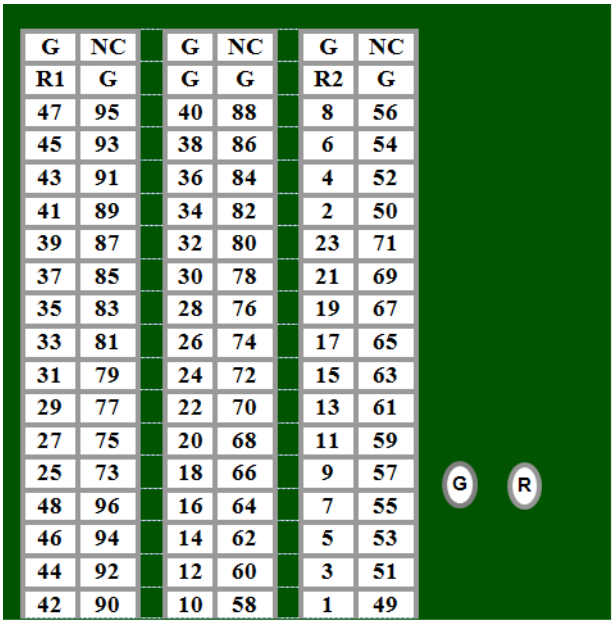
Jumper Configuration

The following table describes the jumper configurations for the ZCA-ICS96.

Jumper Connections	**Operation**
IND REF_1 IND REF_2	Headstage Ground and Reference separated and REF_1, REF_2 pins are not used, yielding referential amplification of signals relative to the voltage of the Reference (IND). An external connection for the headstage reference (IND) must be used for referential amplification.

IND REF_1 IND REF_2	Shorts headstage Reference input (IND) to the pin labeled REF_1 (a low impedance site on the probe) yielding referential amplification of signals relative to the voltage of the REF_1 site.
ND REF_1 IND REF_2	Shorts headstage Reference input (IND) to the pin labeled REF_2 (a low impedance site on the probe) yielding referential amplification of signals relative to the voltage of the REF_2 site.

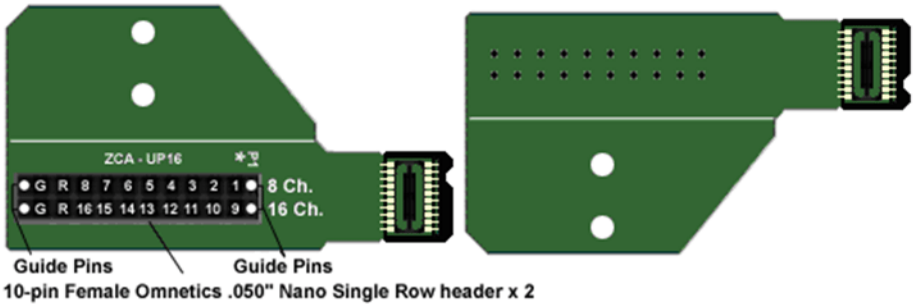
Pinouts



Pinouts are looking into the connector and reflect the preamplifier channels.

ZCA-UP16 16-Channel Plextrode® U-Probe to ZIF-Clip headstage

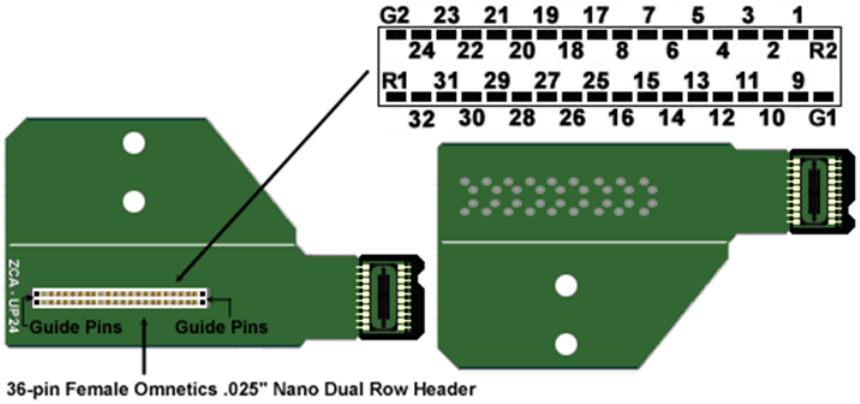
The ZCA-UP16 adapter connects an 8 or 16-channel acute Plextrode® U-Probe connector to a 16-channel ZIF-Clip® headstage. The adapter includes mounting holes for attachment to a micromanipulator. Configuration for single-ended or referential operation is provided on the electrode. Refer to the Plextrode documentation for jumper configurations.



Pinouts are looking into the connector and reflect the preamplifier channels.

ZCA-UP24 24-Channel Plextrode® U-Probe to ZIF-Clip headstage

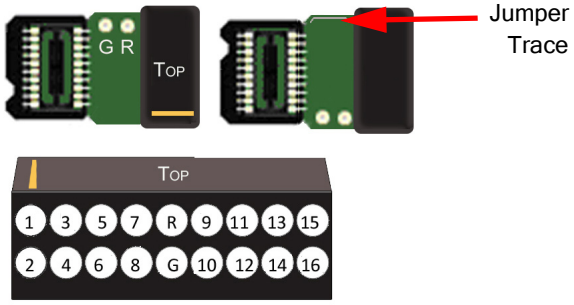
The ZCA-UP24 adapter connects a 24-channel acute Plextrode® U-Probe connector to a 32-channel ZIF-Clip® headstage. The adapter includes mounting holes for attachment to a micromanipulator. Configuration for single-ended or referential operation is provided on the electrode. Refer to the Plextrode documentation for jumper configurations.



Pinouts are looking into the connector and reflect the preamplifier channels.

ZCA-MIL16 ZIF-Clip® Headstage to Mill-Max connector (16 Channels)

The ZCA-MIL16 adapter connects a 18-channel Mill-Max based probe to a 16-channel ZIF-Clip® headstage. By default, the inputs are single ended, with Reference (R) and Ground (G) tied together. To make the inputs referential, sever the jumper trace on the board between R and G (shown below).



Pinouts are looking into the connector and reflect the preamplifier channels.

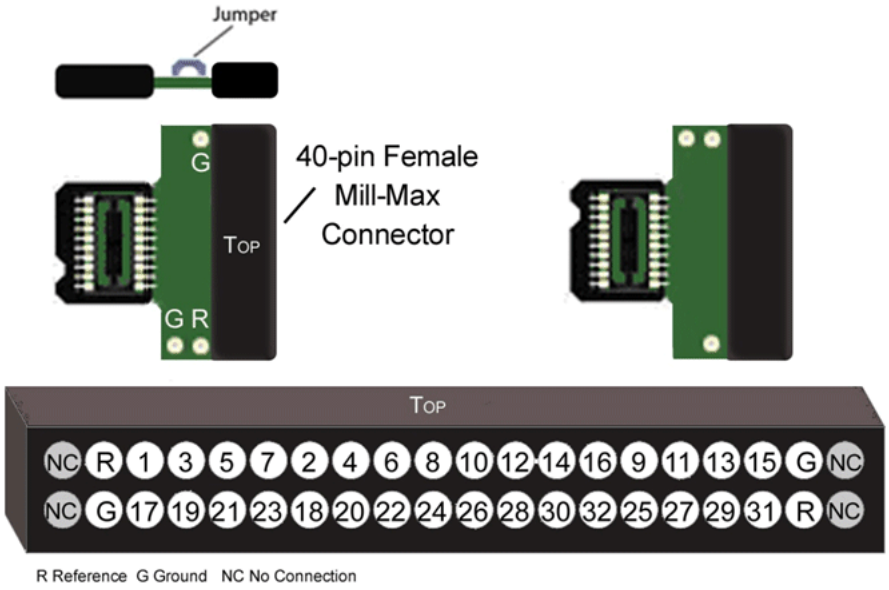
Mill-Max Connector Specifications:

Pitch: 0.050" (1.27 mm)

Row Spacing: 0.050" (1.27 mm)

ZCA-MIL32 ZIF-Clip® Headstage to Mill-Max connector (32 Channels)

The ZCA-MIL32 adapter connects a 32-channel Mill-Max based probe to a 32-channel ZIF-Clip® headstage. By default, the inputs are single ended, with Reference (R) and Ground (G) tied together. To make the inputs referential, cut the jumper between R and G (shown below).



Pinouts are looking into the connector and reflect the preamplifier channels.

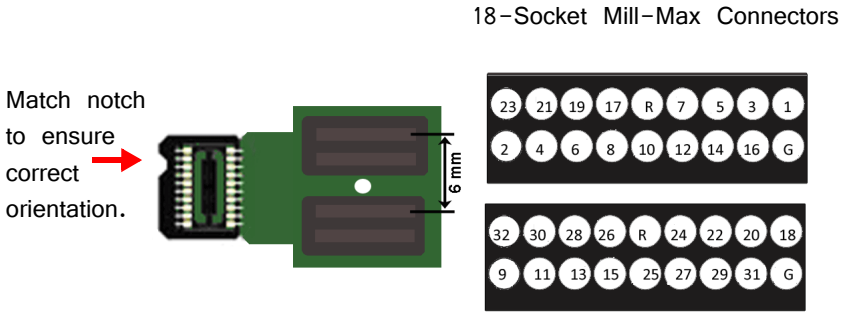
Mill-Max Connector Specifications:

Pitch: 0.050" (1.27 mm)

Row Spacing: 0.050" (1.27 mm)

ZCA-VD8 ZIF-Clip® Headstage to Versa Drive connector (32 Channels)

The ZCA-VD8 adapter connects a Versa Drive (Versa-8 Optical) via two Mill-Max connectors to a 32-channel ZIF-Clip® headstage.



Pinouts are looking through the connector and reflect the preamplifier channels.

Mill-Max Connector Specifications:

Pitch: 0.050" (1.27 mm)

Row Spacing: 0.050" (1.27 mm)

Connector to Connector Specification:

Pitch: 0.236" (6 mm), Pin 1 to Pin 18

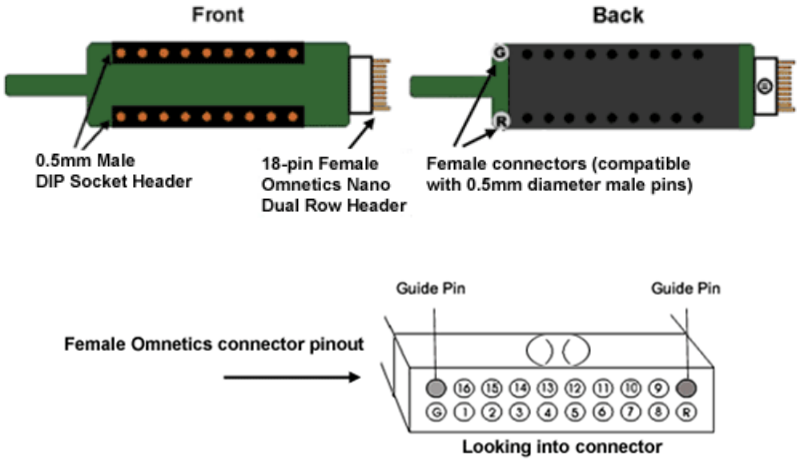
Probe Adapters

Adapters Overview

Each TDT headstage is designed for use with a particular style of probe. Probe adapters allow each headstage to be used with a wider variety of probes. When using adapters, keep in mind that standard operation (referential vs single ended) varies for acute and chronic preparations and headstages are designed accordingly. When adapting across preparations, carefully note and understand the use of the ground (G) and reference (R) connections provided on each adapter.

AC-CH Acute Headstage to Chronic Probe (16 Channels)

The AC-CH adapter allows the user to connect a 16-channel chronic probe (such as a TDT 16 channel microwire array) to an acute TDT headstage (RA16AC/ RA16AC4). Standard operation for chronic preparations is single ended with ground and reference shorted together in the chronic headstage. However, the acute headstage is designed for referential operation. When using the acute headstage with our microwire arrays, short G and R together on the adapter for single ended operation.

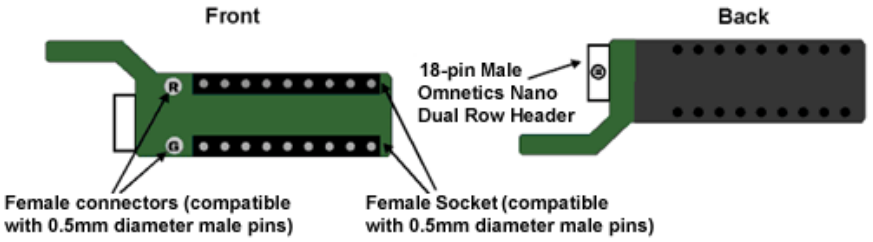


Pinouts are looking into the connector and reflect the preamplifier channels.

TDT probe adapters are designed for specific TDT headstage to probe connections. If you are using a third party headstage, please contact TDT support for assistance.

CH-AC Chronic Headstage to Acute Probe (16 Channels)

The CH-AC adapter connects a 16-channel acute probe to a TDT chronic headstage (RA16CH). Reference and ground are tied together by default on the chronic headstage so in general only one pin connection is necessary. A jumper is provided on the RA16CH for referential operation. See "RA16CH/LP16CH/LP16CH-ZNF - 16 Channel Chronic Headstage" on page 11-44, for information.

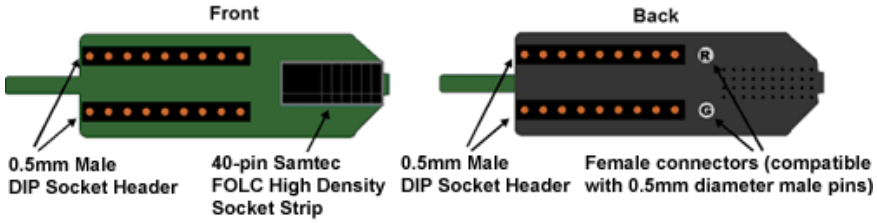


Pinouts are looking into the connector and reflect the preamplifier channels.

TDT probe adapters are designed for specific TDT headstage to probe connections. If you are using a third party headstage, please contact TDT support for assistance.

ACx2-NN 16 Channel Acute Headstage to 32 Channel Acute Probe

The ACx2-NN adapter connects a 32-channel acute NeuroNexus probe to two 16-channel acute TDT headstages (RA16AC/RA16AC4). Standard operation with the NeuroNexus probe is referential. If you wish to use the Reference pad on the probe, do not tie G and R together.



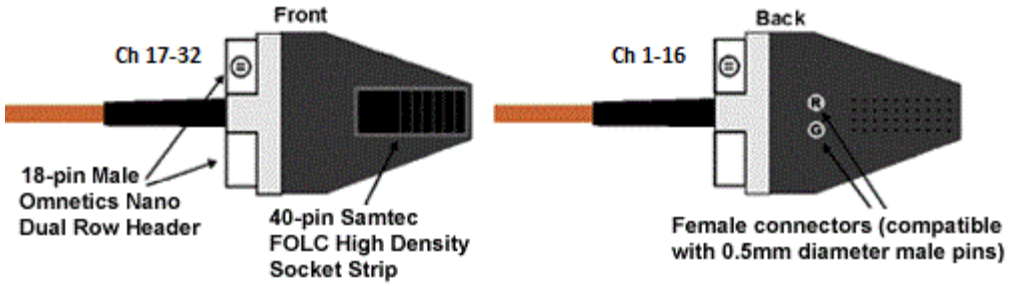
Pinouts are looking into the connector and reflect the preamplifier channels.

TDT probe adapters are designed for specific TDT headstage to probe connections. If you are using a third party headstage, please contact TDT support for assistance.

Important! When using these adapters with NeuroNexus probes, keep in mind that there are several versions of each of the probes. TDTs ACx2-NN is designed for use with Rev 2 of the 32-channel NeuroNexus acute probe. Check the NeuroNexus website for pin diagrams. Also see MCMap in the *RPvdsEx User Guide*, for a description and examples on how to re-map channel numbers.

CHx2-NN 16 Channel Chronic Headstage to 32 Channel Acute Probe

The CHx2-NN adapter connects a 32-channel acute NeuroNexus probe to two 16-channel chronic TDT headstages (RA16CH). Connect the first RA16CH headstage (channels 1-16) to the front of the adapter. Connect the second RA16CH (channels 17-32) to the back of the adapter. This adapter also features a holding rod for connection to a micromanipulator. As with the CH-AC adapter, reference and ground are tied together by default on the chronic headstage so in general only one pin connection is necessary. If you wish to use the Reference pad on the probe, do not tie G and R together and cut the jumper on each headstage to make the inputs referential. See "RA16CH/LP16CH/LP16CH-ZNF - 16 Channel Chronic Headstage" on page 11-44, for more information.



Pinouts are looking into the connector and reflect the preamplifier channels.

TDT probe adapters are designed for specific TDT headstage to probe connections. If you are using a third party headstage, please contact TDT support for assistance.

Important! When using these adapters with NeuroNexus probes, keep in mind that there are several versions of each of the probes. TDTs CHx2-NN is designed for use with Rev 2 of the 32-channel NeuroNexus acute probe. Check the NeuroNexus website for pin diagrams. Also see MCMap in the *RPvdsEx Manual*, for information on how to re-map channel numbers.

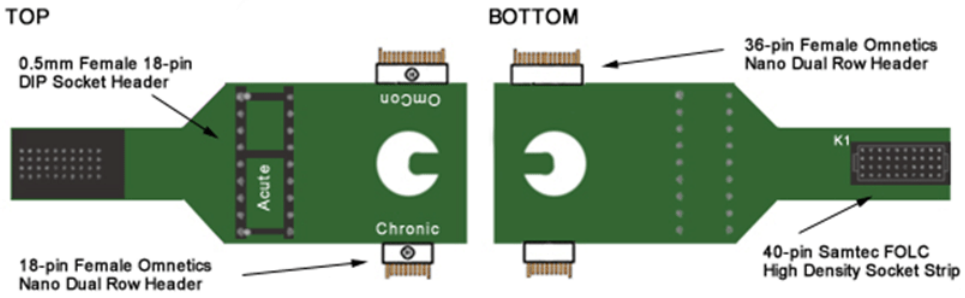
nanoZ-OMN/DIP nanoZ™ to Omnetics and DIP Based Probes

The nanoZ-OMN/DIP adapter allows the user to connect an Omnetics or DIP based probe to a nanoZ™ impedance tester. Connectors are labeled on the circuit board for easy identification.

The K1 connector on the bottom of the adapter is used to connect the nanoZ™ to **one** of the following:

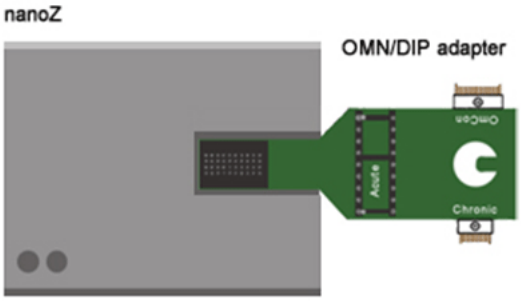
- The **Chronic** connector is a dual row 18-pin Omnetics nano connector that is used with a 16-channel chronic probe, such as a TDT 16-channel microwire array.
- The **OmCon** connector is a dual row 36-pin Omnetics nano connector that is used with a 32-channel chronic probe.
- The **Acute** connector is a 0.5mm female 18-pin DIP socket that is used with a 16-channel DIP-based probe, such as a 16-channel acute Neuronexus probe.

Important! The corresponding channels from each probe connection are tied together, so that channel 1 of the Chronic connector, the OmCon connector, and the Acute connector are all tied to channel 1 of the nanoZ™ connector. See pinouts below for more detail.

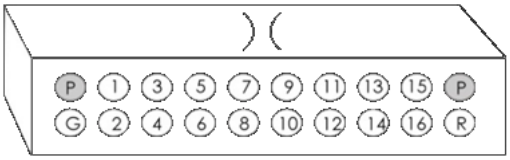


Connecting the Adapter to the nanoZ™

After configuring the nanoZ™ impedance tester as directed in the nanoZ™ User Manual, connect the adapter to the Samtec connector closest to the center, ensuring it is firmly seated. The adapter should cover both nanoZ™ Samtec connectors (as shown below).

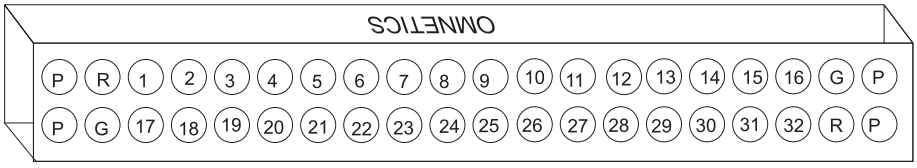


Chronic Pinout



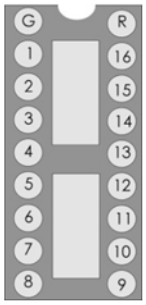
18-pin female Omnetics nano dual row header (pinout looking into the connector)

OmCon Pinout



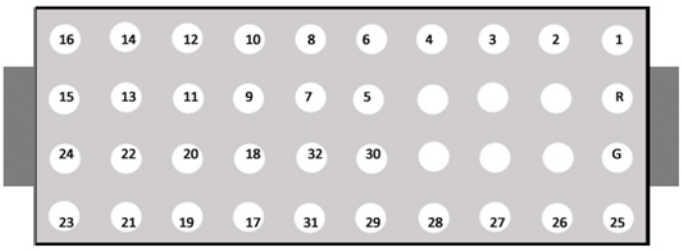
36-pin female Omnetics nano dual row header (pinout looking into the connector)

Acute Pinout



0.5 mm female 18-pin DIP socket header (pinout looking into the connector)

K1 Pinout



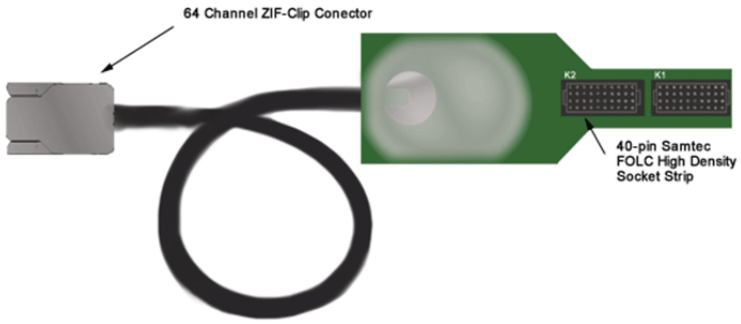
40-pin Samtec FOLC high density socket strip (pinout looking into the connector)

nanoZ-ZCA32/ZCA64 nanoZ™ to ZIF-Clip® Probes

The nanoZ-ZCA32 and nanoZ-ZCA64 adapters allow the user to connect a nanoZ™ impedance tester to a 32- or 64-channel ZIF-Clip® probe.

The nanoZ-ZCA32 K1 connector is used to connect the nanoZ™ to a 32-channel chronic probe, such as a TDT 32-channel ZIF-Clip® microwire array.

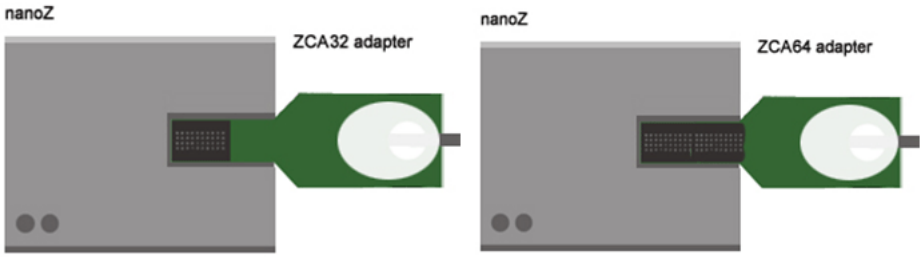
The nanoZ-ZCA64 K1 and K2 connectors are used to connect the nanoZ™ to a 64-channel chronic probe, such as a TDT 64-channel ZIF-Clip® microwire array.



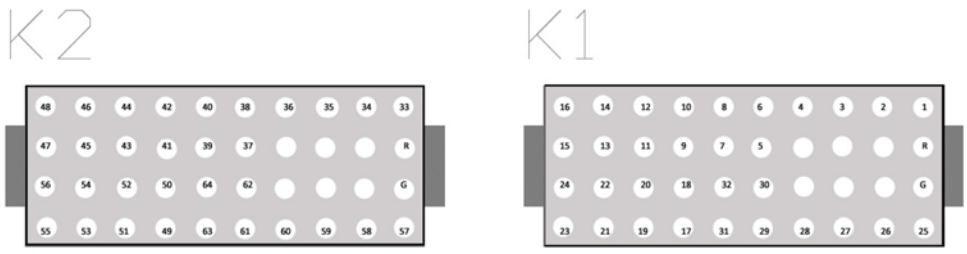
See "ZIF-Clip® Analog Headstages" on page 11-3, for more information on ZIF-Clip® connectors.

Connecting the Adapter to the nanoZ™

After configuring the nanoZ™ impedance tester as directed in the nanoZ™ User Manual, connect the adapter so that both nanoZ™ Samtec connectors (as shown below). Ensure that it is firmly seated. The nanoZ-ZCA32 should connect to the Samtec connector closest to the center of the nanoZ™.



K1 and K2 Pinouts



40-pin Samtec FOLC high density socket strips (pinouts looking into the connector)

Splitters

S-BOX - Amplifier Input Splitter

The S-BOX is a 32-channel passive signal splitter for use with the PZ3 Low Impedance Amplifier. The splitter provides a simple and effective means of routing low impedance biological signals to both a TDT acquisition system and a parallel recording system.

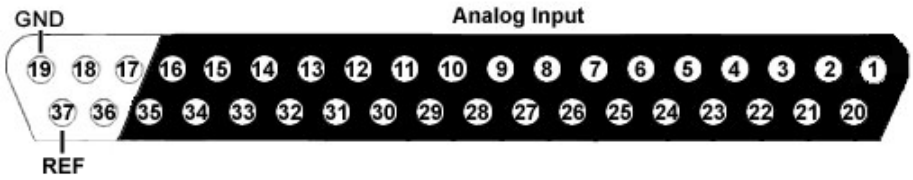
Four DB26 output connectors provide direct connection to a PZ3 amplifier and a single DB37 provides a parallel output connection. Bank letters as well as channel number ranges are labeled on all the DB26 connectors (i.e. Bank A Channels 1-8).

Important! The S-BOX is NOT FDA approved.

The splitter uses standard 1.5 mm safety connectors for input from electrodes. Front panel numbering of these inputs corresponds to TDT amplifier channels in Shared Differential mode.

Important! The S-BOX DOES NOT support Individual (True) Differential mode. Contact TDT if differential recording is required.

DB37 Pinout



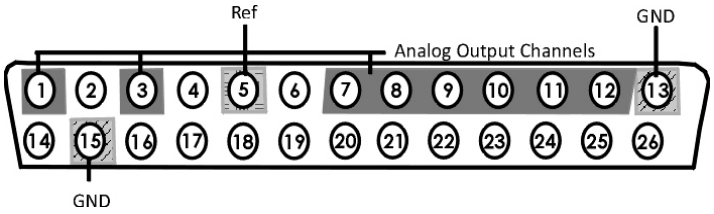
Pin	Name	Description		Pin	Name	Description
1	A1	Analog input channels 1,3,5,7,9,11,13,15,17,19 ,21,23,25,27,29,31		20	A2	Analog input channels 2,4,6,8,10,12,14,16,18, 20,22,24,26,28,30,32
2	A3			21	A4	
3	A5			22	A6	
4	A7			23	A8	
5	A9			24	A10	
6	A11			25	A12	
7	A13			26	A14	
8	A15			27	A16	
9	A17			28	A18	
10	A19			29	A20	
11	A21			30	A22	
12	A23			31	A24	
13	A25			32	A26	
14	A27			33	A28	
15	A29			34	A30	
16	A31			35	A32	
17	NA	Not Used		36	NA	Not Used
18	NA			37	REF	Reference
19	GND	Ground				

Note: No connections should be made to pins 17, 18, and 36.

DB26 Pinout

PZ3 amplifiers have up to 16 26-pin headstage connectors on the back of the unit. The PZ3 channels are marked next to the respective connector on the amplifier. Match S-BOX DB26 Output connectors to the matching connectors on the PZ3.

Pinout Diagram



Note: There are 8 channels per DB26 connector. Bank A is shown. Subsequent banks are indexed by an additional 8 channels.

Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channel		14	NA	Not Used
2	NA	Not Used		15	GND	Ground
3	A2	Analog Output Channel		16	NA	Not Used
4	NA	Not Used		17	NA	
5	Ref	Shared Reference		18	NA	
6	NA	Not Used		19	NA	
7	A3	Analog Output Channels		20	NA	
8	A4			21	NA	
9	A5			22	NA	
10	A6			23	NA	
11	A7			24	NA	
12	A8			25	NA	
13	GND	Ground		26	NA	

S-BOX_PZ5 - Amplifier Input Splitter for the PZ5

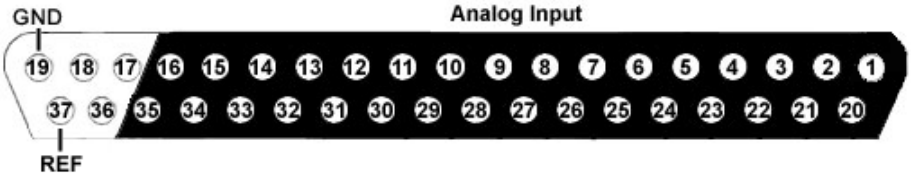
The S-BOX_PZ5 is a 32-channel passive signal splitter for use with the PZ5 Amplifier. The splitter provides a simple and effective means of routing low impedance biological signals to both a TDT acquisition system and a parallel recording system.

Two DB26 connectors provide direct connection to a PZ5 amplifier and a single DB37 provides a parallel output connection. Bank letters as well as channel number ranges are labeled on all the DB26 connectors (i.e. Bank A Channels 1-16).

Important! The S-BOX_PZ5 is NOT FDA approved and is intended for use with the PZ5 Amplifier.

The S-BOX_PZ5 uses standard 1.5 mm safety connectors for input from electrodes. Front panel numbering of these inputs corresponds to TDT amplifier channels.

DB37 Pinout



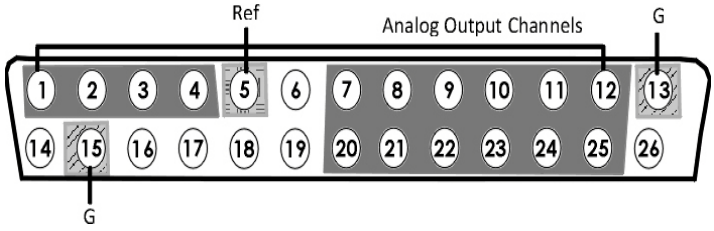
Pin	Name	Description		Pin	Name	Description
1	A1	Analog input channels 1,3,5,7,9,11,13,15,17,19 ,21,23,25,27,29,31		20	A2	Analog input channels 2,4,6,8,10,12,14,16,18, 20,22,24,26,28,30,32
2	A3			21	A4	
3	A5			22	A6	
4	A7			23	A8	
5	A9			24	A10	
6	A11			25	A12	
7	A13			26	A14	
8	A15			27	A16	
9	A17			28	A18	
10	A19			29	A20	
11	A21			30	A22	
12	A23			31	A24	
13	A25			32	A26	
14	A27			33	A28	
15	A29			34	A30	
16	A31			35	A32	
17	NA	Not Used		36	NA	Not Used
18	NA			37	REF	Reference
19	GND	Ground				

Note: No connections should be made to pins 17, 18, and 36.

DB26 Pinout

PZ5 NeuroDigitizers have up to eight 26-pin headstage connectors on the back of the unit. The connectors are labeled alphabetically from bottom to top. The PZ5 can be operated in four different modes. The pinout reflects numbering when using None or Shared Reference Mode. Contact TDT if differential recording is required.

Local, None or Shared Reference Mode



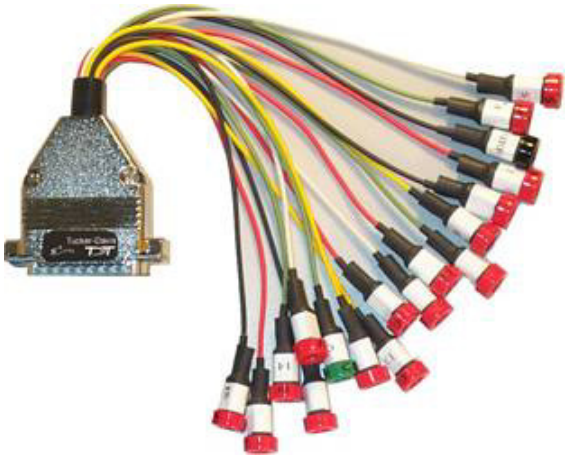
Note: There are 16 channels per DB26 connector. Bank A is shown. Channels in Bank B are incremented by an additional 16 channels.

Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channels		14	NA	Not Used
2	A2			15	GND	Ground
3	A3			16	NA	Not Used
4	A4			17	NA	
5	Ref	Reference		18	NA	
6	NA	Not Used		19	NA	
7	A5	Analog Output Channels		20	A6	Analog Output Channels
8	A7			21	A8	
9	A9			22	A10	
10	A11			23	A12	
11	A13			24	A14	
12	A15			25	A16	
13	GND	Ground		26	NA	Not Used

Connectors

LI-CONN - Low Impedance Connectors

A set of multi-channel low impedance connectors (LI-CONN) for the RA16LI is available for users who do not require a direct connection between the electrodes and the headstage. The LI-CONN uses standard 1.5 mm safety connectors to ensure proper connection between electrodes and the preamplifier.



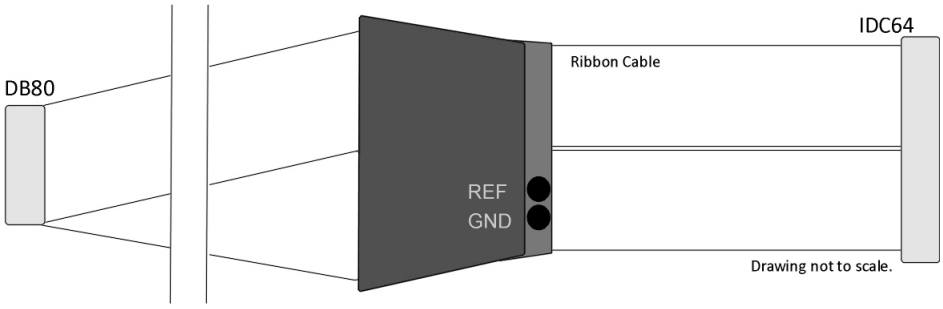
LI-CONN-Z - Low Impedance Connector for the PZ3

The PZ3 is designed to record from low impedance electrodes and electrode caps with input impedance less than 20 kOhm. Signals are input via multiple DB26 connectors on the PZ3 back panel. A break out box or connector(s) is required for electrode connection.

The **LI-CONN-Z** for *Shared Differential* mode features standard 1.5 mm safety connectors and provides easy connections between electrodes and the amplifier.

DB80-I64 PZ5M to I Cable Adapter (64 Channel)

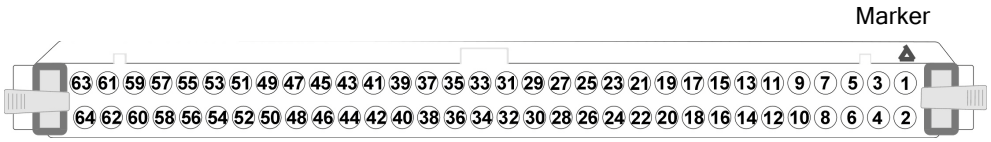
The DB80-I64 adapter connects a standard I connection to a single PZ5M DB80 input connector. Ground and reference are available via standard 1.5 mm touch proof inputs on the polymer bracket. The light-weight bracket reduces tangling near the subject.



DB80-I64 Cable Adapter

The male I connector is keyed to ensure correct connection and includes locking latches to prevent disconnection. The standard length of ribbon cable, from end to end, is 3.6 meters.

I Connector Pinout



Drawing is Looking into the Connector.

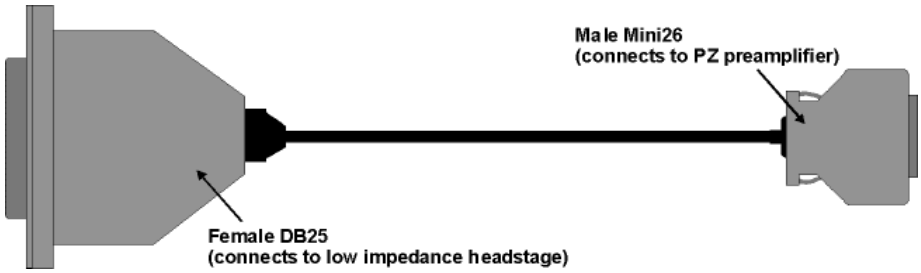
The connector is marked to indicate channel 1. Pins are numbered in the pinout diagram above and reflect amplifier channels.

Preamplifier Adapters

Each TDT headstage is designed for use with either a Legacy or Z-Series preamplifier. Preamplifier adapters allow TDT headstages to be used with a variety of preamplifiers by converting the type of preamplifier connector.

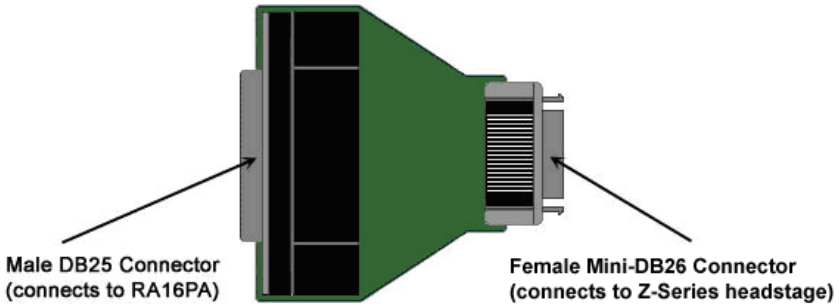
DBF-MiniDBM Low Impedance Headstage to PZ Preamplifier (16-channels)

This adapter connects a low impedance headstage (RA4LI or RA16LI) to a PZ preamplifier.



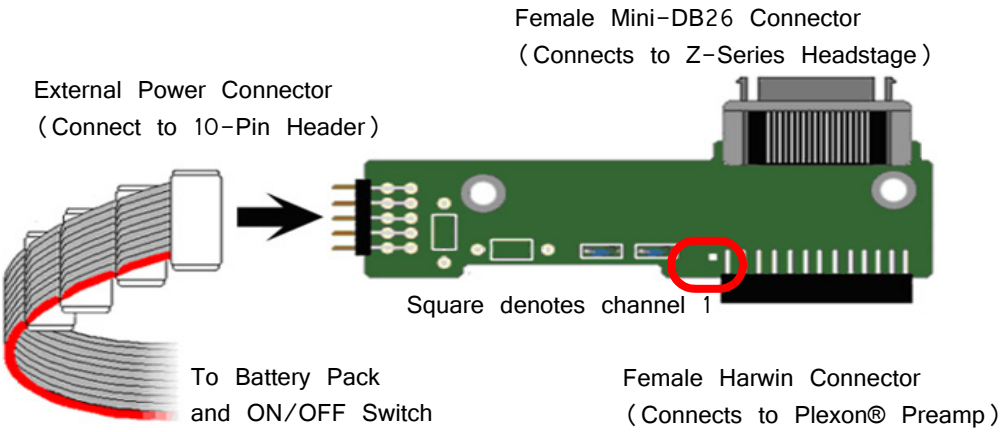
MiniDBF-DBM Z-Series Headstage Female Mini-DB26 to Male DB25 Cable Adapter

This adapter converts a Z-Series headstage Mini-D connector to a DB25 connector for use with a Medusa RA16PA preamplifier.



PLX-ZCA Z-Series Headstage to Plexon® Preamplifier

This adapter connects a Z-Series headstage to a Plexon® preamplifier. Each PLX-ZCA adapter board connects 16-channels. Multiple adapter boards can be stacked for a higher channel count and are fastened together using two screws on either side of the adapter board. An external power source is provided to power the headstage.



External Power Source Connector and a Single PLX-ZCA Adapter Board

External Power Source

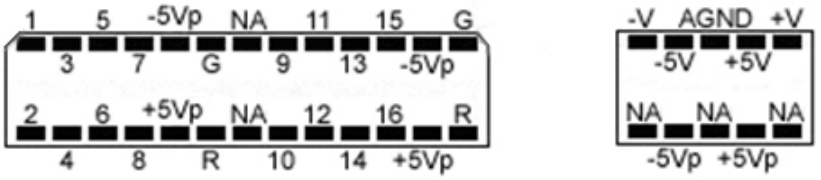
In order to power TDT headstages when using this adapter, an external power source is required. Each external power source includes four connectors and can power up to four PLX-ZCA adapter boards. The external power source uses two 1.5 V D batteries and is enabled through a simple ON/OFF switch.

To power the PLX-ZCA adapter:

1. Align the red colored stripe to the Harwin connector side of the adapter (as shown in the diagram above).
2. Connect an external power connector to the 10-pin header located on the adapter.
3. Ensure that the batteries are correctly inserted in the battery pack then move the switch to the ON position.

Note: To power multiple PLX-ZCA adapters, simply connect each 10-pin header to one of the available external power connectors.

Plexon Header Pinout



Harwin Connector

10-Pin Header
(For external power connector)

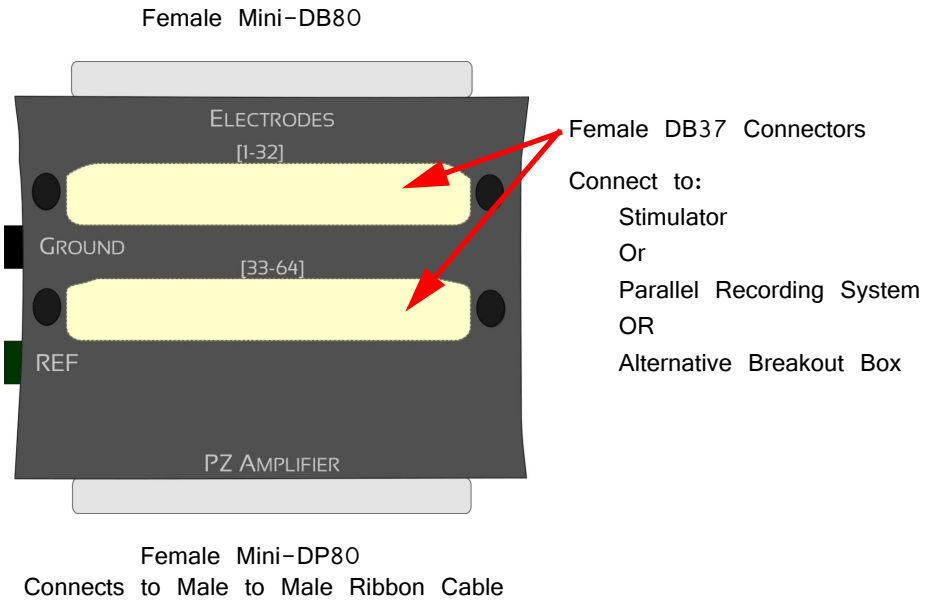
NA = Not Used, G = AGND, R = Reference

Pinouts are looking into the connector and reflect the preamplifier channels.

SB64 64-Channel Stimulator Buffer

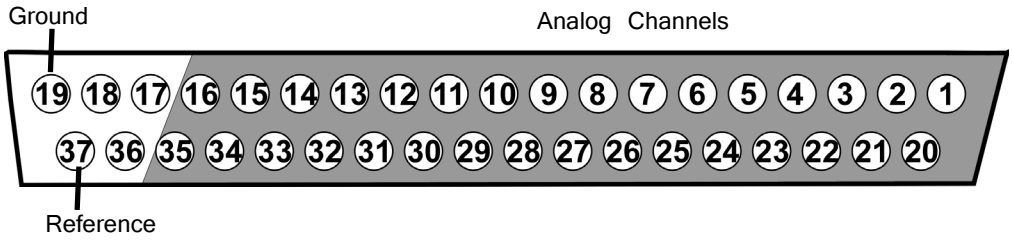
This adapter provides multiple ways of connecting up to 64-channels. Two mini-DB80 connectors, one for direct connection to a PZ5M NeuroDigitizer/Amplifier and one for connection to up to 64 electrode channels. Two DB37 connectors provide an additional passive input or output connection. Each DB37 is tied to the corresponding 32 electrode channels and is buffered from the active electronics associated with the PZ amplifier connection. They can be used to connect stimulation to the corresponding electrodes, pass electrode signals to a parallel recording system, or serve as an alternative input connection from a breakout box (such as a a Xltek EMU128FS).

The SB64 uses standard 1.5 mm safety connectors for Ground and Reference (REF) connections. Front panel numbering of the DB37 connectors corresponds to TDT amplifier channels. Use caution to avoid miswiring.



Pinout Diagrams

(1-32) DB37 Connector



Pin	Name	Description		Pin	Name	Description
1	A1	Analog input channels 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31		20	A2	Analog input channels 2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32
2	A3			21	A4	
3	A5			22	A6	
4	A7			23	A8	
5	A9			24	A10	
6	A11			25	A12	
7	A13			26	A14	
8	A15			27	A16	
9	A17			28	A18	
10	A19			29	A20	
11	A21			30	A22	
12	A23			31	A24	
13	A25			32	A26	
14	A27			33	A28	
15	A29			34	A30	
16	A31			35	A32	
17	NA	Not Used		36	NA	Not Used
18	NA			37	REF	Reference
19	GND	Ground				

Note: No connections should be made to pins 17, 18, and 36.

(33-64) DB37 Connector

Increment above channel numbers by 32.

Electrodes Mini-DB80

The pinout for this connector duplicates the map of the PZ5M Input Connectors and is dependent on the NeuroDigitizer reference mode. See the PZ5M “Input Connectors” on page 7-53.

Part 14: Microwire Arrays

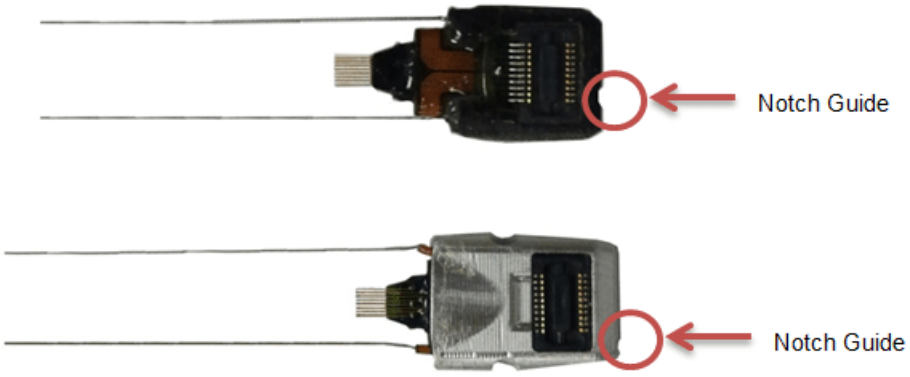
ZIF-Clip® Based Microwire Arrays

ZIF-Clip® microwire arrays are made to user specifications. All arrays use polyimide-insulated tungsten microwire which yield excellent recording characteristics and ample rigidity to facilitate insertion.

The standard ZIF2010 resin form factor array consists of sixteen channels configured in two rows of eight electrodes each. The ZIF2012-AL adds an aluminum shroud to provide increased durability. Both types of probes connect to our ZIF-Clip® headstage. When determining insertion spacing between two or more arrays, be sure to consider the headstage dimensions to ensure sufficient clearance.

Note: This section provides information specific to TDT arrays. For more general information see "Suggestions for Microwire Insertion" on page 14-11.

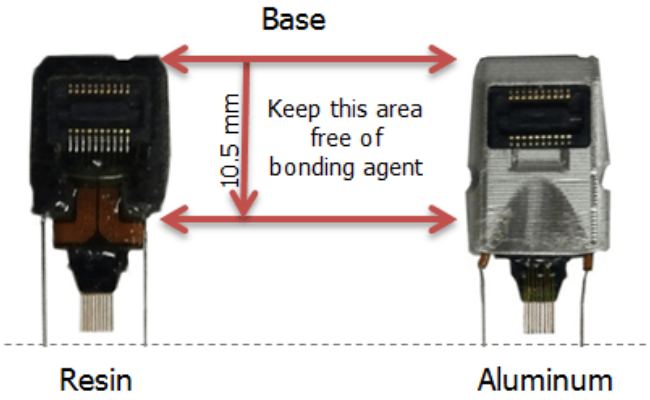
Connecting to a Headstage



A notch at the base of the array facilitates proper connection to the ZIF-Clip® headstage and can help the user identify the correct mapping of electrodes. Ensure that the notch side is properly aligned with the arrow symbol on the headstage. See "Adapter and Probe Connection " on page 11-4, for images and instructions.

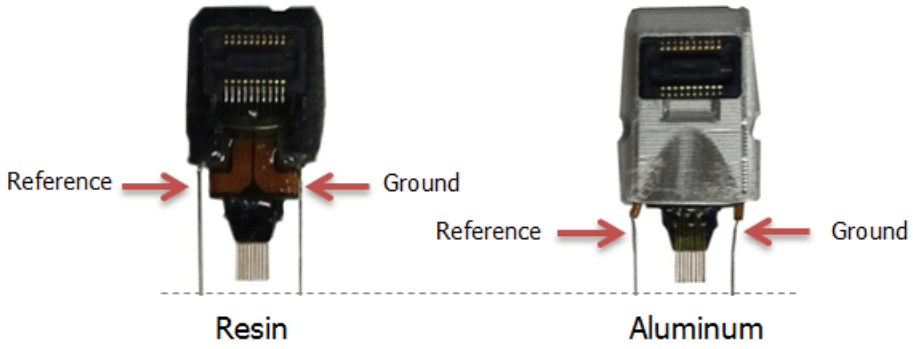
Bonding the Arrays

After insertion, ensure acrylic or other bonding agent does not come into direct contact with the active circuitry. Bonding agents can cause permanent damage to the array. There should be no bonding agent closer than 10.5 mm to the base.



Grounding the Electrode

The images below show the possible connections made for reference or ground wires. These wires are attached at TDT.



⚠ Caution! The ZIF resin (no-aluminum shroud) microwire arrays can be damaged by extreme heat. Use caution when soldering.

ZIF-Clip® Based Microwire Array Specifications

Specifications might vary based on custom order:

Specification	Default	Options
n Rows X n Electrodes	2X8	Max channels per connector = 64
Metal	Tungsten	
Wire Diameter	50 μm	33 μm
Insulation	Polyimide	
Electrode Type	Standard	Flex Ribbon
Flex Ribbon Site Specification	Attached	Separated

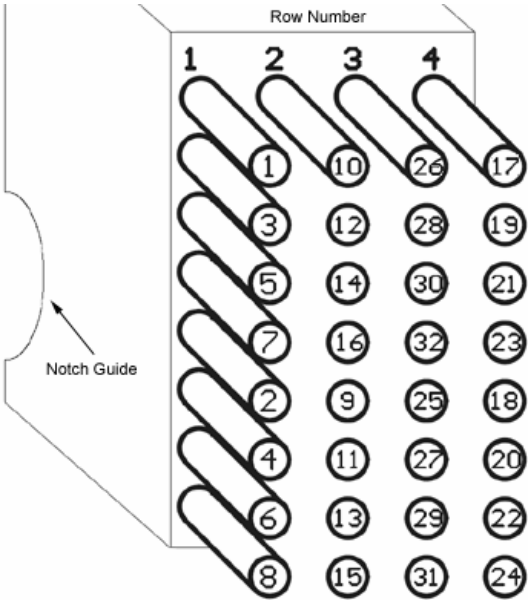
Specification	Default	Options
Electrode Spacing	250 μm	500 μm
Row Separation	375 μm	
Tip Angle	Blunt Cut (0 degrees)	30, 45, 60 degrees
Tip Length	2mm	0.5 - 10 mm
Ground and Reference Wires	Referential	Single-Ended

See the *Online Order Form* for more information on ordering specifications.

ZIF-Clip® Based Microwire Array Site Map

The following diagrams illustrate the site map configurations for 16, 32, and 64 channel ZIF-Clip® based microwire arrays. Site numbers reflect the site map or channel output to a TDT amplifier from the ZIF-Clip® based microwire array (when connected with a ZIF-Clip® headstage).

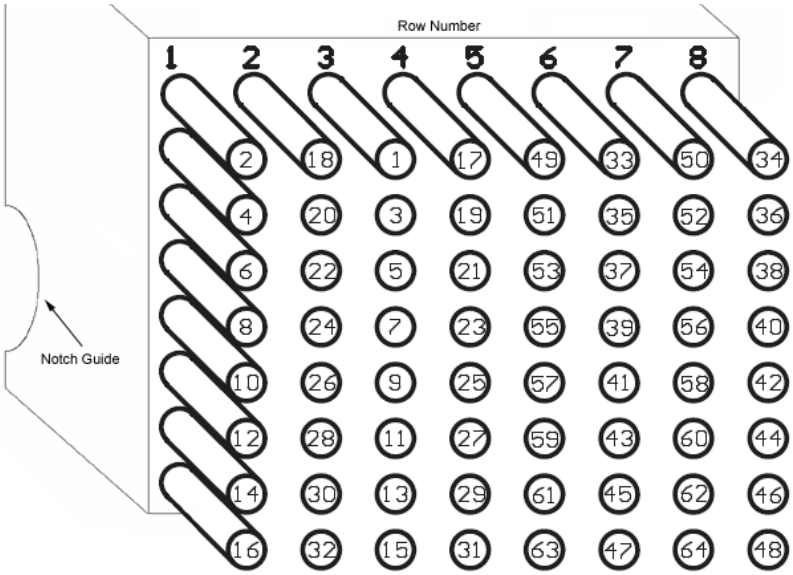
16 and 32 Channel ZIF-Clip® Microwire Arrays



(looking into array)

Note: 16 channel ZIF-Clip® based microwire arrays contain only the first 2 rows.

64 Channel ZIF-Clip® Microwire Array



(looking into array)

ZCAP - Aluminum ZIF-Clip® Cap

Part Number: ZCAP, ZL-CAP

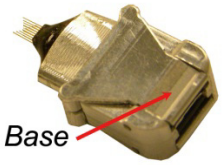
The ZIF-Clip® Caps are made of high quality aluminum and are designed to protect the ZIF-Clip® micro connector from potential damage in the absence of the ZIF-Clip® headstage. They can be used with both ZIF-Clip® probe adapters and microwire arrays.

The ZCAPn Standard Cap

The ZCAP fits directly over all resin form factor ZIF-Clip® compatible connectors and features a rubber O-ring for easy handling and grip.

To use the ZCAP:

- Grip it with two fingers and gently slide it onto the ZIF-Clip® micro connector.



To remove the ZCAP:

- Grasp both sides of the O-ring grip and gently pull away from the ZIF-Clip® micro connector until the ZCAP releases from the connector.

The ZL-CAP Locking Cap

The ZL-CAP can only be used with aluminum form factor ZIF-Clip® arrays. It locks onto the shroud to prevent unintentional removal of the cap by the subject when not in use. Aluminum shroud arrays and locking caps are recommended for larger test subjects.

To use the ZL-CAP:

1. Pinch the base with two fingers and gently slide it onto the ZIF-Clip® micro connector.
2. Pinch the opposite end of the connector to engage the locking clamp.

To remove the ZL-CAP:

- Pinch the base with two fingers to open the locking clamp and gently slide it off of the ZIF-Clip® micro connector.

Omnetics Based Microwire Arrays

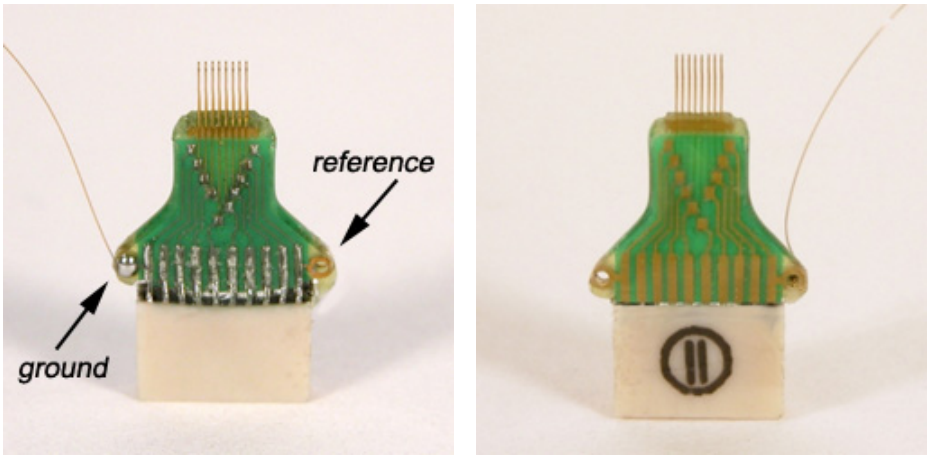
Part Numbers: OMN1010, OMN1005, OMN1020, OMN1030

Standard 50 µm polyimide-insulated tungsten microwire gives the arrays excellent recording characteristics and the rigidity of tungsten facilitates insertion. The standard OMN1010 array consists of sixteen channels configured in two rows of eight electrodes each and are typically accessed via our RA16CH 16-channel headstages. OMN1005, OMN1020, and OMN1030 share this standard configuration with varying electrode separation specifications. Consult the documentation provided with your array for custom specifications.

Grounding the Electrode

Our latest laser cut microwire arrays (OMN1010) have one location each to connect needed ground and reference wires. Because the reference and ground are shorted together in our RA16CH chronic headstages (unless the jumper is cut by the user) only one wire will be needed for most cases.

Important! The solder pad is located on the backside of the microwire circuit board.



Back View ------ Front View

The illustrations above show a single wire connected to the ground pad located on the backside of the array.

⚠ Caution! The microwire array can be damaged by extreme heat. Use caution when soldering.

Specifications might vary based on custom order:

Specification	Default	Options
n Rows X n Electrodes	2X8	Max channels = 32
Metal	Tungsten	
Wire Diameter	50 μm	33 μm
Insulation	Polyimide	
Electrode Spacing	250 μm	175 μm, 350 μm, 500 μm
Row Separation	500 μm	1000 μm, 1500 μm, 2000 μm
Tip Angle	Blunt Cut (0 degrees)	30, 45, 60 degrees
Tip Length	2mm	0.5 - 4 mm
Attached G/R Wires	None	Ground, Reference

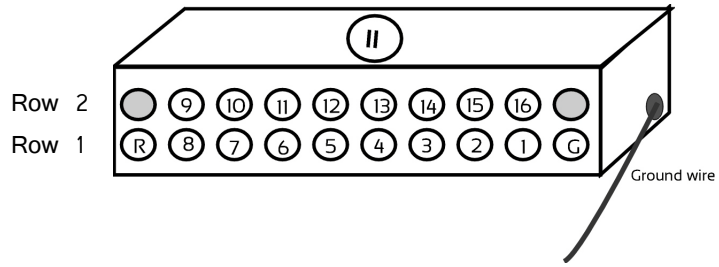
See the *Online Order Form* (PDF format) for more information on ordering specifications.

Pinout Diagram

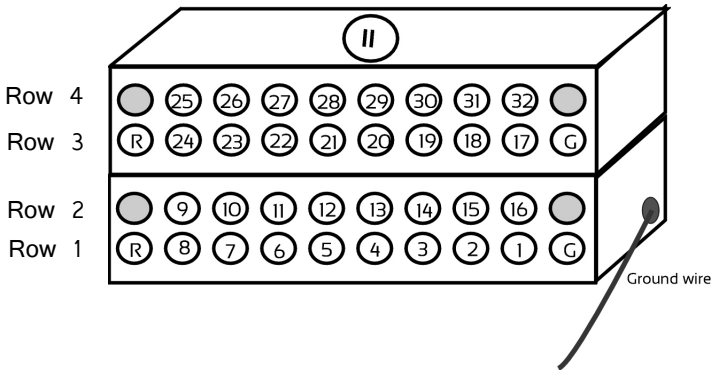
Omnetics dual row 18-pin nano connector(s) (0.025 mil pitch; <2x7x4mm)

Ground wire is attached adjacent to row 1.

16 Channel Connector



32 Channel Connector



Suggestions for Microwire Insertion

I. General Procedures:

The following are general suggestions for insertion of TDT microwire arrays and may not comply with your animal care and use guidelines. Investigators should consult officials at their respective institutions to determine the regulations governing animal care and use in their laboratory.

We use aseptic techniques and avertin anesthesia for mouse, ketamine/xylazine anesthesia for rat.

We use the general procedures for rodent survival surgery described in: "Principles of Aseptic Rodent Survival Surgery: General Training in Rodent Survival Surgery - Part I" In: Laboratory Animal Medicine and Management, Reuter J.D. and Suckow M.A. (Eds.) International Veterinary Information Service, Ithaca NY (www.ivis.org), 2004; B2514.0604.

This can be downloaded from http://www.ivis.org/advances/Reuter/brown1/IVIS.pdf.

NIH offers instructional videos entitled: "Training in Basic Biometholodology for Laboratory Mice" and "Training in Survival Rodent Surgery" at their website: https://olaw.nih.gov/education/training-videos.htm

II. Stereotaxic Surgery:

We use procedures similar to those described in: "Stereotaxic Surgery In The Rat: A Photographic Series" by Richard K. Cooley and C.H. Vanderwolf. This reference is available from Amazon.com for $27.97 and is highly recommended.

III. Microwire Procedures:

General information, pictures, and available configurations for TDT microwire arrays can be found at:

https://www.tdt.com/component/omnetics-based-electrodes/

https://www.tdt.com/component/zif-clip-array-electrodes/

A recent paper by Kralik et al. (2001) contains a very helpful description of microwire array insertion methods (Methods. 2001 Oct; 25(2): 121-50).

In rat and mouse, we recommend following the general and neurosurgical procedures as described in the references above.

We first prepare the subject and perform a craniotomy above the implantation site following the methods of Cooley and Vanderwolf (2004). Implant several skull screws as described in this reference to help bond the dental acrylic and array to

the skull. A base coat of OptiBond FL (Kerr) applied to the skull works well to help bond the dental acrylic. Keep this out of the craniotomy.

For rat and mouse we recommend a durotomy, using the tip of a sterile syringe needle as a micro-scalpel to cut an "X" shaped incision through the dura. Reflect the flaps of dura aside, taking care not to disturb the pia or pial vasculature.

Advance the array to the pial surface using a stereotaxy and check that all electrodes are unobstructed by bone or dura. We have also used the stereotaxy to quickly advance the array through the pia and then to adjust the array to its final depth. This method has worked well for a number of our customers as well.

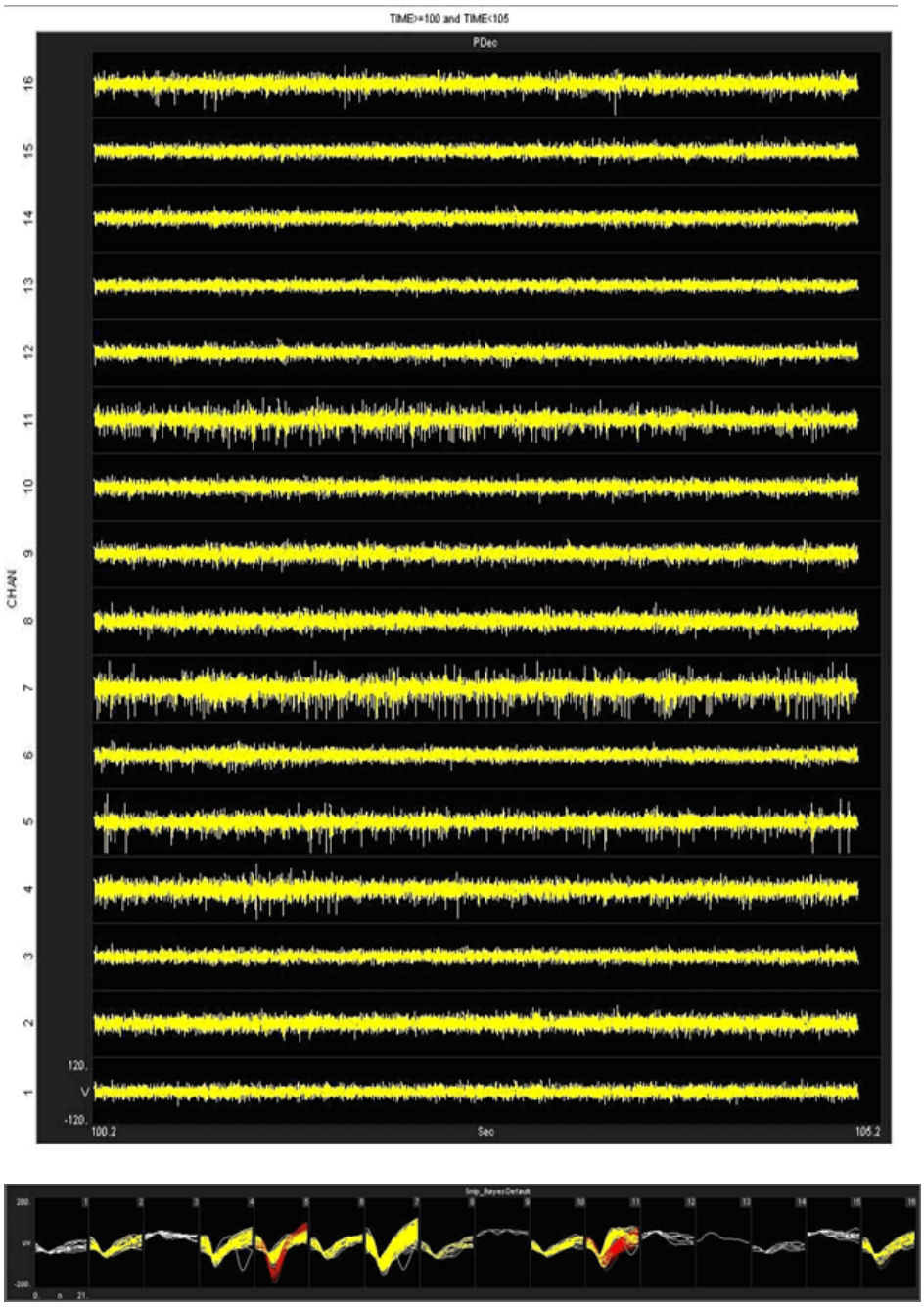
There have been two schools of thought on insertion speed. Fast insertion (e.g. Rousche PJ, Normann RA. Ann Biomed Eng. 1992;20(4):413-22) using an inserter device, and slow insertion (e.g. Nicolelis et al., Proc Natl Acad Sci U S A. 2003 Sep 16;100(19): 11041-6). A recent paper by Rennaker et al., 2004, (J Neurosci Methods. 2005 Mar 30;142(2):169-76) explores the relative merits of each method.

Regardless of which insertion method you choose, advance the array to its desired position, leaving it attached to the stereotaxy until it is fully bonded to the skull with dental acrylic. Prevent CSF from weeping from the craniotomy by gently packing around the array with gelfoam. The CSF will eventually soak through and keep the acrylic around the craniotomy from curing, so perform this step quickly. Bone wax or Kwik-Cast would probably work better than the gelfoam, but we have not used these in our lab to date.

Attach the array to the skull using a thin layer of dental acrylic and the methods described by Cooley and Vanderwolf. Do not build up a large base of acrylic until the ground wire(s) of the array have been attached by wrapping them around the stainless skull screws. Make very sure that the ground wire(s) make good electrical contact to the screws. Pot the entire array/screw complex with dental acrylic using the methods described by Cooley and Vanderwolf.

In our hands, explanted arrays come out of the brain with roughly the same impedance they went in with. Here, recording duration seems to be more limited by surgical technique/capsule formation than by the arrays themselves. We recommend ethylene oxide gas sterilization of the arrays and good sterile surgical technique.

We have obtained good recordings in rat and mouse cortex for several weeks; using only alcohol sterilization of the arrays (we have no access to ethylene oxide). An example from rat with lots of active channels, ~150 µV spikes on ~20 µV background noise is below. We have seen up to ~300 µV spikes on the same noise floor. Our customers have reported recordings durations of several months in rat and monkey.


TIME>=100 and TIME<105
PDec
CHAN
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
120.
V
-120.
100.2
Sec
105.2

Part 15: Attenuator

PA5 Programmable Attenuator

Overview

The PA5 Programmable Attenuator is a precision device for controlling signal levels over a wide dynamic range, providing 0 to 120 dB of attenuation for signals up to 100 kHz in frequency. The device is fully programmable; however, simple manual operation is also available using front panel controls.

When used **programmatically**, the module may be controlled via TDT's ActiveX Controls, as well as any programming environment that supports ActiveX or programs that allow scripts for implementing ActiveX controls, such as Microsoft Access and Excel. For information about how to control the module programmatically, see the *ActiveX Reference Manual*.

When used in manual operation, the attenuation level is adjusted in two modes of operation:

- The *Atten* mode permits the user to adjust the attenuation level of the signal from 0 to 120 dB in increments of 0.1 dB.
- The *UserAtt* mode permits the user to adjust the attenuation level of the signal using user-programmed parameters. Before using the UserAtt mode, attenuation parameters must be set up using the UserOps menu.

Power and Interface

The PA5 Programmable Attenuator is powered via the System 3 zBus (ZB1PS) and requires an interface to the PC (Gigabit, Optibit, or USB). Ensure that the ZB1PS chassis housing the PA5 is connected in the interface loop according to the installation instructions for the interface in use.

Important! The chassis housing the PA5 must be powered and connected to a PC via the PC interface for BOTH manual and programmed operation.

Features

Display

Displays the current level of attenuation being applied to the signal or displays the manual operations menu. During manual operation it is used to set up user-defined attenuation parameters and to obtain descriptions for menu items. See “PA5 Display Icons” on page 15-12, for more information.

(ESC) Button

Exits the manual operations menu items without accepting changes.

SELECT (ENTER) Knob

During manual operation, allows the user to adjust the attenuation applied to the signal. In addition, it allows the user to scroll through the manual operation menus, set up user-defined attenuation parameters, and access descriptions of menu item.

Turn the Select knob to adjust attenuation or view menus. Press and release the knob to make a selection. The module must be in Attn or UserAtt mode to manually adjust attenuation. See “PA5 Manual Operation ” on page 15-4, for more information.

INPUT BNC

Source signal input. The maximum input voltage is +/- 10 V peak.

OUTPUT BNC

Attenuated signal output.

PA5 Manual Operation

Important! The PA5 is powered via the zBus and must be connected to the PC via an interface module during manual operation.

In manual operation, the PA5 is operated using front panel controls. The menu options are viewed by turning the Select knob and entered by pressing and releasing the knob. The module must first be set to Attn or UserAtt mode to manually adjust attenuation.

To access a menu:

- Turn the knob until the name of the desired menu appears on the display, then press and release the knob. The module has two levels of menus.

  Top-level menu items are indicated by a single filled box in the upper left corner of the menu display, and sub-menus are indicated with an additional indicator box for each level. Only the UserOps menu item has sub-menu items. See “PA5 Display Icons” on page 15-12, for more information.

For a definition of each menu item:

- Turn the **Select** knob until the name of the menu appears on the display, then press and hold down the **Select** knob. A description of the menu function will scroll across the display.

To exit a menu without changing settings:

- Press and release the **ESC** button.

Operation in *Atten* Mode

In *Atten* mode, the user sets the desired level of attenuation with the Select knob. When the unit is powered on, it defaults to the Atten mode with 0.0 dB of attenuation.

To use Atten mode:

- Turn the **Select** knob until *Atten* appears on the display, then press and release the **Select** knob.

  A small letter "A" appears in the upper left corner of the display, indicating the unit is in *Atten* mode, and a decibel reading appears on the right side of the display. See "PA5 Display Icons" on page 15-12, for more information.

- Turn the **Select** knob to adjust attenuation in 0.1 dB increments.

Operation in *UserAtt* Mode

In *UserAtt* mode, the user can adjust the attenuation level of the signal using user-programmed parameters available in the *UserOps* menu. Users can also save common parameter configurations in the PA5's nonvolatile memory. See "Using Preset Configurations" on page 15-10, for more information.

To use *UserAtt* mode:

1. Turn the **Select** knob until *UserAtt* appears on the display, then press and release the **Select** knob.

   A small letter "U" appears in the upper left corner of the display, indicating the unit is in *UserAtten* mode, and a decibel reading appears on the right side of the display. See "PA5 Display Icons" on page 15-12, for more information.

2. Turn the **Select** knob to adjust attenuation according the current user programmable parameters (available in the *UserOps* menu). The default settings include a step size of 3.0 dB and dynamic update mode.

   Note: When the Update attenuation parameter is set to Manual, the intensity of the display will dim as the user turns the knob—this indicates that the changes have not been applied to the output signal. The user must press and release the Select knob to apply attenuation changes to the output signal.

To access the UserOps menu:

1. Turn the **Select** knob until ***UserOps*** appears on the display.
2. Press and release the **Select** knob.
3. Set the *UserOps* parameters as desired.

   To set parameters such as step size (StpSize), update mode (Update), minimum attenuation (AbsMin), base attenuation (BaseAtt), and reference value (Refrnce); turn the Select knob to the desired value and then press and release to save changes.

4. To exit any menu without saving parameter changes, press and release the **ESC** button before the settings are saved.

About UserAtten Mode Parameters

In *UserAtten* Mode, the user may set parameters such as step size (*StpSize*), update mode (*Update*), and minimum attenuation (*AbsMin*). The scale can be adjusted using the base attenuation (*BaseAtt*) and reference value (*Refrnce*) parameters. Both base attenuation and reference can be used simultaneously, producing an actual attenuation equal to (*Refrnce*+*BaseAtt*-dial setting). See "PA5 Manual Operation " on page 15-4, for more information.

BaseAtt--Base Attenuation

Adds a fixed attenuation value, shifting the scale down and allowing attenuation to be displayed relative to this base level (useful for calibrating signals played over varying transducers). See "Setting Base Attenuation" on page 15-8, for more information.

StpSize--Step Size

Sets the increments in which attenuation is applied to the signal when using the Select knob.

Refrnce—Reference

Sets a reference value used to "flip" the scale of the display (useful for displaying actual signal level on the front panel of the PA5). May be used only when the intensity of the input signal is known. See "Setting a Reference Value " on page 15-10, for more information.

Update—Update

Determines whether attenuation changes dynamically as the selector knob is turned or only after pressing enter to select the current value.

AbsMin--Minimum Attenuation

Sets the minimum level of attenuation the user can apply to the signal (to avoid accidentally presenting excessively loud signals).

PA5 Manual Operation Menus

To access a menu:

- Turn the knob until the name of the desired menu appears on the display, then press and release the knob. The module has two levels of menus.

  Top-level menu items are indicated by a single filled box in the upper left corner of the menu display, and sub-menus are indicated with an additional indicator box for each level. Only the UserOps menu item has sub-menu items.

For a definition of each menu item:

- Turn the Select knob until the name of the menu appears on the display, then press and hold down the Select knob. A description of the menu function will scroll across the display.

To exit a menu without changing settings:

- Press and release the **ESC** button.

PA5 Top Level Menu

Command	Description
Atten	Sets attenuation from 0.0 to 120.0 dB in 0.1 dB increments. The default setting is 0.0 dB. When Atten is in use, the letter "A" appears on the left side of the display, while the attenuation level appears on the right side of the display.
UserAtt	Sets attenuation based on UserOps settings. Before use, attenuation parameters must be set up via the UserOps sub-menus (see below). The default setting is 0.0 dB. When UserAtt is in use, the letter "U" appears on the left side of the display, while the attenuation level appears on the right side of the display.
UserOps	**Access UserOps submenu** UserOps Sub-menu: ***BaseAtt*** Sets a fixed level of attenuation as a reference. The default setting is 0.0 dB and the range is 0 to 100.0 dB. When BaseAtt is set, a "+" symbol appears on the left side of the display. When used, the attenuation level displayed is relative to BaseAtt. For example, with BaseAtt set to 60.0 dB, the attenuation level will be display from -60.0 dB to 60.0 dB. ***StpSize*** Sets the increments of attenuation. The default setting is 3.0 dB, and the range is 0.1 to 60.0dB. ***Refrnce*** Changes the display so it shows the output signal intensity rather than the attenuation level. This function may be used only when the input signal strength is known. When Refrnce is set, the letter "R" appears on the left side of the display. The default setting is 0.0, and the range is ± 300.0. For example, when Refrnce is set to 136 and the attenuation level set to 0.0 dB, the display shows 136.0. When the attenuation level is adjusted to 30.0 the display shows 106. ***Update*** Determines when attenuation is applied to the signal. When set to Dynamic, attenuation is applied as the Select knob is turned. When set to Manual, attenuation is applied after the Select knob is pressed and released. The default setting is Dynamic. Note that when Update is set to Manual, the attenuation level on the display changes as the Select knob is turned, but the attenuation is not applied to the signal until the Select knob is pressed and released. In this mode, the intensity of the display dims to indicate that the attenuation has not been applied to the signal. ***MinAttn*** Sets the minimum attenuation level for the UserAtt mode. This is used to avoid signals that are too loud for the subject or equipment. The default value is 0.0 dB and its range is 0.0 to 100.0 dB. Note that setting this parameter limits the range of possible attenuation levels. For example, when it is set to 30.0 dB, the range of attenuation is 30 db to 120 dB.

PA5 Top Level Menu

Command	Description
Load PS	Loads one of four preset UserAtt configurations from non-volatile memory. See Save PS (Below). The default is 1 and its range is 1 to 4.
Save PS	Saves the current UserAtt configuration in one of four non-volatile memory buffers. This permits the user to save commonly used UserAtt configurations. The default is 1 and its range is 1 to 4. To save a configuration, first ensure that all UserAtt parameters are set as desired then turn the Select knob until the desired memory location is displayed, and press the Select knob. Saving appears on the display. The preset is ready of use.
Reset	Resets all menu items, including presets, to their default conditions. ***Confirm*** The user must confirm the reset by pressing and releasing the Select knob. While the module is resetting, Reseting appears on the display. The user must confirm the reset by pressing and releasing the Select knob. While the module is resetting, Reseting appears on the display. To exit without resetting, turn the Select knob until Cancel appears on the display and then press and release the Select knob, or press the Esc button. ***Cancel*** Cancels the reset.

Setting Base Attenuation

When operating the PA5 manually in User Attenuation (UserAtt) mode, the Base Attenuation (BaseAtt) parameter can be used to apply a fixed attenuation level to the signal. Any additional attenuation to the signal is displayed relative to this base level within a range of 0 to 120 dB. For example: if the BaseAtt is set to 6 dB, when the user sets the attenuation to 3 dB the actual attenuation applied is 9 dB. This feature can be used to calibrate a number of different experimental setups, attenuating each by a different base attenuation so as to provide identical signal levels when each is set to 0.0 dB UserAtt.

When this feature is in use, a "+" symbol is displayed on the left side of the display. Note that the Base Attenuation and Reference parameters can be used simultaneously. When both of these features are in use, the letter "R" and a "+" symbol are displayed on the left side of the display. See "PA5 Display Icons" on page 15-12, for more information.

To set the base attenuation:

1. Access the *UserAtt* mode, by turning the **Select** knob until *UserAtt* appears on the display, then pressing and releasing the knob.
2. Access the *UserOps* menu, and turn the **Select** knob until *BaseAtt* appears on the display.
3. Press and release the **Select** knob. *0.0 dB* appears on the display.
4. Turn the **Select** knob until the display shows the desired level of attenuation.
5. Press and release the **Select** knob. The level is saved and *BaseAtt* appears on the display.

6. To exit the *UserOps* menu, press and release the **ESC** button again.

Example 1: Adding Speaker Calibration Attenuation

A user wishes to equilibrate the level of stimuli applied to two different loudspeakers. Speaker #2 is 7.3 dB louder at the frequency of interest than speaker #1. This example requires the use of two PA5 programmable attenuators.

To more directly compare thresholds measured with both loudspeakers, set the BaseAtt parameter for speaker #1 to *0.0 dB* and set the *BaseAtt* parameter for speaker #2 to 7.3 dB, so that the signal level delivered for a given *UserAtt* is the same for both loudspeakers. Actual attenuation versus displayed levels is shown in the following table.

Speaker 1: BaseAtt=0			**Speaker 2: BaseAtt = 7.3**	
***UserAtt* Display Value**	**Actual Attenuation**		***UserAtt* Display Value**	**Actual Attenuation**
0	0		-7.3	0
120	120		0	7.3
			112.7	120

Example 2: Multiple Signals of Varying Levels

The base attenuation feature is also useful when working with multiple signals of varying levels. BaseAtt can be configured so the intensity of each signal input is identical at 0.0 dB. When working with three signals 30, 34, and 36 dB SPL, the BaseAtt parameters are set and the actual versus displayed value of attenuation are shown in the table below.

This example requires three PA5 programmable attenuators.

Input Signal	**BaseAtt**	**Displayed Value**	**Actual Attenuation**
36 dB SPL	6.0 db	0	6
		4	10
		6	12
		8	14
34 dB SPL	4.0 dB	0	4
		4	8
		6	10
		8	12
30 dB SPL	0.0 dB	0	0
		4	4
		6	6
		8	8

Setting a Reference Value

The Reference parameter is used to display the intensity of the output signal. This parameter can be used only when the strength of the input signal is known. This serves to "flip" the scale, displaying larger numbers for smaller attenuation values.

When in use, a letter "R" is displayed on the left side of the display. Note that the Base Attenuation and Reference parameters can be used simultaneously. When both of these features are in use, the letter "R" and a "+" symbol are displayed on the left side of the display. See "PA5 Display Icons" on page 15-12, for more information.

To set the Reference parameter:

1. Access the *UserOps* menu, and turn the **Select** knob until *Refrnce* appears on the display.
2. Press and release the **Select** knob. *0.0 dB* appears on the display.
3. Turn the **Select** knob until the display shows the desired level.
4. Press and release the **Select** knob. The reference is saved.
5. To exit the *UserOps* menu, press and release the **ESC** button.

Example 1: Displaying Signal Level in SPL

A user wishes to use the PA5 to display the signal level in dB Sound Pressure Level (SPL) for the frequency of interest. Measurements with a sound level meter show a sound level of 96.4 dB SPL with 0.0 dB of attenuation in the PA5. The user sets the Refrnce parameter to 96.4.

The actual attenuation versus the displayed value is as follows:

Display Value (in dB SPL)	Attenuation
0	96.4
50	46.4
96.4	0

Example 2: Combining Reference and Base Attenuation

When the Reference parameter is set to 110 dB and the Base Attenuation parameter is set to 6.0 dB, the actual attenuation versus displayed value is as follows:

Display Value (in dB SPL)	Attenuation
0	116
50	66
110	6

Using Preset Configurations

The PA5 Programmable Attenuator allows users to save four unique User Operation configurations that may be used in UserAttn mode. These configurations may include any of the UserOps parameters (such as step size, base attenuation, and minimum attenuation). Before a configuration can be loaded, it must be set up via the UserOps menu and saved via the SavePS menu.

Saving Preset Configurations

WARNING: This procedure overwrites the contents of the selected preset location. Be certain that the existing configuration is not needed before continuing.

Before a configuration can be saved, it must be set up via the *UserOps* menu. Once the configuration is set up as desired, save the configuration by performing the following:

1. At any top-level menu, turn the **Select** knob until *SavePS* appears on the display.
2. Press and release the **Select** knob. *Preset-1* appears on the display.
3. Turn the **Select** knob until the desired preset location is displayed and then press and release the **Select** knob.

   Saving appears on the display and then *Atten* appears on the display.

   The configuration is saved.

Loading Preset Configurations

When a configuration has been set up via the *UserOps* menu and saved via the *SavePS* menu, load the configuration by performing the following:

1. Turn the **Select** knob until *LoadPS* appears on the display.
2. Press and release the **Select** knob. *Preset-1* appears on the display.
3. Turn the **Select** knob until the desired preset location is displayed, and then press and release the **Select** knob.

   Loading appears on the display and then *Attn* appears on the display.

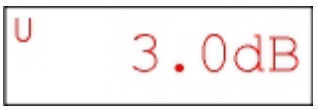
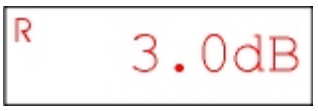
   The configuration is loaded.

PA5 Display Icons

Menu Level Icons

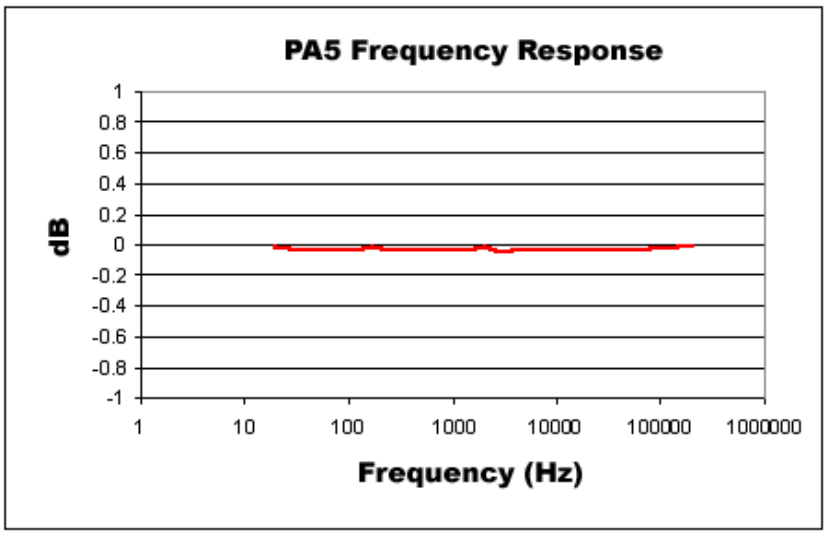
Display	Description
	Single Box: indicates a top-level menu.
	Double Box: indicates a second-level menu.

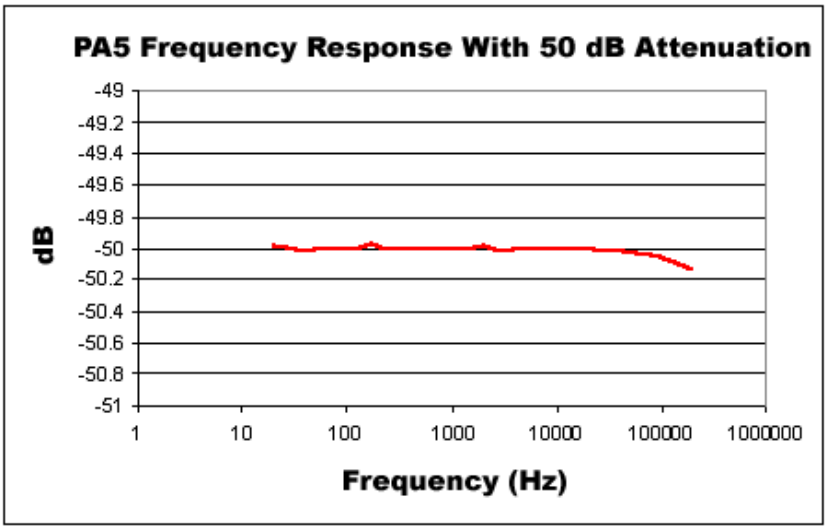
Attenuation Mode Icons

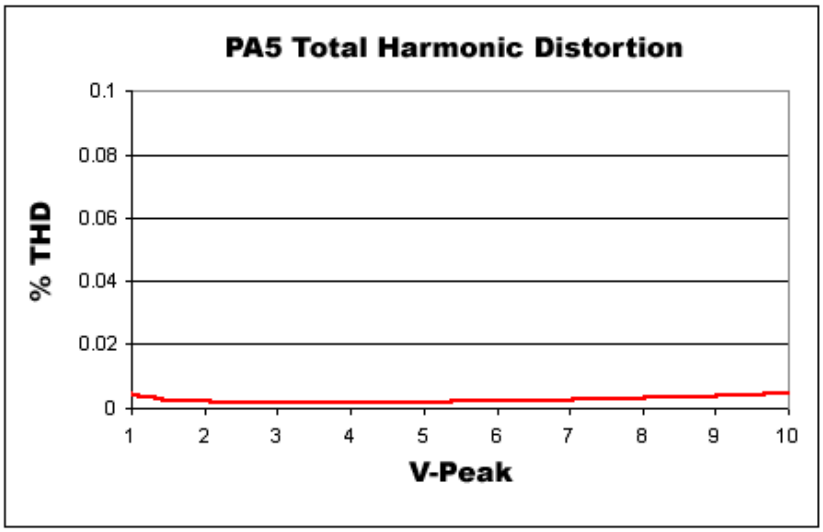
Display	Description
	A: Normal Attenuation Mode
	U: User Attenuation Mode
	U+: User Attenuation Mode. Base attenuation value set.
	R: User Attenuation Mode. Reference level set.
	R+: User Attenuation Mode. Base attenuation value and reference level set.

PA5 Technical Specifications

Input Signal Range	±10V peak
Frequency Range	– 200 kHz
Attenuation Range	0.0 to 120.0 dB
Attenuation Resolution	0.1 dB
Attenuation Accuracy	0.05 dB
Spectral Variation	< 0.04 dB (20Hz to 80 kHz)
Offset	< 10 mV
Signal/Noise	113 dB (20 Hz to 80 kHz at 9.9 V)
Noise Floor	16 μV rms (20 Hz to 80 kHz)
THD	< 0.003% (1kHz tone +/- 7V peak, 0 dB attenuation)
Attenuation Settling Time	5 ms
Switching Transient	< 8 mV (0 Hz to 80 kHz)
Input Impedance	10 kOhm
Output Impedance	10 Ohm




PA5 Frequency Response With 50 dB Attenuation
dB
-49
-49.2
-49.4
-49.6
-49.8
-50
-50.2
-50.4
-50.6
-50.8
-51
1
10
100
1000
10000
100000
1000000
Frequency (Hz)


PA5 Total Harmonic Distortion
% THD
0.1
0.08
0.06
0.04
0.02
0
1
2
3
4
5
6
7
8
9
10
V-Peak

Part 16: Commutators

ACO32/ACO64 Motorized Commutators

Overview

The ACO32 and ACO64 (Active Commutator with Optogenetic stimulation) are motorized commutators that actively track rotation on a headstage cable connected to an awake, behaving subject. They spin the motor to compensate, eliminating turn-induced torque at the subject's end of the cable. The commutator is typically used for systems acquiring neural recordings from up to 32 or 64 channels when using a PZ5 analog amplifier or up to 256 channels or 512 channels when using ZD digital headstages and a PZ5 digital amplifier.

Built-in electrical shielding ensures an ultra-quiet environment for recording and lightweight cables and connectors minimize the torque caused by subject motion. Pushbuttons allow for optional manual control of the commutator motor, and an input BNC can be used to inhibit the motor during critical recording periods. A banana jack provides access to ground, so that users can connect the commutator ground to an external ground, such as a Faraday cage, to minimize ground loops.

Optionally, a fiber optic rotary joint with single-channel optical fiber assembly may be added (shown above) to allow optical targeting and excitation on neural circuits for artifact free stimulation. The optical assembly is user serviceable to allow for easy optical fiber replacement.

Part numbers:

ACO32 — 32 Channel Commutator

ACO64 — 64 Channel Commutator

FORJ — Fiber Optic Rotary Joint and Fiber Optic Cable

Power and Interface

The ACO32 has a rechargeable 1950 mAh Li-ion Battery. The ACO64 has a 3900 mAh battery. A 6-9 V, 3A, center negative adapter (one provided) charges the device. Low battery status is reported only by a decrease in rotational speed.

ACx Models

Earlier versions of the commutator were designed for use with the Medusa RA16PA preamps. The ACx commutators provided comparable performance in 16, 32, and 64 channel versions, but did not support the fiber optic rotary joint. ACx model operation is the same except where noted.

Part numbers:

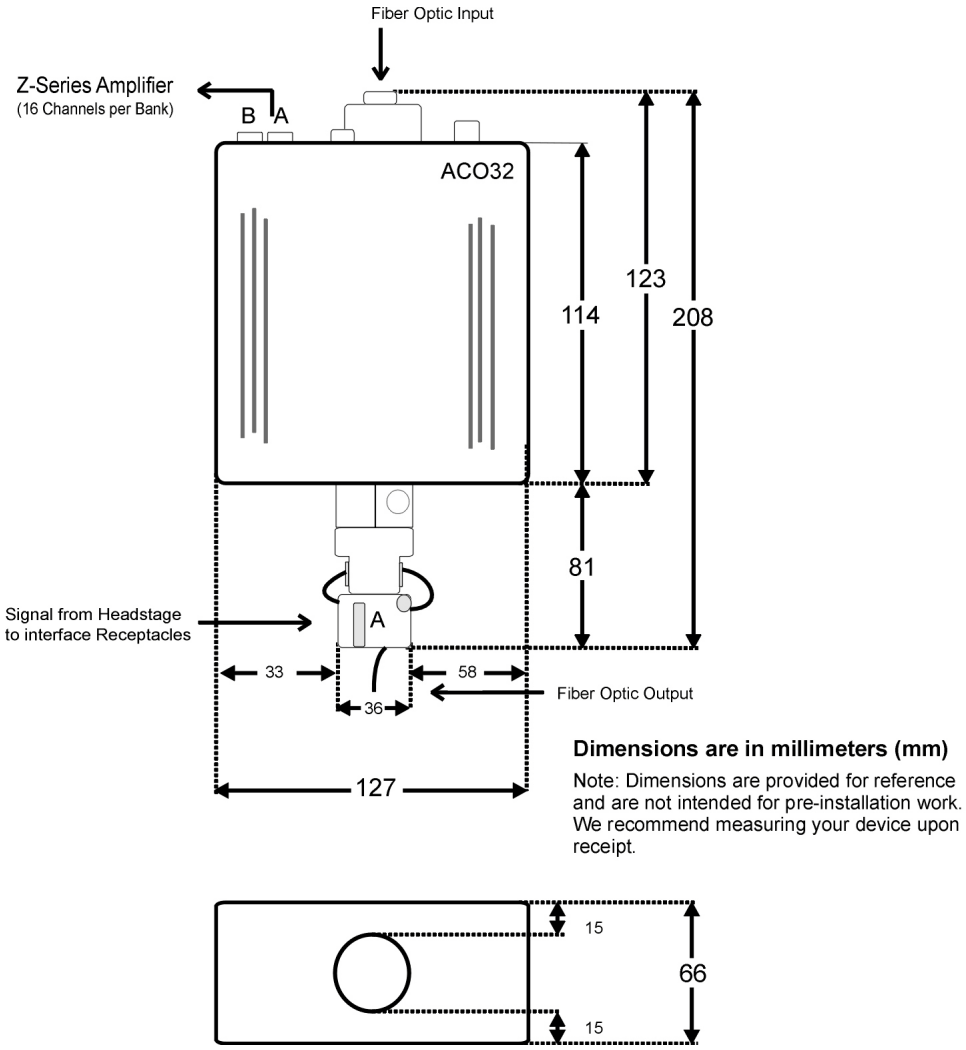
AC16 — 16 Channel Commutator

AC32 — 32 Channel Commutator

AC64 — 64 Channel Commutator

Hardware Setup

The commutator (ACO32 dimensions shown below with FORJ) is mounted above the subject. A PZ preamplifier is connected to the DB26 connectors marked A and B on the face of the commutator. A headstage (with splice connector) and a splice-to-splice adapter are connected to the interface receptacles on the connector module. See Headstage Connections below for more information on this connection.

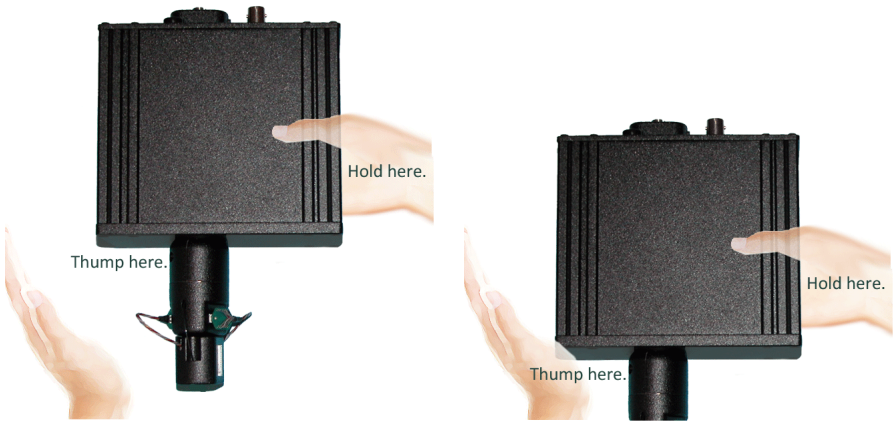


Note: The motor in the ACO32 commutator is attached to a plate designed to allow it to be disengaged for testing and troubleshooting noise issues. The plate may slide out of normal position during shipping or anytime the commutator is turned upside down.

If the motor is not engaged, you can turn the bottom section of the rotating shaft, but the rest of the shaft does not follow.

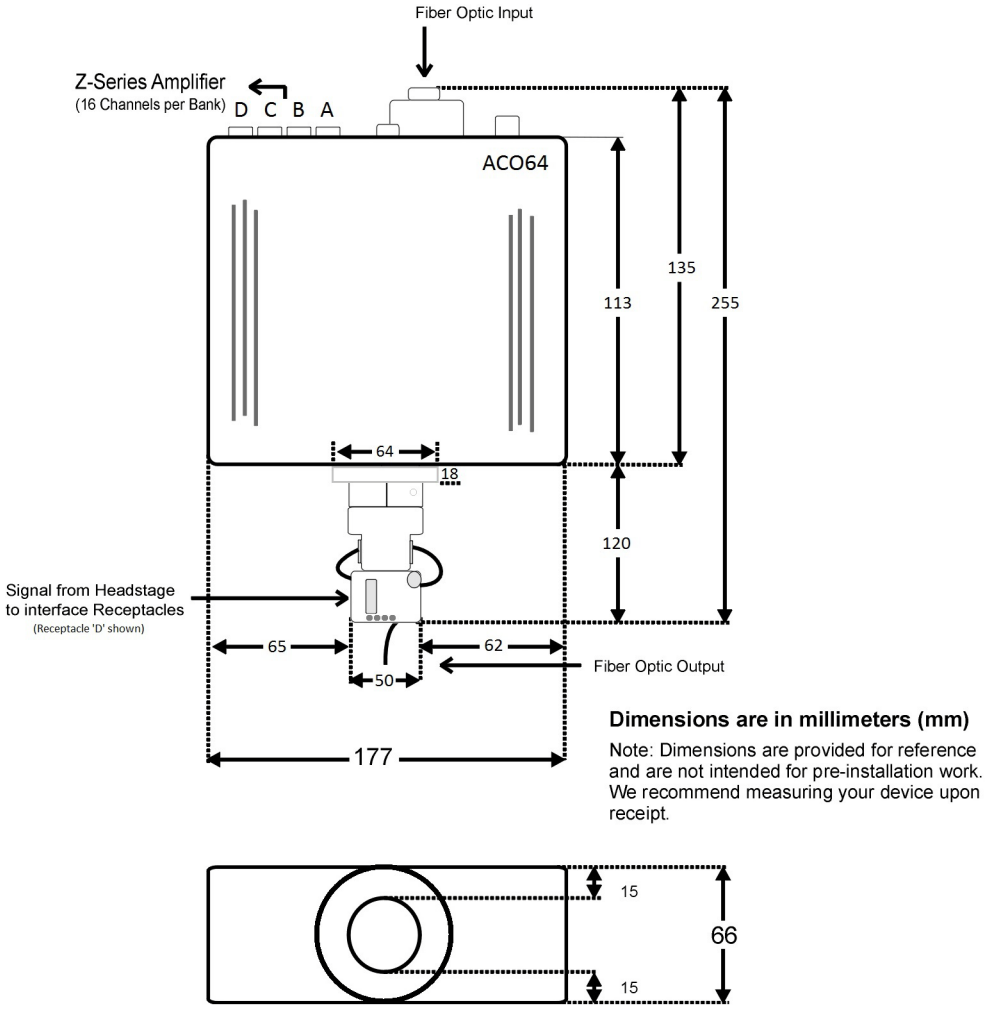
To reengage the motor:

1. Hold the commutator with the faceplate up.
2. Grip one side of the commutator.
3. Bring the commutator down to thump the bottom corner with the heel of your palm, as shown below.



ACO64

The ACO64 commutator (shown below with FORJ) is analogous to the ACO32 and also typically mounted above the subject. A PZ preamplifier is connected to the DB26 connectors marked A, B, C, and D on the face of the commutator. A headstage (with splice connector) and a splice-to-splice adapter are connected to the interface receptacles on the connector module. See Headstage Connections below for more information on this connection.



Dimensions are in millimeters (mm)

Note: Dimensions are provided for reference and are not intended for pre-installation work. We recommend measuring your device upon receipt.

Note: The motor in the ACO64 commutator does not disengage like the ACO32. The ACO64 has an additional hardware mount on the bottom, below the headstage receptacles, facing the subject.

ACx Setup Notes

Dimensions and form factor for ACx commutators not pictured. Before using the AC32 and AC64 commutators, adjust the wire harness to ensure it is balanced. The AC32 harness should be in two loops 180 degrees apart and the AC64 harness should be in four loops 90 degrees apart. Typically, preamps are connected to the connectors on the face of the commutator and headstages (with special splice connectors) are connected to the interface receptacles.

Features

LEDs

The four indicator LEDs on the front panel indicate power, the status of the Inhibit BNC input, clockwise rotation and counterclockwise rotation.

P	Power (~2 Hz flash when on)
I	Inhibit
	Counterclockwise rotation
	Clockwise rotation

Manual Rotational Buttons

The commutator features both clockwise and counterclockwise manual rotational buttons. When pressed, these buttons will rotate the commutator at approximately 18 RPM. Pressing either of these buttons also overrides the current rotational state of the commutator.

Inhibit BNC

During critical recording periods it may be necessary to prevent rotation to ensure signal integrity. A logical low (0) on the Inhibit BNC will prohibit any rotation initiated by either the sensors on the commutator or the manual rotational button.

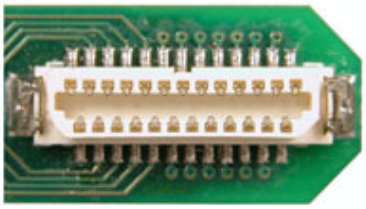
External Ground

A banana jack located on the face (GND) provides connections to common ground on the commutator.

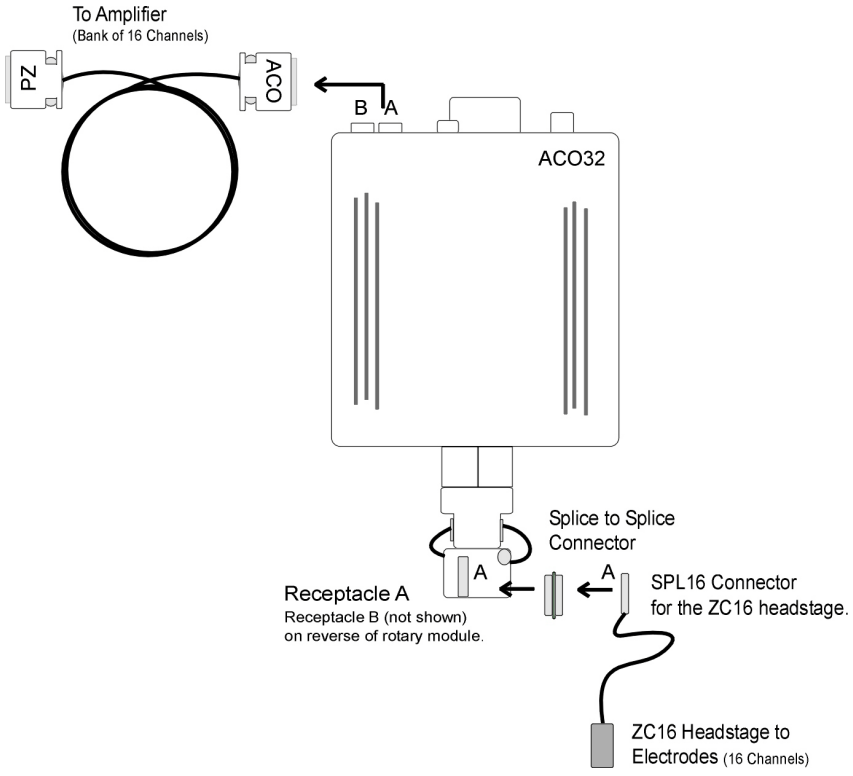
The external ground is optional and should only be used in cases where the subject must occasionally make contact with a metal surface that isn't tied to the animal ground, such as a lever press. When contact is made, a ground loop is formed that temporarily adds extra noise to the system. Grounding this metal surface directly to the TDT hardware removes this ground loop at the cost of raising the overall noise floor a small amount.

A cable kit is provided to ensure cables used with the external ground are suitable for this use. Each kit includes: one male banana plug to male banana plug pass through and one male banana plug to alligator clip pass through. These cables also include ferrite beads to remove any potential RF noise that might travel through the cable. For best results position the ferrite bead close to the source of the RF noise.

Headstage Connections



Two or four interface receptacles are positioned on the rotary interface module. The receptacles are labeled to correspond to the DB26 connectors on the face. The ACO32 uses 'A' and 'B' labels, the ACO64 uses 1-4 silver marks on the receptacles. TDT offers headstages and connectors with a mate for these receptacles.



The diagram above shows the ACO32 connection for the A subset of channels:

- from headstage (with SPL16 analog or SPL16-D digital connectors)
- to splice-to-splice connector

- to commutator receptacle
- to amplifier connection cable.

Channel numbers correspond to the amplifier bank of channels to which the cable is connected. For example, if the A connector is connected to Bank A on the PZ5 preamplifier, channels are numbered 1 – 16.

See "ACO Technical Specifications" on page 16-16, for pin mapping.

Amplifier Connections

The ACO commutator interfaces with a PZ amplifier via two or four DB26 connectors, 16 analog channels each) on the face. Adapter cables may also be used for connections to Medusa Preamps.

See "ACO Technical Specifications" on page 16-16, for connector pinouts.

Fiber Optic Rotary Joint (Optional)

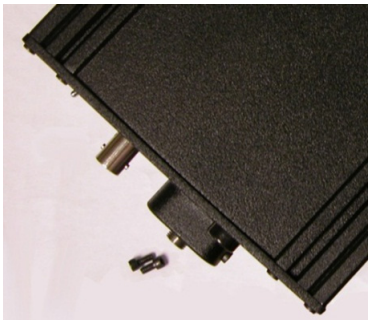
The fiber optic rotary joint (FORJ) assembly is an available add-on component. It includes an FC/FC optical fiber connector accessible on the commutator face and a single channel optical fiber threaded through the module. The FORJ can pass wavelengths from 440 – 610 nm suitable for optogenetic stimulation and the assembly supports use of fiber with a 1.25 mm cannula (tip). FORJ is also compatible with branched optical fibers of up to four bundles in the ACO64.

Replacing the Optical Fiber (ACO32)

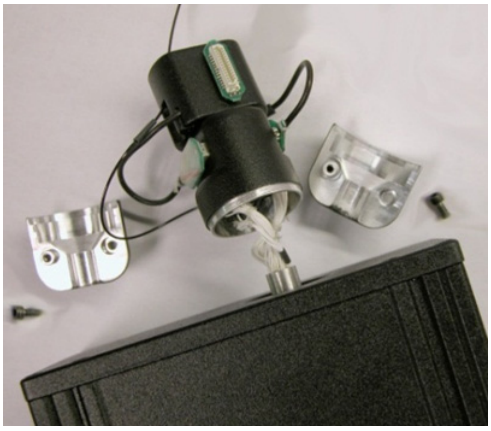
The FORJ assembly can be removed and re-installed by the user to replace the optical fiber.

To remove a currently installed FORJ:

1. Use a 3/32" Allen hex driver to remove the two screws securing the fiber optic rotary joint to the commutator face.



2. Use the hex driver to remove two screws securing the encoder clamping plates.



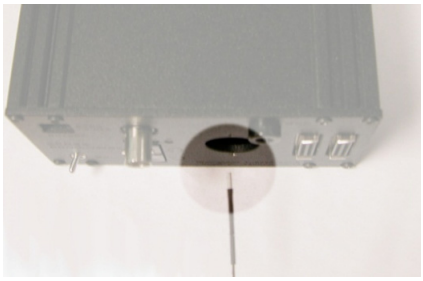
3. Carefully pull the FORJ away from the commutator face until the fiber is free.

4. Disconnect the fiber from the joint.

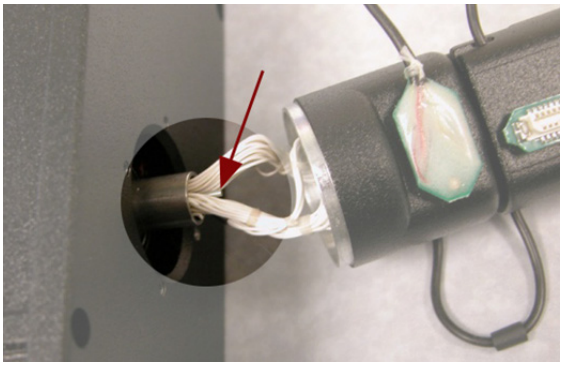
5. Replace the fiber.

To install the FORJ:

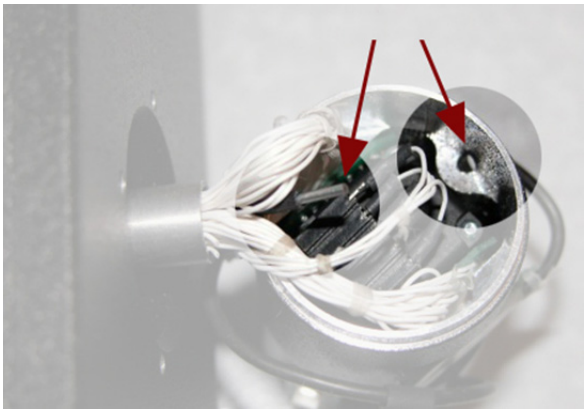
1. Insert metal cannula end of fiber into center of gear inside of ACO32.



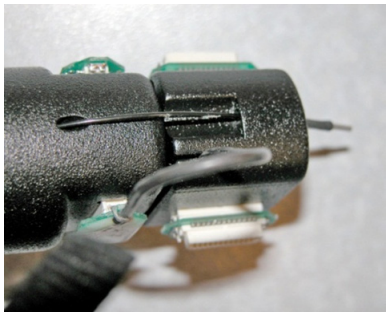
2. Slowly push fiber through hole until the end appears among the wires on the other side of the ACO32.



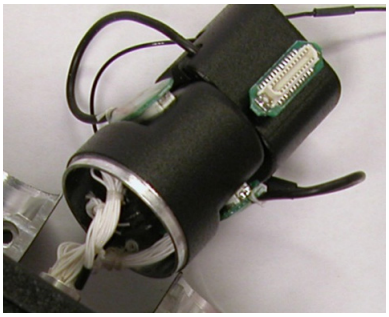
3. Using a pair of tweezers, carefully pull the end of the fiber and insert it into the hole next to the encoder.



4. Pull the end of the fiber through the hole and insert it through the hole in the groove of the connector module.



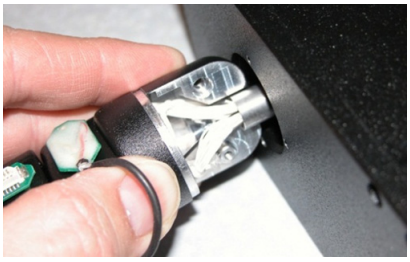
5. Leave enough slack in the section of fiber between the encoder and connector modules to match the loop of the other wires. A small lightweight tie can be loosely attached to hold the fiber adjacent to the wires.



6. Connect the FC/PC connector end of the fiber to (the smaller section of) the fiber optic rotary joint.

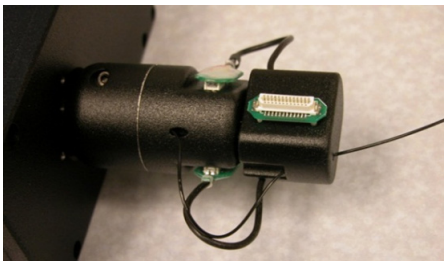
7. Slowly pull all of the excess fiber through the ACO32 until the FC/PC connector is inside the ACO32 and the fiber optic rotary joint plate can be attached to the ACO32 plate.

8. Attach the encoder clamping plates back onto the ACO32 shaft by tightening the two screws.



The plate should be just below body of the ACO32 and the encoder body should sit snuggly inside the lip of the clamping plates.

Be careful not to pinch any wires or the fiber as the plates are tightened together.



Note: If a FORJ is not used, the through-hole can be used for other related applications (e.g. fluid delivery system). Contact TDT for more details or assistance.

Change Kits

TDT provides two kits for users removing or adding a FORJ after initial purchase.

If you purchased the ACO32 or ACO64 without a FORJ and then add one, use the kit below to mount the new optics to the ACO32 or ACO64 faceplate.

If you purchased the ACO32 or ACO64 with a FORJ and wish to remove it, use the kit below to cover the opening where the FORJ was previously mounted.

Note: the two configurations use different screws, so be sure to save all screws.

Replacing the Optical Fiber (ACO64)

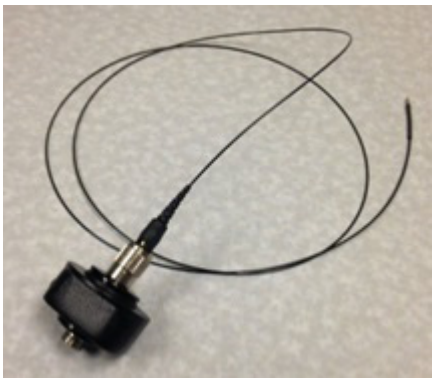
The FORJ assembly can be removed and re-installed by the user to replace the optical fiber.

To remove a currently installed FORJ:

1. Use a 3/32" Allen Hex driver to remove the two screws securing the fiber optic rotary joint to the commutator face.

2. Use the hex driver to remove the two screws securing the encoder clamping plates.

3. Carefully pull the FORJ away from the commutator face until the fiber is free.

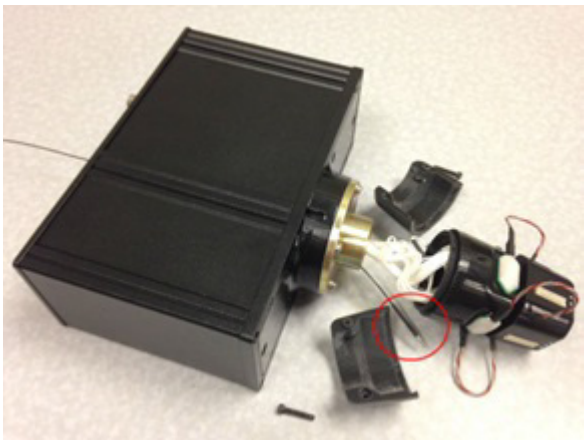


4. Disconnect the fiber from the joint.

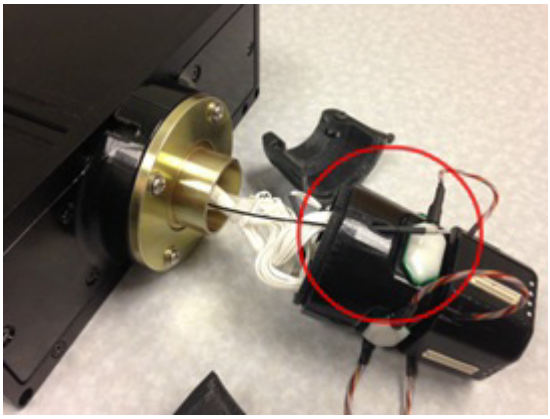
5. Replace the fiber.

To install one optical fiber in the FORJ:

1. Insert metal cannula end of the fiber into center of gear inside the ACO64.
2. Slowly push fiber through hole until the end appears among the wires on the other side of the ACO64. Carefully pull the wire through the slip ring.

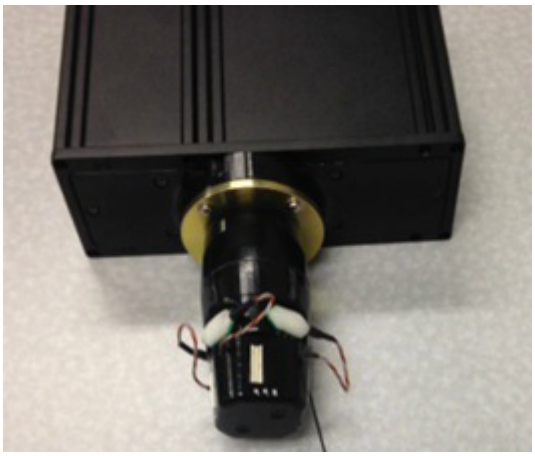


3. Insert and guide the fiber through a hole in the encoder cover, then pull through.



4. Secure the two encoder clamping shells back onto the ACO64 shaft by inserting and tightening the two screws.

5. The plate should be just below the body of the ACO64 and the encoder body should sit snugly inside the lip of the clamping plates. Be careful not to pinch any wires or the fiber as the plates are tightened together.



ACO Technical Specifications

Channels:	ACO32: with PZ2 or PZ5: up to 32 analog channels with PZ5: up to 256 digital channels ACO64: with PZ2 or PZ5: up to 64 analog channels with PZ5: up to 512 digital channels AC16: 16 AC32: 32 AC64: 64
Signal/Noise:	120 dB (20 Hz to 25 kHz)
RPM (approx):	18
Digital Inputs:	1 Inhibit
Power Consumption:	ACO32 and ACO64 quiescent: 35 mA ACO32 rotating: 65 mA ACO64 rotating: 75 mA
Run time:	ACO32: ~20 hr ACO64: ~40 hr
Power Supply:	ACO32: 1950 mAh Li-ion battery. 1000 cycles of charging. ACO64: 3900 mAh Li-ion battery. 1000 cycles of charging. Charger 6-9 V, 3A, center negative. Battery charges in 3-4 hours.
Weight (g):	ACO32 ~917 ACO32 with FORJ ~957 ACO64 ~1372 ACO64 with FORJ ~1412 AC16, AC32 ~665 AC64 ~945

Interface Receptacles

The interface receptacle diagram shows how the pins on each receptacle map to the pins on the associated DB26 connector on the face of the commutator. See pinouts below for the appropriate model.

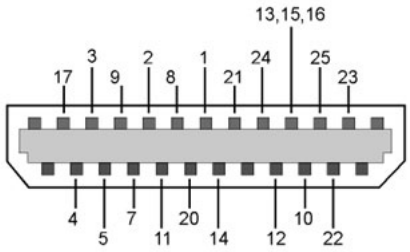
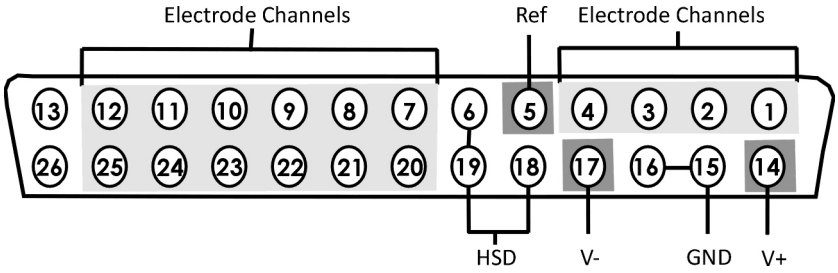


Diagram reflects pin numbers (not channel numbers).

ACO32 and ACO64 Amplifier Connectors Pinout

Connectors are labeled A and B on ACO32 and A, B, C, D on ACO64. Electrode channels below are relative to the electrode/headstage connected to the corresponding interface receptacle.

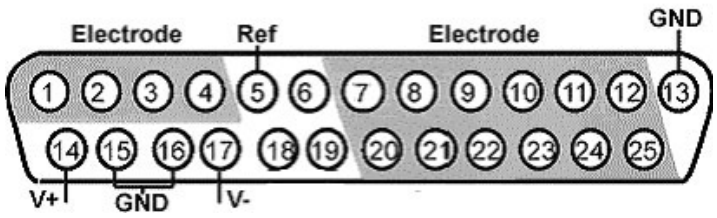


Pin	Name	Description		Pin	Name	Description
1	E1	Electrode Channels		14	V+	Positive Voltage
2	E2			15	GND	Ground
3	E3			16	GND	Ground
4	E4			17	V-	Negative Voltage
5	Ref	Reference		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	Headstage Detect
7	E5	Electrode Channels		20	E6	Electrode Channels
8	E7			21	E8	
9	E9			22	E10	
10	E11			23	E12	
11	E13			24	E14	
12	E15			25	E16	
13	N/A	Not Used		26	N/A	Not Used

Note: When mapping channel numbers for recording purposes, the preamplifier connections must be taken into account. The first channel as labeled below is relative to the amplifier bank of channel numbers connected. If connector B on the ACO32 is connected to the channel 1 – 16 connector on the preamplifier, E1 is channel 1, if connected to the channels 17 – 32 connector on the preamplifier, E1 is channel 17.

Important! **When using digital headstages and PZ4**, channel mapping is handled by the PZ4 and channels will be ordered consecutively beginning with Connector A (if connected).

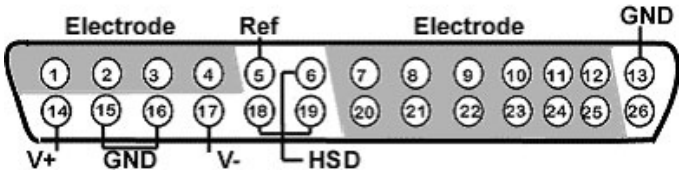
AC16 and AC32 A and B Connector Pinout



Pin	Name	Description		Pin	Name	Description
1	E1	Electrode Channels		14	V+	Positive Voltage
2	E2			15	GND	Ground
3	E3			16	GND	Ground
4	E4			17	V-	Negative Voltage
5	Ref	Reference		18	N/A	Not Used
6	N/A	Not Used		19	N/A	Not Used
7	E5	Electrode Channels		20	E6	Electrode Channels
8	E7			21	E8	
9	E9			22	E10	
10	E11			23	E12	
11	E13			24	E14	
12	E15			25	E16	
13	GND	Ground				

Note: Electrode channel numbers relative to the connected bank of preamplifier channels.

AC64 1 - 4 Connector Pinout



Pin	Name	Description		Pin	Name	Description
1	E1	Electrode Channels		14	V+	Positive Voltage
2	E2			15	GND	Ground
3	E3			16	GND	Ground
4	E4			17	V-	Negative Voltage
5	Ref	Reference		18	HSD	Headstage Detect
6	HSD	Headstage Detect		19	HSD	Headstage Detect
7	E5	Electrode Channels		20	E6	Electrode Channels
8	E7			21	E8	
9	E9			22	E10	
10	E11			23	E12	
11	E13			24	E14	
12	E15			25	E16	
13	GND	Ground		26	N/A	Not Used

Note: Electrode channel numbers relative to the connected bank of preamplifier channels.

Important! Connectors 2, 3, and 4 share common GND, V+, and V-.

Part 17: Transducers and Amplifiers

MF1 Multi-Field Magnetic Speakers

Overview

TDT Multi-Field Magnetic Speakers offer high output and fidelity over a wide bandwidth and deliver more power at lower frequencies than our electrostatic speakers. They are well-suited for laboratory species with lower frequency hearing and for noise exposure studies.

A detachable tip allows them to be configured for either free- or closed- field use. The closed-field configuration incorporates an internal parabolic cone designed to maximize output and minimize distortion. The tip is tapered for use with 1/8" O.D. PVC tubing. The mono speaker is provided with two 10 cm tubes and the dual speaker set is provided with four 10 cm tubes.

Note: An Ear Tip for direct application (no tubing required), is also available.

Speakers feature a rugged aluminum housing and a built-in, 8-32 threaded hole for use with standard laboratory mounting hardware. The mono speaker includes an aluminum stand and the dual speaker set includes a variety of aluminum mount/base fittings for easier positioning.

Each MF1 kit (serial number > 1200) also includes a USB drive containing several speaker-specific closed field and free field calibration curves (TCF files) made during final testing at TDT. These files were designed to be used with the BioSigRZ software. When using the MF1 speakers above 30kHz in free field mode, TDT recommends using the speaker-specific TCF files in place of the generic speaker curves provided in the BioSigRZ installation (stored, by default, at C:\TDT\BioSigRZ\TCF).

The speakers can be driven directly from the RZ6 or using either TDT's SA1 or SA8 stereo amplifiers. The speaker input carries both bias and signal voltages from the stereo amplifier.

Part Numbers:

MF1-M—Mono

MF1-S—Dual （two speakers）

Multi-Field Configurations

The MF1 speaker is comprised of the free-field speaker and a closed-field adapter, a tapered tip, and line filter for closed-field use. An RCA to BNC adapter and stand are also provided.

Using the MF1 for Free Field Operation

The MF1 main speaker component can be used for free-field sound production. The speaker can be connected to the source via an RCA connector located on the back of the MF1 housing. If using the stereo amplifier built into the RZ6, simply connect the supplied RCA cable from the MF1 to one of the output BNC connectors on the RZ6 using the supplied RCA to BNC adapter.

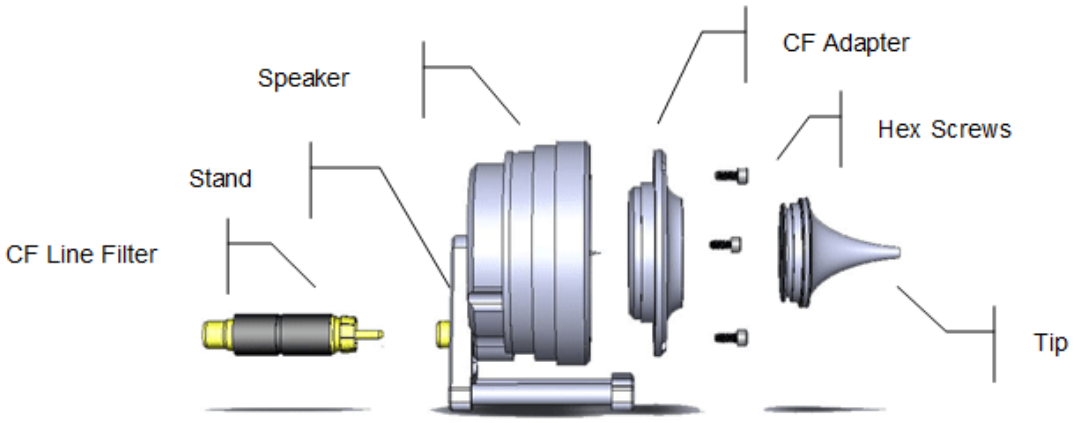
⚠ Caution!: When the speaker is configured for free field use, be careful to avoid touching the exposed speaker membrane.

Configuring the MF1 for Closed Field Operation

For closed-field operation, the Close Field adapter is attached to the face of the speaker using three hex screws. A parabolic tip is be mounted in the recessed socket on the closed-field adapter and is held securely in place by an o-ring at the base of the tip.

The speaker can be connected to the source via an RCA connector located on the back of the MF1 housing. If using the stereo amplifier built into the RZ6, simply connect the supplied RCA cable from the MF1 to one of the output BNC connectors on the RZ6 using the supplied RCA to BNC adapters.

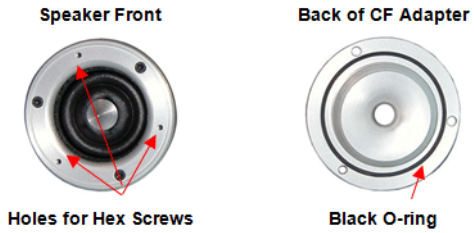
Important! When using the MF1 in the closed-field configuration the supplied CF line filter must be installed between the BNC to RCA adapter and the RCA cable. This filter minimizes distortion at lower frequencies in the closed-field.



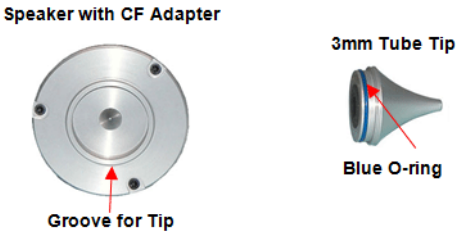
To configure the MF1 for closed-field:

1. Ensure black o-ring is in place on back of CF adapter, as shown.

   Attach the CF adapter to the front of the speaker using three of the provided 1/4 x 4-40 hex screws.



2. Ensure the blue o-ring is in place at the base of the desired tip, as shown.
3. Insert one of the tips into the groove on the CF adapter. Ensure the tip is bottomed in its socket. If using the tube tip, gently insert the tube into the narrow end of the tip.



4. Attach a BNC to RCA adapter to the BNC amplifier port of your source device.

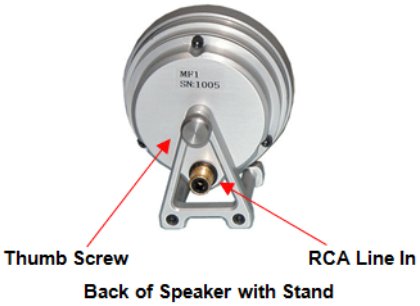
   Attach the CF filter to the RCA cable.

CF Filter

For Closed Field Configuration Only

If desired, the provided stand can be attached to the speaker using a thumbscrew.

- Connect the MF1 to the amplifier using the RCA cable (with CF filter attached).



Back of Speaker with Stand

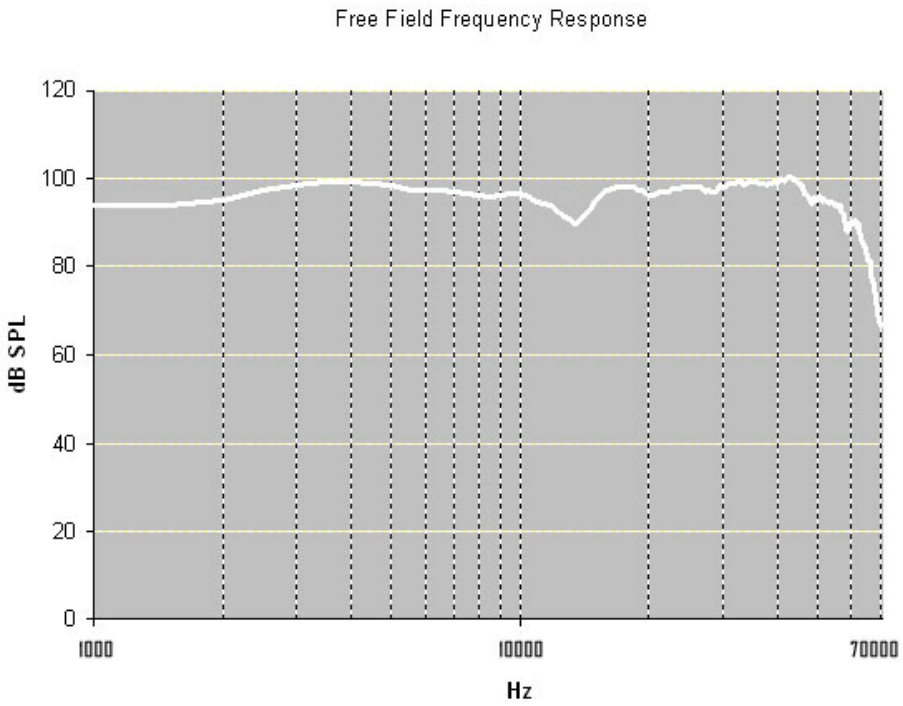
Closed-Field Speaker Design Considerations

When using the closed-field configuration for experiments, the provided PVC tubing will transfer the signal best when it is kept straight. Note that the speaker performance is dependent on the coupling system used and the ear of the subject. All speaker configurations should be calibrated to your specific configuration. Technical specifications measured under specific controlled conditions are provided for comparison purposes.

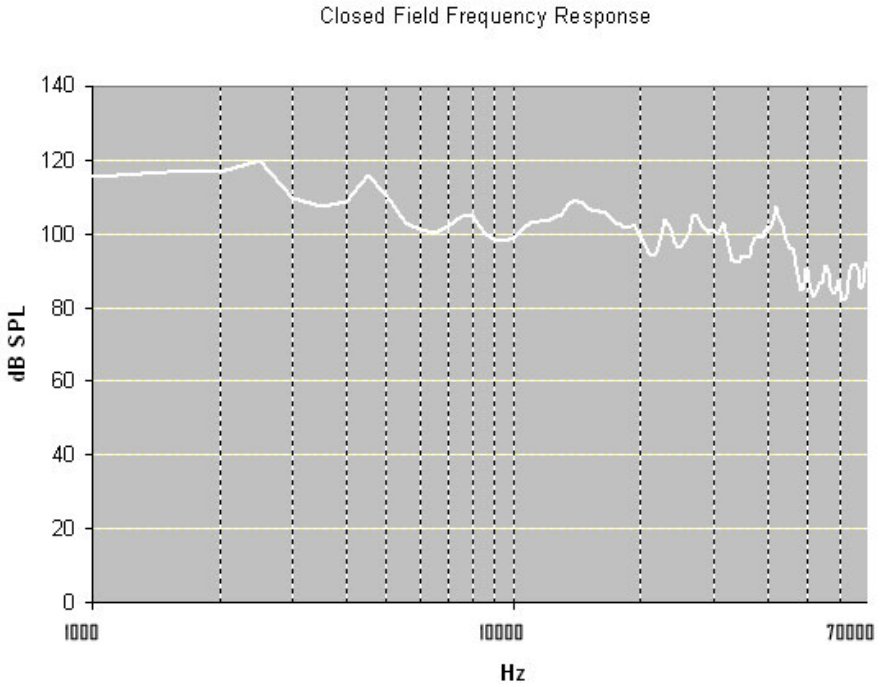
Technical Specifications

Weight	Free Field Closed Field	~216g ~277g	
Dimensions	Outside Diameter		6.6 cm
	Depth	Free Field	3.6 cm
		w/Tube Tip	6.8 cm
		w/Ear Tip*	7.1 cm
Typical Output (+/- 1 V peak input)	Free Field	87 dB SPL at 10 cm	
	Closed Field	100 dB SPL in 0.1 cc coupler	
THD	<= 1% from 1kHz to 50 kHz		
Impedance	4 Ohms		
Max driving voltage	75 W (for third party amps)		

* Available on request.

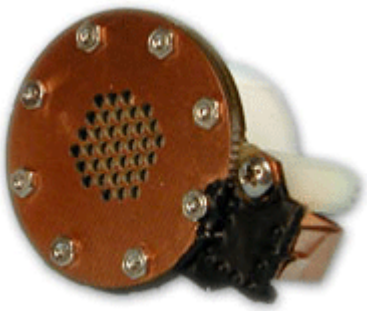


Free field measurements typical at 10 cm using +/- 1V input.



Closed field measurements typical for approx 0.1cc eartip coupler using +/- 1V input.

EC1/ES1 Electrostatic Speaker



Overview

TDT Electrostatic Speakers (Patent No. US 6,842,964 B1) are designed specifically for ultrasonic signal production. The electrostatic design offers a thin, flexible membrane with an extremely low moving mass. Unlike conventional speakers, these speakers distribute the driving signal homogeneously over the surface of the membrane. These factors produce a small, lightweight speaker with an excellent ultrasonic response and very low distortion. Available with or without a coupler, both models are easy to position and are particularly well suited for studies with small animals that have hearing in the ultrasonic range.

Part Numbers (Patent No. US 6,842,964 B1):

ES1—Free Field Electrostatic Speaker

EC1—Electrostatic Speaker—Coupler Model

Cable Connection

The ES1 and EC1 electrostatic speakers work exclusively with the ED1 Electrostatic Speaker Driver. Input is via a 4-pin, mini-DIN connector, which carries both bias and signal voltages from the speaker driver. Connection to the speaker driver is through a standard 6.1 m long cable. Other cable lengths can be special ordered, but will affect the speaker's frequency response. The speakers come fully enclosed to eliminate access to the high-voltage bias and driving signals. A 3.175 mm mounting hole at the base of the speaker accepts a standard 4-40 standoff. See "ED1 Electrostatic Speaker Driver" on page 17-15, for information about gain settings.

The orientation of the cable connection is indicated with dots on the cable connector and on the speaker. The cable should be connected so that the dot on the cable faces towards the speaker.

When connecting the cable, ensure that the four pin connectors are fully seated on the speaker and the speaker driver. When the cable is repeatedly moved during the experiment, periodically check that the connectors are fully seated.

EC1 Coupled Electrostatic Speaker

The EC1 includes a small piece of Tygon® tubing coupled to the output. The tubing will transfer the signal best when it is kept straight. Note that the speaker performance is dependent on the coupling system used and the ear of the animal. Users should test the device under experimental conditions to ensure it meets their requirements. Technical Specifications measured under specific controlled conditions are provided for comparison purposes.

Maximizing the Life of the Speakers

The TDT electrostatic speakers are designed to operate with input signals between 4 and 110 kHz. Playing signals below 4 kHz causes a large amount of harmonic distortion that degrades the operation of the speakers over time, causing a decreased power output across all frequencies. Although the speakers won't clip until +/-10V, presenting continual input voltage over +/-4 V will reduce speaker lifespan.

Broadband Signals

When using broadband signals, limit the amount of energy in the low frequency ranges whenever possible. For example, band limiting noise stimuli with a high pass filter at 4 kHz or above (the higher the better for the life of the speakers) and limiting complex harmonic signals, such as frequency sweeps, to frequencies above 4 kHz can increase the effective life of the speakers.

Click Stimuli

ABR experiments in both human and mouse studies typically use a 100 microsecond click stimuli, which has most of its energy in the 2 kHz to 8 kHz range. Because click stimuli are short impulses that generate signals across a broad frequency range, band limiting the frequencies is not feasible. TDT recommends that users attenuate the click stimuli so as to minimize the potential effects on the speaker. Also note that the shorter the stimuli the flatter the frequency response and the greater the energy in the higher frequencies. Moreover, the shorter the duration of the click the less total energy it has (for a given voltage).

Routine Care and Maintenance

Inspect speakers for visual damage or obstruction of the speaker holes prior to use. If there is damage to the copper shield around the components next to the connector or debris clogging the speaker holes, contact TDT for an RMA for repair.

⚠ CAUTION! NEVER attempt to clean the holes in the baseplate of the speaker. Doing so can puncture the speaker membrane.

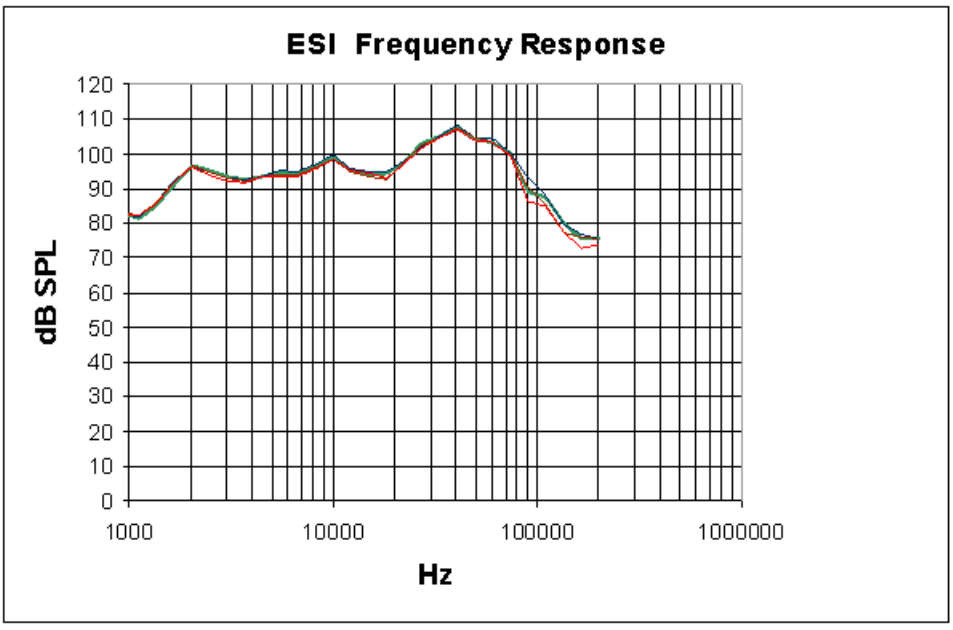
When using the EC1, check the end of the Tygon® tubing for cerumen and other debris and clean as necessary.

Technical Specifications

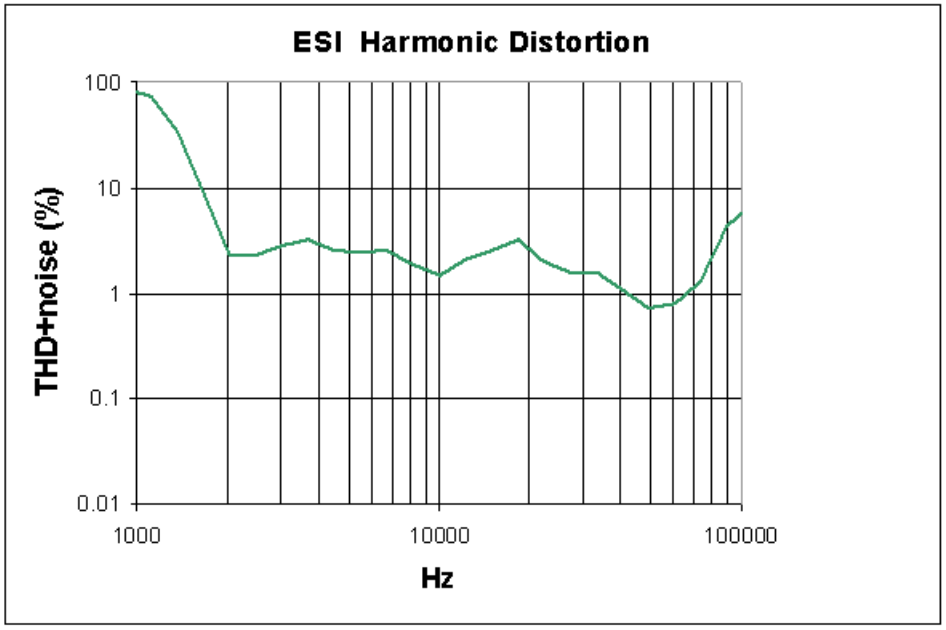
ES1 Technical Specifications

Frequency Response	+/- 11 dB from 4 kHz to 110 kHz
Weight	22 Grams
Dimensions	3.8 cm outside diameter x 2.6 cm deep
Typical Output (10V peak input)	95 dB SPL at 10 cm, 5 kHz signal
THD	< 3%, 2 kHz - 110 kHz, 4 Vp input

Free-field Frequency Response of Four Speakers at 10 cm



Harmonic Distortion at 4 V Peak



Noise as well as harmonic distortion is measured. Lower signal levels (e.g. above 75 kHz shown above) have higher THD+noise because of lower signal to noise ratios. When measured at higher signal levels, the THD above 75 kHz is actually <3% up to 110 kHz.

EC1 Technical Specifications

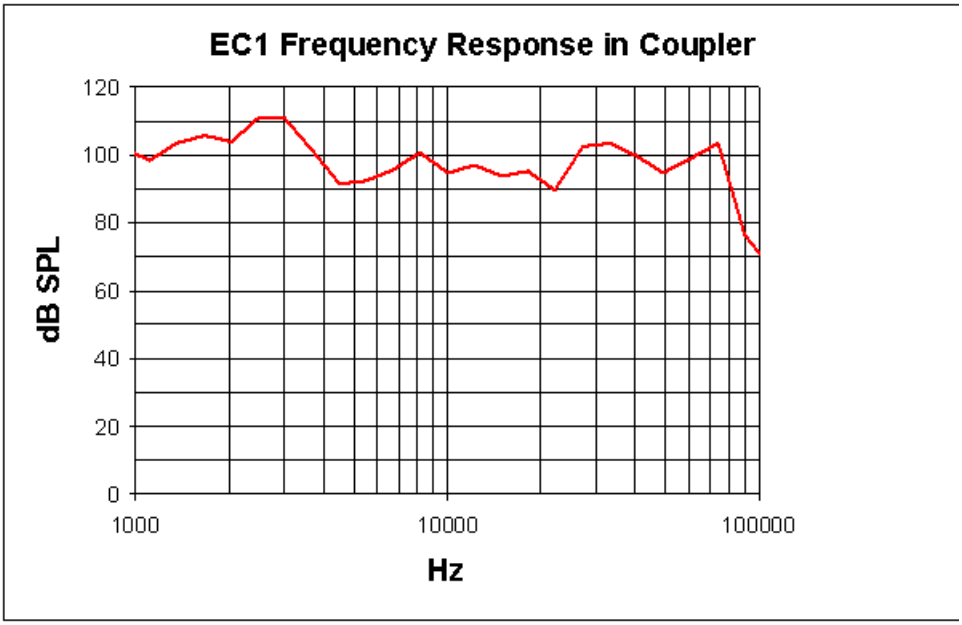
Frequency Response	+/- 9 dB from 4 kHz to 110 kHz
Weight	22 Grams
Dimensions	3.8 cm outside diameter x 2.6 cm deep
Typical Output	90 dB SPL, 5kHz signal∗ *Every experimental setup is unique. It is important to calibrate the response of the speaker in each experimental setup.*
THD	*Every experimental setup is unique. It is important to calibrate the response of the speaker in each experimental setup.*

Frequency Response in Plexiglas Coupler

∗Measurements were made in a 1 cm x 0.5 cm coupler with a 20 cm length of 2.4 mm i.e. tubing attached to the fitting of the EC1. 4 V peak input tones were tested and frequency response was measured with a calibrated pressure microphone.

The results of the calibration will vary depending on the type of ear to which the speaker is coupled and the length of the tube that is coupled to the ear. This curve

is provided as representative of the type of response that may be obtained in a closed field.



In this case, the low end of the response (< 5 kHz) is enhanced over the free-field response while the high end of the response (> 80 kHz) is attenuated.

Every experimental setup is unique. It is important to calibrate the response of the speaker in each experimental setup.

Important! Modifying the EC1 or ES1 can result in unexpected changes in the transfer function. All modifications to the EC1 or ES1 should be performed by TDT. If you need to be 30-60 dB lower than specifications, or if you have one of these devices, contact TDT for assistance.

ED1 Electrostatic Speaker Driver

Overview

The ED1 is a broadband electrostatic driver that produces incredibly flat frequency responses reaching far into the ultrasonic range. The ED1 is designed especially for TDT's ES series electrostatic speakers. The ED1 Electrostatic speaker driver can drive two ES series speakers and is powered off the zBus.

The ED1 is a TDT System 3 device, and receives power from the zBus. It's two input BNCs accept input signals up to 10 Vpeak. The front panel gain control can be used to the control overall signal level of both channels from 0 to -27 dB in 3 dB steps. ED1 output is via two 4-pin, mini-DIN connectors, which carry both bias and signal voltages. The ED1 is designed to work exclusively with TDT ES series electrostatic speakers.

While the ED1 will accept a 10V input, it is possible to overdrive and ES1 when the ED1 is on the maximum gain setting. Always check that the output signal is not distorted. If the signal is distorted, turn down the gain on the ED1 until the distortion disappears. The SigCalRP software that is distributed with SigGenRP is useful for measuring the frequency response of the ES1 and to measure the Total Harmonic Distortion (THD) of the speaker. SigCalRP also generates normalization curves that can be used to flatten the frequency response of the ES1.

Power

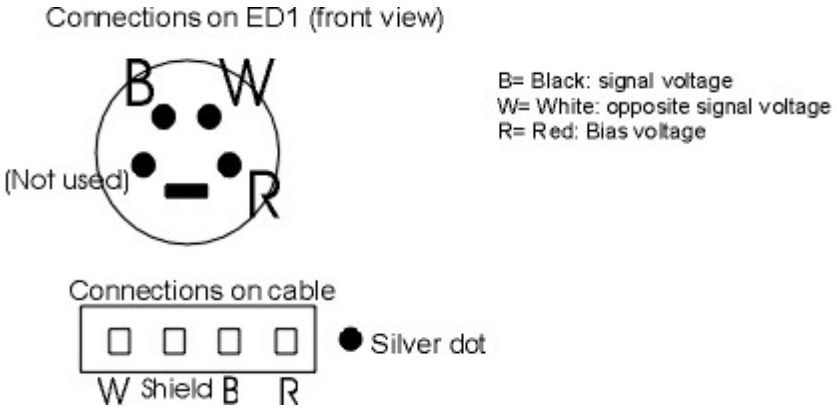
The ED1 Electrostatic Speaker Driver is powered via the System 3 zBus (ZB1PS). No PC interface is required.

ED1 Technical Specifications

Input Signal Range	+/- 10 V peak into ED1
Gain	0 dB to -27 dB on both channels, in 3 dB steps
Input Impedance	10 kOhm
Output Impedance	1 kOhm

Note: For further information, see “EC1/ES1 Electrostatic Speaker” on page 17-9.

ED1 Pinouts



HB7 Headphone Buffer

Overview

The HB7 headphone buffer is used to amplify signals for headphones. The HB7 is a two channel device. The outputs include both a stereo headphone jack and Left and Right BNC connectors. The output level can be controlled with a Gain knob, and there is a Differential switch that allows the LEFT input to be output to the Left and Right outputs resulting in an additional 6 dB of gain.

Power

The HB7 Headphone Buffer is powered via the System 3 zBus (ZB1PS). No PC interface is required.

Features

Inputs

The HB7 has two inputs for signals up to ±10 V, accessed through front panel BNC connectors labeled LEFT and RIGHT.

Outputs

The outputs include both a stereo headphone jack labeled PHONO and Left and Right BNC connectors.

Note: When monitoring both output channels with only one input connected, users should short the unused input channel to ensure maximum channel separation.

Gain

A single GAIN knob provides control over the signal output level in 3 dB steps from 0 to -27 dB.

AC/DC Switch

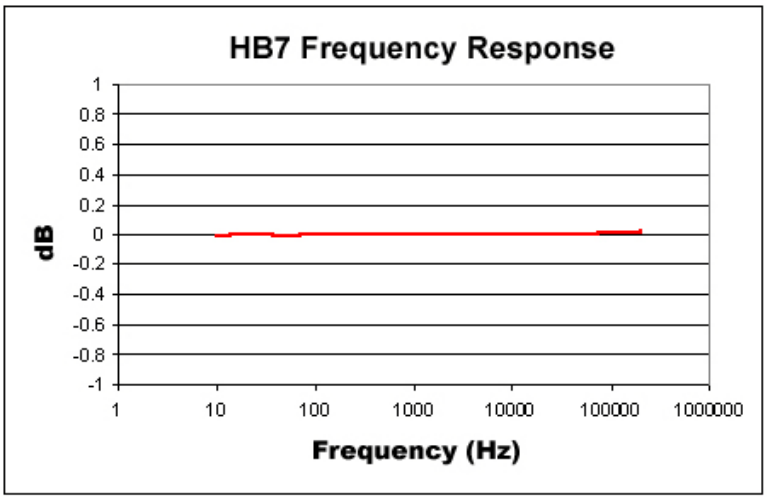
The AC/DC switch can be used to switch from DC coupling to AC coupling mode. In AC coupling mode, a 0.5Hz high pass filter is applied to the signals.

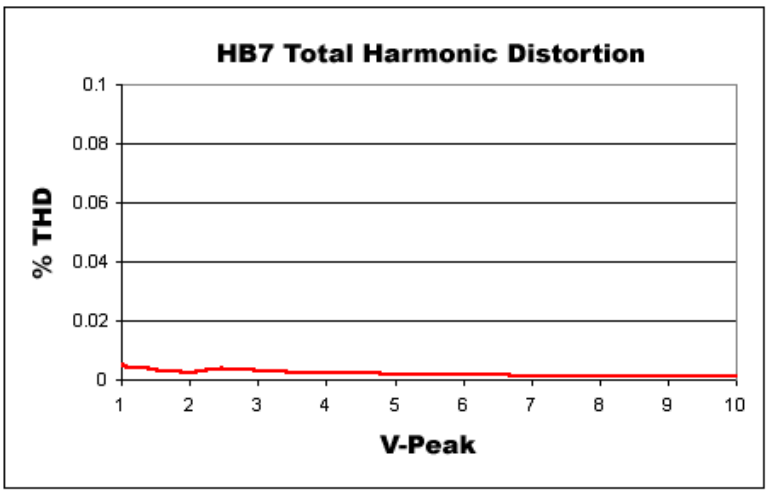
DIFF Switch

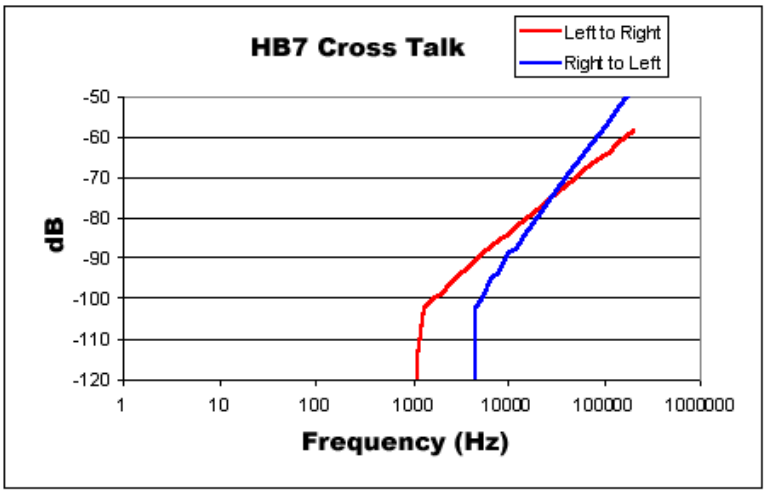
The DIFF switch will switch to a differential output mode that gives 6 dB of additional gain when connected to a speaker. When DIFF is switched on (the switch in the up position), the left channel input goes to both the left and right channels and is inverted on the right channel (the right input BNC is not used). The differential output will usually only be used with speakers, not headphones. To connect the speaker, connect the left output to one pole of the speaker and the right output to the other pole of the speaker (neither ground of the left nor right output will be connected).

HB7 Technical Specifications

Input Signal Range	±10 V peak
Power Output	0.12 W into 4 Ohms, 0.25 W into 8 Ohms, 1.0 W into 32 Ohms
Spectral Variation	< 0.1 dB from 10 Hz to 200 kHz
Signal/Noise	117 dB (20 Hz to 80 kHz)
Noise Floor	9.2 μV rms
THD	< 0.0002% (1 kHz tone, +/- 7V peak)
Corner Frequency (AC-Coupled Mode)	0.5 Hz
Input Impedance	10 kOhm
Output Impedance	5 Ohm


HB7 Frequency Response
dB
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
1
10
100
1000
10000
100000
1000000
Frequency (Hz)


HB7 Total Harmonic Distortion
% THD
0.1
0.08
0.06
0.04
0.02
0
1
2
3
4
5
6
7
8
9
10
V-Peak


HB7 Cross Talk
Left to Right
Right to Left
dB
-50
-60
-70
-80
-90
-100
-110
-120
1
10
100
1000
10000
100000
1000000
Frequency (Hz)

MA3 Microphone Amplifier

MA3 Overview

The MA3 is a two-channel microphone amplifier for auditory scientists. This high-quality low-cost system is designed for use with both ¼" audio jack microphones and balanced XLR inputs for optimum impedance and noise characteristics. The MA3 is able provide a bias voltage for microphones that require it. Two BNC connectors provide analog output. A variable gain knob provides amplification from 10 dB to 55 dB in 5 dB steps. A toggle switch provides 20 dB of additional gain for over five thousand fold amplification.

Power

The MA3 Microphone Amplifier is powered via the System 3 zBus (ZB1PS). No PC interface is required.

MA3 Features

Inputs

The MA3 comes with three inputs: an XLR microphone input and two ¼" TRS connector inputs. Signals from two microphones can be amplified simultaneously.

Bias

The Bias switch produces a bias voltage for microphones that require it.

Gain Control

The gain control amplifies the microphone input in 5 dB steps from 10-55 dB (3x-560x). The Gain Switch adds an additional 20 dB (10x) of gain for a maximum amplification of 5600.

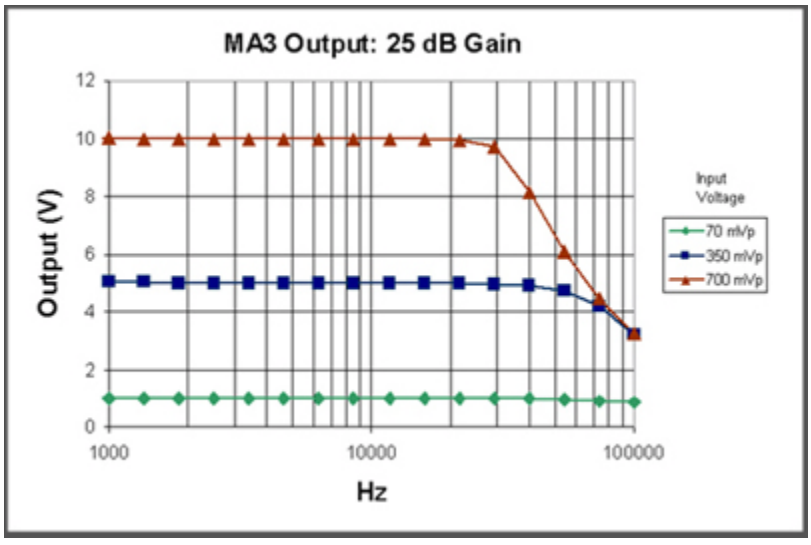
Outputs

Two BNC outputs give easy connection to any TDT System 3 device. The maximum voltage output is +/- 10 Volts. Clip lights indicate and overvoltage on the signal output.

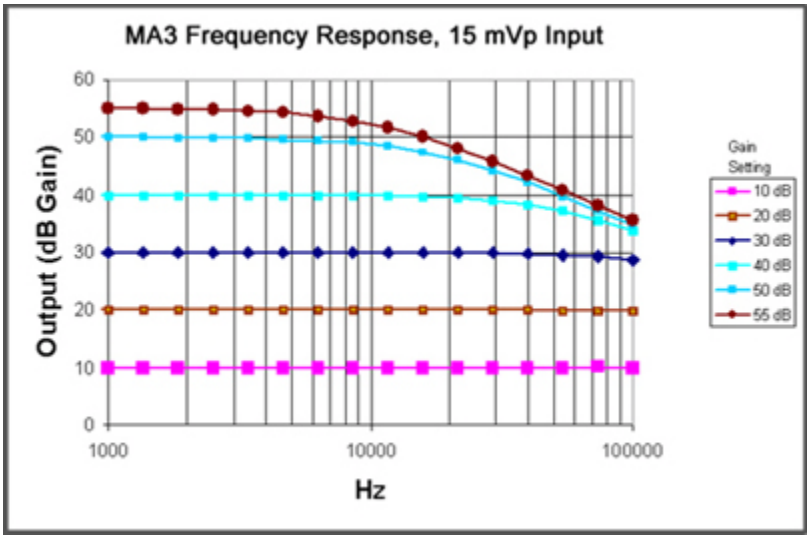
MA3 Technical Specification

Input Signal Range	+/- 10 V peak
-3dB Bandwidth	200 kHz @ 40 dB gain
Gain Accuracy	+/- 1 dB
Spectral Variation	1 dB from 20 Hz to 20 kHz
Signal/Noise	110 dB (20 Hz to 30 kHz at 9.9 V)
Noise Floor	9.2 µV rms
THD	< 0.002% (1 kHz tone, +/- 7 V peak)
Input Impedance	600 Ohm
Output Signal Range	+/- 10 V peak
Bias Voltage	10 V, 150 mA max, superimposed onto microphone
Output Impedance	5 Ohm

Output Diagram



Frequency Response Diagram



MS2 Monitor Speaker

MS2 Overview

The MS2 Monitor Speaker is used as an audio monitor for signals up to ± 10 V. The MS2 output level is controlled manually using a 1-turn potentiometer on the front panel interface. Maximum output is greater than 90 dB SPL at 10 cm. The frequency response ranges from 300Hz to 20 kHz. A typical use of the MS2 is for audio monitoring of electrophysiological potentials.

Power

The MS2 Monitor Speaker is powered via the System 3 zBus (ZB1PS). No PC interface is required.

MS2 Features

Manual control is via a single LEVEL knob, which provides control over the signal output level. The MS2 has one input channel for signals up to ±10 V, accessed through a front panel BNC connector

The MS2 is useful for monitoring the output signal that may be going to headphones in a soundproof room and for monitoring physiological signals that are being acquired, such as neurophysiology recordings.

MS2 Technical Specifications

Input Signal Range	±10V peak
Max Output	> 90 dB SPL at 10 cm
Input Impedance	10 kOhms

SA1 Stereo Amplifier

SA1 Overview

The SA1 is a power amplifier for the zBus that delivers up to 3 watts of power to speakers. It has excellent channel separation combined with low noise and distortion. The frequency response is flat from 50 hertz to 200 kilohertz. Gain can be varied over a 27 dB range in 3 dB increments.

Power

The SA1 Stereo Amplifier is powered via the System 3 zBus (ZB1PS). No PC interface is required.

SA1 Features

Inputs

There are two inputs (±10 V maximum) that connect through BNC's labeled IN-1 and IN-2.

Outputs

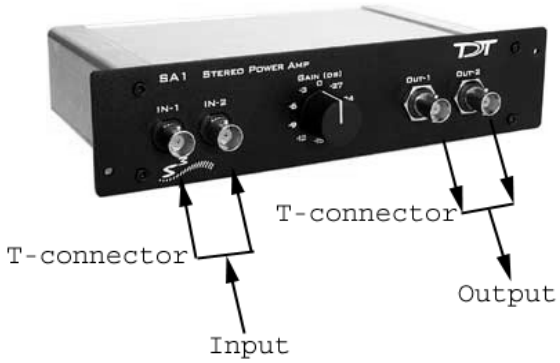
The outputs are two (OUT-1 and OUT-2) BNC connectors.

Gain

A single GAIN knob provides control over the signal output level in 3 dB steps from 0 to -27 dB.

Ganged Output Mode

A ganged output mode gives 6 dB of additional gain when connected to a speaker. Split the signal to the input; send one to the IN-1 and the other to IN-2. Take the outputs from OUT-1 and OUT-2 and combine them to boost the gain.



SA1 Technical Specifications

Input Signal Range	± 10 V peak
Power Output	1.5 W/channel into 5.5 ohm, 4 W with ganged output
Spectral Variation	< 0.1 dB from 50 Hz to 200 kHz
Signal/Noise	116 dB (20 Hz to 80 kHz)
THD	< 0.02% at 1 Watt from 50 Hz to 100kHz
Noise Floor	10.5 uV rms
Input Impedance	10 kOhm
Output Impedance	0.6 ohm, 0.3 ohm ganged

SA8 Eight Channel Power Amplifier

SA8 Overview

The SA8 is an eight-channel power amplifier that delivers up to 1.5 watts of power per speaker to up to eight speakers. The unit features high channel separation with low cross talk combined with low noise and distortion. The gain for all eight channels can be set to 0, -6, -10 or -13 dB.

Power

The SA8 Power Amp is powered via the System 3 zBus (ZB1PS). No PC interface is required.

SA8 Features

Inputs

There are eight available inputs located on the DB9 connector on the front panel of the SA8.

Outputs

The eight output channels are accessible via the DB25 connector and are arranged for optional direct connection to a PP16 Patch Panel. For easy wiring and connection to a wide variety of transducers, the eight outputs are duplicated on the DB25 and sufficient ground pins are provided to allow for connections requiring a single ground for all channels or paired grounds for each channel. See "Mapping SA8 Output to PP16 Connectors" on page 17-30, for more information on easy access to SA8 output channels via the patch panel.

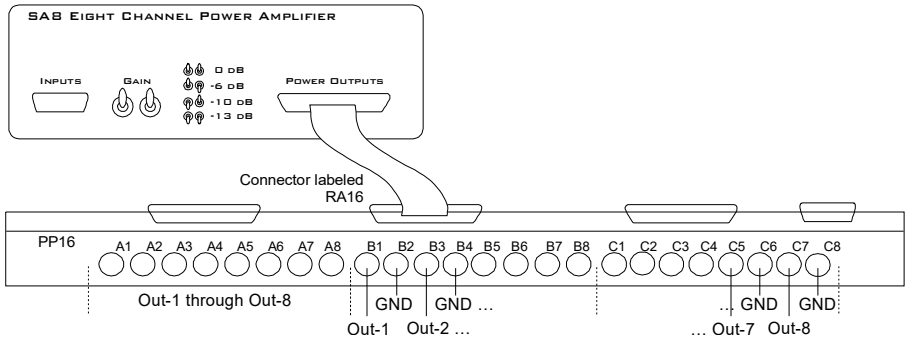
Gain

The gain is controlled by two toggle switches on the front panel of the SA8. The following table describes the selectable gain values.

Front Panel Diagram	Left Toggle	Right Toggle	dB Gain
	Up	Up	0
	Up	Down	-6
	Down	Up	-10
	Down	Down	-13

Mapping SA8 Output to PP16 Connectors

The picture below maps the SA8 signal out connection to the PP16.

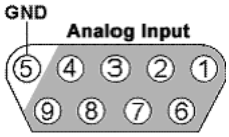


SA8 Technical Specifications

Input Signal Range	± 10 V peak
Power Output	5 W total into 5.5 ohm loads, split across all connected channels
Spectral Variation	< 0.1 dB from 50 Hz to 200 kHz
Signal/Noise	116 dB (20 Hz to 80 kHz)
THD	< 0.02% at 1 Watt from 50 Hz to 100kHz

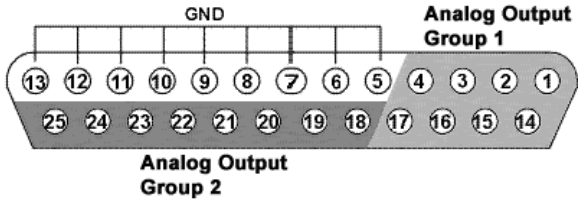
Noise Floor	10.5 µV rms
Input Impedance	10 kOhm
Output Impedance	2 ohms
Cross Talk	< -60 dB

Analog Input Pinout Diagram



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		6	A2	Analog Input Channels
2	A3			7	A4	
3	A5			8	A6	
4	A7			9	A8	
5	GND	Ground				

Analog Output Pinout Diagram



Pin	Name	Description		Pin	Name	Description
1	A1	Analog Output Channels Group 1		14	A2	Analog Output Channels Group 1
2	A3			15	A4	
3	A5			16	A6	
4	A7			17	A8	
5	GND	GND		18	A1	Analog Output Channels Group 2
6				19	A2	
7				20	A3	
8				21	A4	
9				22	A5	
10				23	A6	
11				24	A7	
12				25	A8	
13						

FLYSYS FlashLamp System

Overview

The Flashlamp System includes a high intensity photic stimulator, lamp driver, and liquid light guide optic. Ideal for standard ERG, Visual Evoked Potential, and Visual Neurophysiology applications, the system features rapid flash rates, variable intensity control, high output, and a spectral range from UV to near infrared.

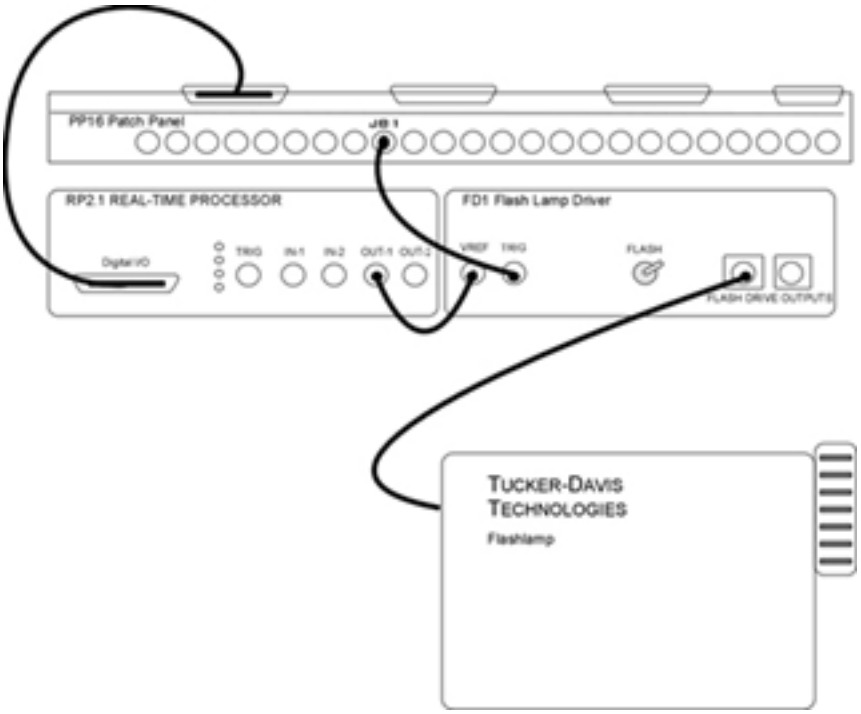
The modular design and supplied 9' cable allows for precise positioning of the Flashlamp (LS1130) and the 1 meter liquid light guide optic (FO1) offers additional positioning and focusing abilities.

Power

The Flash Lamp Driver (FD1) provides power for the flashlamp and can control flashlamps that use their own power supply. The driver is powered via the System 3 zBus (ZB1PS). No PC interface is required for FD1 operation.

System Set-Up

The LS1130 output intensity and rate of stimulation are controlled via the FD1, which receives a variable voltage reference and trigger input from one of the System 3 processors. The diagram below shows how the system would be connected when using an RP2.1 module for control.



System Features

Vref Input Signal

The variable reference voltage controls flashlamp output intensity and can be supplied by any System 3 device with a DC level positive, such as the RP2.1 or RX processors (the RA16BA cannot be used), and must be set high for 10 mSec before the stimulus trigger.

Trig Input Signal

A TTL trigger controls stimulation rate and is typically supplied by a digital output line from one of the System 3 processors, such as the RP2.1 or RX6. Alternatively, the trigger line can be provided by an external source TTL source with a maxium voltage of 5 V and 1 mSec duration.

Flash Switch

This manual switch can be used to trigger the flashlamp. To trigger the lamp, push the switch up and then press down.

Flash Driver Output (LS1130 or MVS7000)

The Flashdrive LS1130 output will drive the standard LS1130 flashlamp that ships with the FLSYS. The MVS7000 output can be used to control other flashlamps.

Important! Contact TDT for assistance before using any other flashlamps with the FD1.

Flash Intensity

To calculate the flash intensity, use the following equation:

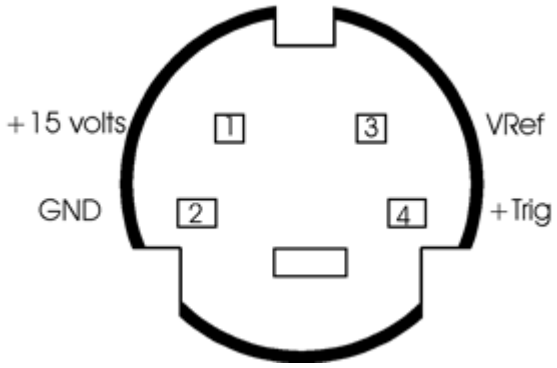
J=1/2(0.50 µF) (Vref∗100)^2

FLYSYS Technical Specifications

Includes FD1 Flash Lamp Driver, LS1130 Flashlamp, and FO1 Liquid Light Guide.

Flash Rate	0.1 - 200 Hz
Flash Duration	10 µsec
Trigger	TTL (5V max)
Flash Intensity (max)	0.235 Joules
Charge Time	30 msec
Spectrum	350 – 800 nm
Input Signal (Vref)	4 – 10 V
Life	10^9 flashes
Power and Communication	zBus required for FD1

LS1130 and MVS7000 Connector Pinout



Note: Connectors are wired the same.

CF1/FF1 Magnetic Speakers

Overview

TDT Magnetic Speakers offer high output and fidelity over a bandwidth from 1 – 50 kHz. These broadband speakers have more power at lower frequencies than our electrostatic speakers, making them well suited for laboratory species with lower frequency hearing. Their high output levels and broad bandwidth also make them excellent for noise exposure studies.

These 4-Ohm magnetic speakers are available in either free-field or closed-field models. The free-field model delivers signals of over 100 dB SPL with < 1% distortion over its entire bandwidth (+/- 4 V, 10 cm). The closed-field model has an internal parabolic cone designed to maximize output and minimize distortion. Its tapered tip can be inserted directly to the subject's ear or fitted with the provided tubing and used with most standard ear tips.

The FF1 and CF1 magnetic speakers can be driven using either TDT's SA1 or SA8 stereo amplifiers. The speaker input is connected via a BNC connector, which carries both bias and signal voltages from the stereo amplifier. Both models feature a rugged polymer enclosure with a stable base as well as a built-in, ¼"-20 threaded post for positioning with laboratory mounting hardware.

Part Numbers:

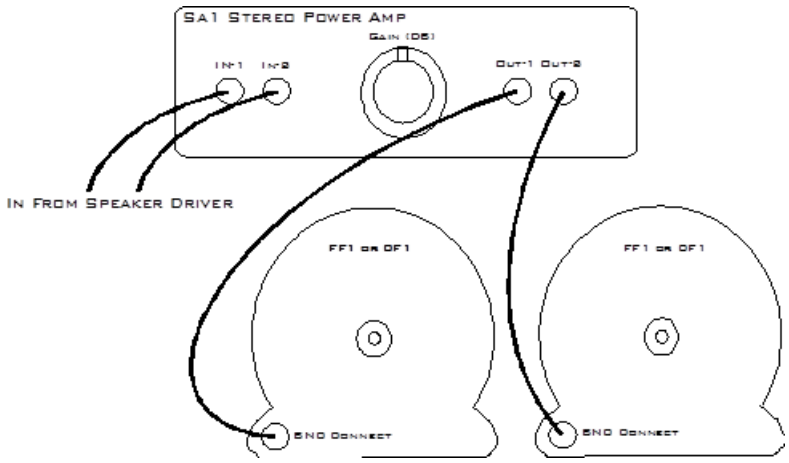
FF1—Free-Field Magnetic Speaker

CF1—Closed-field Magnetic Speaker (Provided with 6" of 1/8" O.D. PVC tubing)

Cable Connection

Connections to the speakers are made through a BNC connector located on the back of the FF1 and CF1 housing. If using the SA1 stereo amplifier, simply connect a

BNC cable from the FF1 or CF1 to one of the output BNC connectors on the SA1 as shown in the following figure.



If you are using the SA8 See *"SA8 Eight Channel Power Amplifier " on page 17-29*, for more information.

Routine Care and Maintenance

Inspect speakers for visual damage prior to use. Exposure to high temperatures will damage the speaker. The polymer used to construct the speaker's housing is very durable, however prolonged pressure, such as supporting the weight of the CF1 with the speaker's parabolic cone, may alter the original structure of the cone causing possible distortion and undesirable effects.

Unlike the closed-field model the free-field model's speaker is exposed and should be carefully handled. Sharp objects could puncture the speaker membrane causing damage to the unit.

If there is damage to the BNC connector or the speaker housing, contact TDT for an RMA for repair.

Closed Field Speaker Design Considerations

All speaker configurations should be calibrated to your specific configuration. If you are planning to deliver tone stimuli, SigCalRP can be used to normalize the desired stimulus signals. For questions about normalizing other types of stimuli, contact TDT.

When using the CF1 speaker for experiments the provided PVC tubing will transfer the signal best when it is kept straight. Note that the speaker performance is dependent on the coupling system used and the ear of the subject. Users should

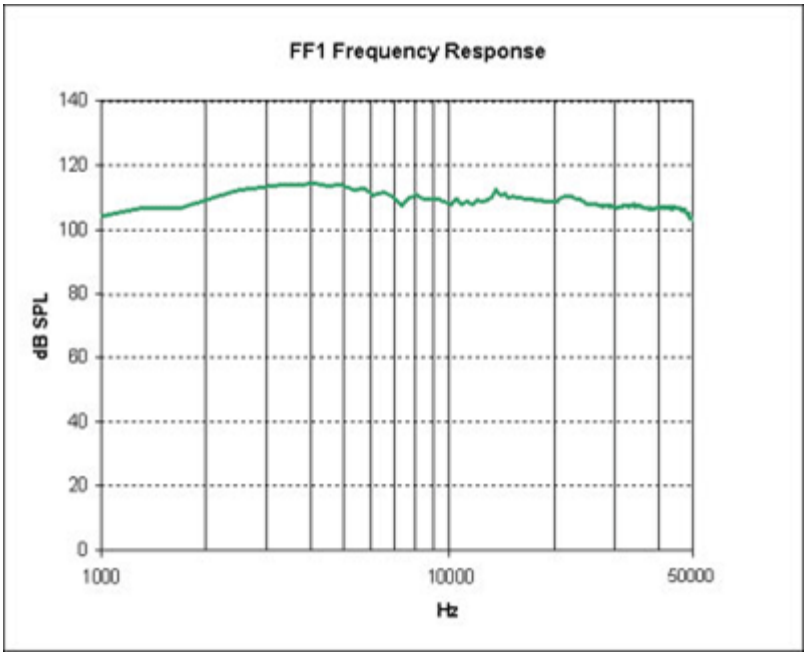
test the device under experimental conditions to ensure it meets their requirements. Technical Specifications measured under specific controlled conditions are provided for comparison purposes.

Technical Specifications

FF1 Technical Specifications

Crossover Frequency	500 Hz High Pass
Weight	~550 Grams
Dimensions	7.62 cm outside diameter x 3.81 cm deep
Typical Output (+/- 1 V peak input)	108 dB SPL at 10 cm from 1 kHz to 50 kHz
THD	<= 1% from 1kHz to 50 kHz
Impedance	4 Ohms

Free-field Frequency Response at 10 cm

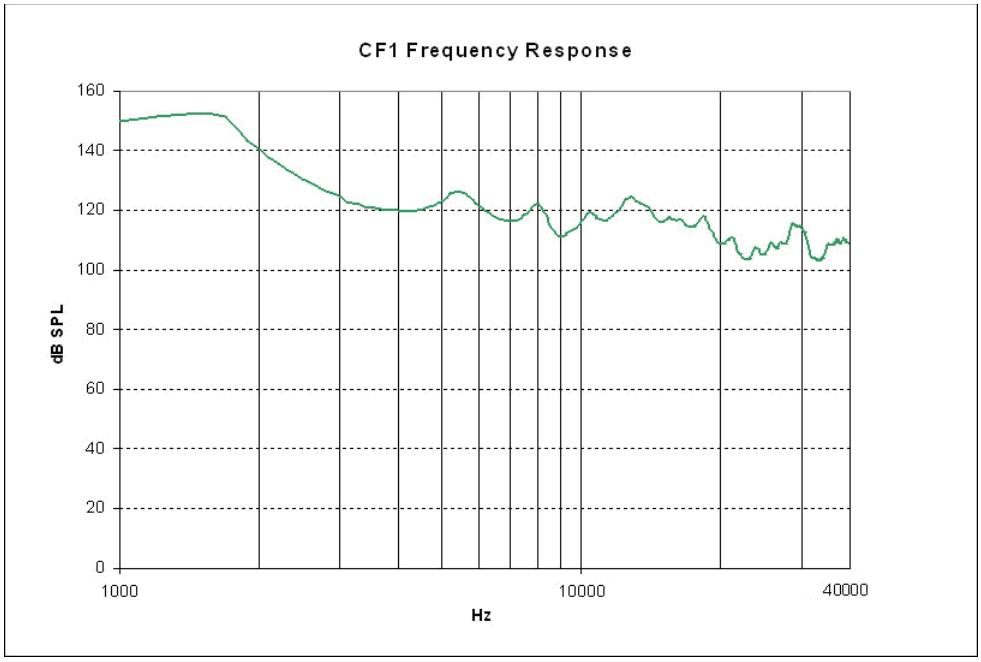


FF1 measurements typical at 10 cm using +/- 4V input.

CF1 Technical Specifications

Crossover Frequency	500 Hz High Pass
Weight	~590 Grams
Dimensions	7.62 cm outside diameter x 8.89 cm deep
Typical Output (+/- 1 V peak input)	120 dB SPL from 1 kHz to 40 kHz
THD	<= 1% from 1kHz to 40 kHz

Closed-field Frequency Response



CF1 measurements typical for approx 0.1cc pvc tube coupler using +/- 1V input.

Part 18: Behavioral Interfaces

RBOX Response Box

The RBOX has four buttons for user response and four LEDs that can be used to provide a subject with feedback. This small, lightweight response box is an affordable solution for collecting simple subject response data. The RBOX is intended for use as part of a TDT system with a compatible real-time processor providing control and response acquisition. There are several versions of the RBOX, each customized for a particular processor.

Part numbers:

RBOX—Response Box for RP2.1

RBOX4—Response Box for PI2, RM1, or RM2

RBOX_RX6—Response Box for RXn

RBOX_RZ6—Response Box for RZ6

Software Support

PsychRP and SykoFizX software applications for psychophysics provide support for the RBOX. The response box can also be used with custom designed software developed using RPvdsEx and TDT's ActiveX or OpenDeveloper tools.

Note: More information on RBOX operation can be found in the *PsychRP Help*.

Connecting the RBOX to the Processor

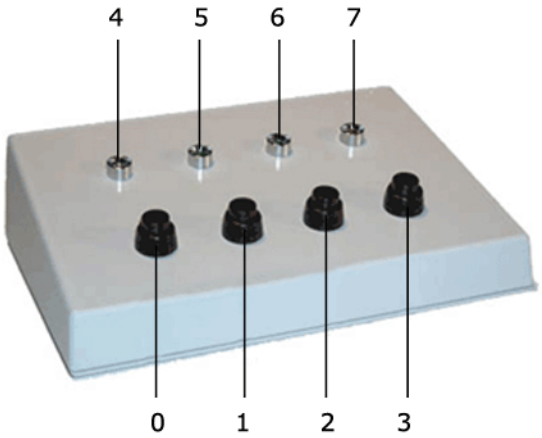
The RBOX must be connected to Digital I/O port on the controlling processor, using the provided cable. The Digital I/O ports on the RP2.1, RXn, and RZ6 (serial numbers ≥2000) use a DB25 connector. The Digital I/O ports on the RM1/RM2 and RZ6 (serial numbers < 2000) use a DB9 connector.

Note: If you are using the RZ6s serial number < 2000 (with a DB9 connector), contact TDT support for assistance.

The RM1/RM2, RXn, and RZ6 processors require additional RPvdsEx software configuration for use with the RBOX. See the corresponding sections below for device specific information.

Buttons and LEDs

The buttons and LEDs are numbered as follows.



Button Number:	BitIn Mask Value:	LED Number:	BitOut Mask Value:
0	M=1	4	M=16
1	M=2	5	M=32
2	M=4	6	M=64
3	M=8	7	M=128

Note that the logic on the inputs to the RP/RM/RX processors is reversed. Therefore, when polling the lines to determine if a button has been pressed, a logic high or '1' means that no button is pressed and a logic low or '0' indicates a button press.

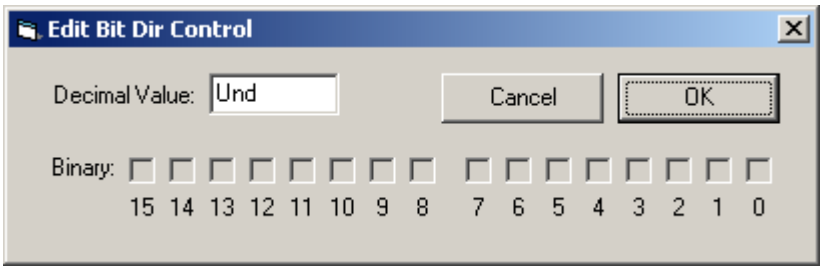
Contact TDT for assistance with custom button or LED configurations.

Configuring an RM Processor for the RBOX4

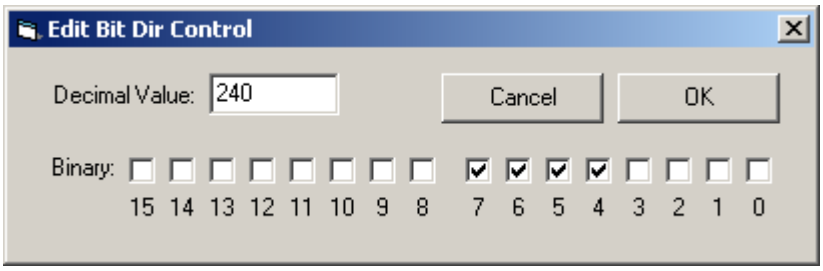
The RBOX4 uses the ground connection (pin 1) and the 8 bits of digital I/O on an RM-series processor Digital I/O port. Bits 0 through 3 are used as button inputs and Bits 4 through 7 are used as LED outputs.

To use the response box with an RM processor, configure the bits in the RPvdsEx configuration register as follows:

1. Click the **Device Setup** command on the **Implement** menu.
2. In the **Set Hardware Parameters** dialog box, click the **Type** drop-down box and select either the **RM1** or **RM2** from the list.
3. The dialog expands to display the **Edit Bit Dir Control** dialog box.
4. Click **Modify** to display the **Edit Bit Dir Control** dialog box. In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.



5. To enable the check boxes, delete **Und** from the **Decimal Value** box and enter **240**. This configures Bits 4 through 7 as outputs.



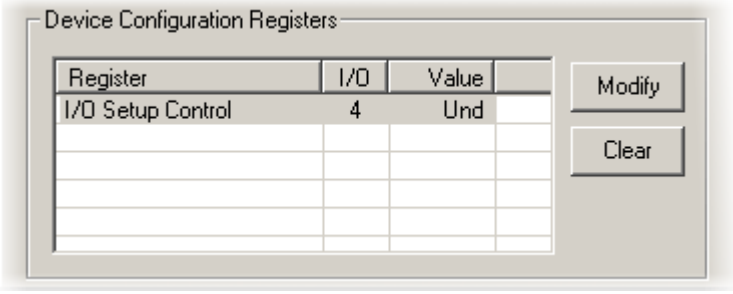
6. When the configuration is complete, click **OK** to return to the **Set Hardware Parameters** dialog box.

Configuring an RX Processor for the RBOX_RX6

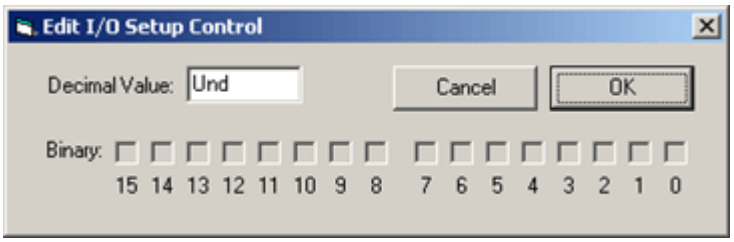
The RBOX_RX6 uses the ground connection (pin 5) and the 8-bits of bit-addressable digital I/O on an RX-series processor Digital I/O port. Bits 0 through 3 are used as button inputs and Bits 4 through 7 are used as LED outputs.

To use the response box with an RX processor, configure the bits in the RPvdsEx configuration register as follows:

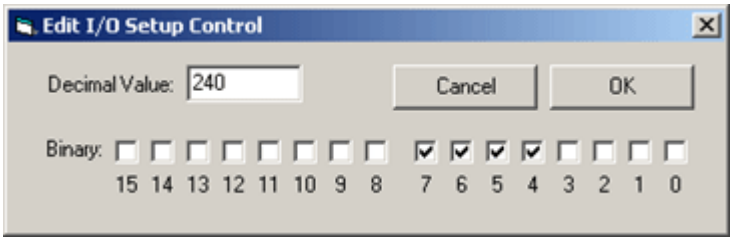
1. Click the **Device Setup** command on the **Implement** menu.
2. In the **Set Hardware Parameters** dialog box, click the **Device Type** box and select any RX device from the list.
3. The dialog expands to display the **Device Configuration Register**.



4. Click **Modify** to display the **Edit I/O Setup Control** dialog box. In this dialog box, a series of check boxes are used to create a bitmask that is used to program all bits.



5. To enable the check boxes, delete **Und** from the **Decimal Value** box and enter **240**. This configures Bits 4 through 7 as outputs.



6. When the configuration is complete, click **OK** to return to the **Set Hardware Parameters** dialog box.

Configuring the RZ6 Processor for the RBOX

The RBOX_RZ6 uses the ground connection (pin 5) and the 8-bits of bit-addressable digital I/O on an RZ6 Digital I/O port. Bits 0 through 3 (see "Buttons and LEDs" on page 18-3) are used as button inputs and Bits 4 through 7 ("Buttons and LEDs" on page 18-3) are used as LED outputs.

To use the response box with an RZ6 processor, use RPvdsEx BitIn and BitOut components to address the buttons and LEDs.

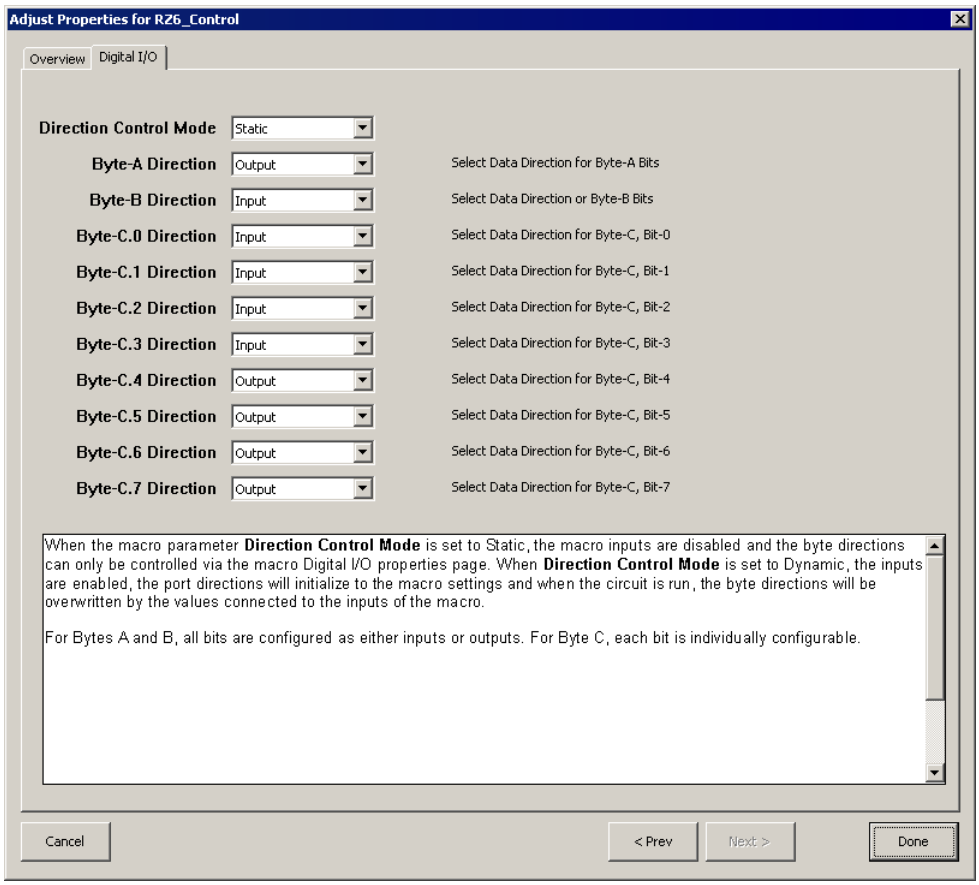
Note: Logic inputs are Logic-High by default with open circuit (button not pressed). A button press shorts the input, causing a Logic-Low state.

The bit-addressable digital I/O lines can be either inputs or outputs. By default, all are configured for inputs. Modifying the RZ6_Control macro will enable Bits 4-7 to be outputs for driving the LEDs of the RBOX.

To configure the RZ6_Control macro:

1. In RPvdsEx, under the **Components Menu**, choose **Circuit Macros**.
2. Navigate to **Device\RZ6_Processor** and choose **RZ6_Control**.
3. Click **Insert** and click the circuit to place the macro.
4. Double-click the newly placed macro to open its properties.
5. Choose the **Digital I/O** tab.
6. Select Output for bits 4, 5, 6, and 7 to set them all as outputs, as shown below.

   Byte-A and Byte-B are not used with the RBOX so they can be inputs or outputs, either value will have no effect.



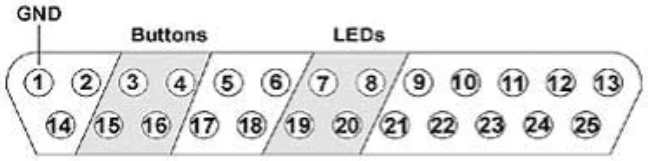
Response Box Technical Specifications

RBOX, RBOX_RX6, and RBOX_RZ6 Specifications

Response Box for RP2.1, RXn, and RZ6.

Buttons	4
LEDs	4
Connection	25-pin **Note:** RBOX_RZ6, serial numbers <2000, use a DB9 Connector. See "RBOX4 DB9 Connector Pinout" on page 18-8.
Cable Length	6'

RBOX DB25 Pinout



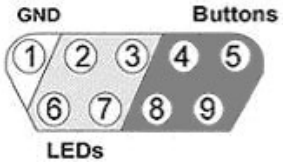
Pins	Name	Description		Pins	Name	Description
1	GND	Ground		14	NA	Not Used
2	NA	Not Used		15	B0	Button Bit 0
3	B1	Button Bit 1		16	B2	Button Bit 2
4	B3	Button Bit 3		17	NA	Not Used
5	NA	Not Used		18		
6				19	L0	LED Bit 0
7	L1	LED Bit 1		20	L2	LED Bit 2
8	L3	LED Bit 3		21	NA	Not Used
9	NA	Not Used		22		
10				23		
11				24		
12				25		
13						

RBOX4 Technical Specifications

Response Box for RM1, RM2, or PI2.

Buttons	4
LEDs	4
Connection	9-pin
Cable Length	6'

RBOX4 DB9 Connector Pinout



Pin	Name	Description		Pin	Name	Description
1	GND	Ground		5	B0	Button Bit 0
2	L2	LED Bit 2		6	L3	LED Bit 3
3	L0	LED Bit 0		7	L1	LED Bit1
4	B2	Button Bit 2		8	B3	Button Bit 3
5	B0	Button Bit 0		9	B1	Button Bit 1

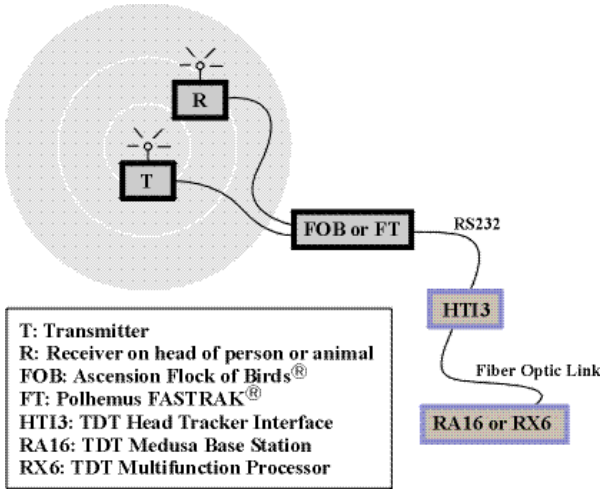
HTI3 Head Tracker Interface

Overview

The HTI3 is an interface between your System 3 processor and either the Polhemus FASTRAK® or Ascension Flock of Birds® or miniBIRD® motion trackers and can acquire X, Y, and Z coordinates as well as azimuth, elevation, and roll (AER) data from two receivers/sensors. A boresight signal can be used to zero the AER values to a relative position. This can be accomplished by a manual button press on the front panel of the HTI3 or from an external 3V digital source via the boresight input BNC.

Data can be transferred directly to any System 3 processor with a fiber optic input, bypassing the host computer and enabling movement and positional information to be integrated into experiments in real-time without any increase in latency. Positional information from motion trackers can be efficiently stored and synchronized with biological signals such as EMG, EEG and extracellular neurophysiology or used to update a 3D audio signal presentation in real-time.

The HTI3 parses the incoming signals from the motion tracker into the following data components:



Receiver #: Each HTI3 can handle up to 2 channels of motion tracker receivers.

Error code: The HTI3 will generate four channels that encode the decimal error codes from the Fastrack motion tracker.

XYZ coordinate space: The HTI3 will generate three channels of coordinate space distance from each receiver in either inches or centimeters based on information from the motion tracker.

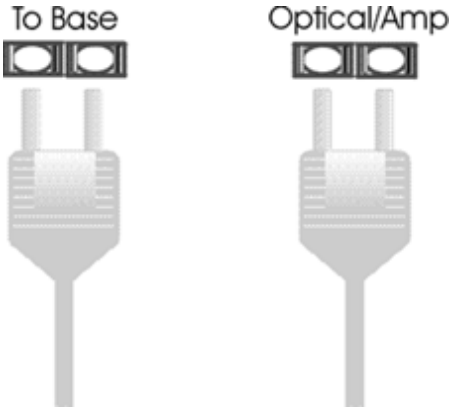
Azimuth, Elevation and Roll (AER): The HTI generates three channels of AER information for each receiver based on signal information from the motion tracker.

Note: The XYZ space is absolute distance from the transmitter while the AER information is relative to the boresight point.

The raw HTI3 output signals must be scaled to achieve the appropriate signal range before the data can be used. Special processing must be implemented in RPvdsEx to perform the necessary scaling and to reduce redundancy in the data. See "HTI3 Circuit Design" on page 18-11, for more information about this processing and techniques for using the data with HRTF filter components.

Power and Interface

The device is powered via the System 3 zBus (ZB1PS) and requires an interface to the PC. If the HTI3 is housed in one of several ZB1PS chassis in your system, ensure that it is connected in the interface loop according to the installation instructions: Gigabit, Optibit or USB Interface.



To Base

The HTI3 sends information to the base station over a fiber optic cable. When connecting the HTI3 to a base station, make sure that the fiber optic cable is connected as shown to the right.

HTI3 Features

Reset/Boresight

Pressing the Reset/Boresight button momentarily will issue a boresight command to the tracker unit. This signal will zero the AER values respective to the boresight position. Holding the button down for one second will issue a reset command to the tracker unit and undo the boresight command. The AER values will now be returned with respect to the default initial positioning.

To Tracker

The To Tracker DB9 input connects the motion tracker to the HTI3.

Note: When using the FOB or miniBIRD® motion tracker, data will be properly transferred to the interface if only pins 2, 3 and 5 are connected. A special connector is shipped with the HTI3 to make this transition from the RS232 cable to the tracker. This connector also performs the required RS232 gender change.

Polhemus/FOB

The toggle switch is provided to select between the FT or FOB motion tracker. This switch must be in the correct position on power up of the HTI3 for correct operation.

Using the miniBIRD® Set to FOB

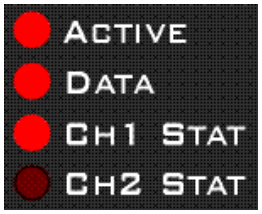
The miniBIRD® tracker must be set to Normal Addressing Mode and the DIP settings should be configured as below:

1	2	3	4	5	6	7	8
ON	ON	ON	OFF	OFF	OFF	ON	OFF

Boresight

A boresight command can be issued from an external 3V digital source via the Boresight BNC input. This signal needs to be a logical high ('1') pulse of at least 200 ns in length. The signal then needs to be set logic low ('0') for at least 200 ns before another boresight command can be issued.

Activity Lights



Active

The Active LED indicates if the HTI3 is connected to a base station via a fiber optic cable. This LED will flash slowly (~1 Hz) if this connection is not properly made.

Data

The Data LED indicates if the HTI3 is receiving data from the motion tracker unit. This LED will also flash slowly (~1 Hz) if the tracker is not properly connected to the HTI3.

CH1 Stat/Ch2 Stat

The Ch1 Stat and Ch2 Stat LEDs indicate if the interface is receiving data from receiver 1, receiver 2 or both. The figure below shows the LED pattern for the HTI3 properly connected to a base station and a motion tracker while acquiring data from receiver 1.

HTI3 Circuit Design

The HTI3 parses incoming signals from a motion tracker into 16 channels of data and sends it to a base station (such as RZ5, RX6, or RA16BA) at rates up to 25 kHz. Most motion trackers send data at a slow rate (~120 Hz). This means that there is a large amount of redundancy in the data acquired by the base station. The circuit designs described below will reduce the resulting redundancy and convert the raw HTI3 output signals into useful information such as error codes, distance measures and relative positional information such as Azimuth, Elevation, and Roll.

Acquiring and Scaling Motion Tracker Signals

Motion tracker signals are acquired via a fiber optic cable connecting the HTI3 to a base station. The most common signals input via the fiber optic port are biological signals amplified using one of the TDT preamplifiers; so all signals input through one

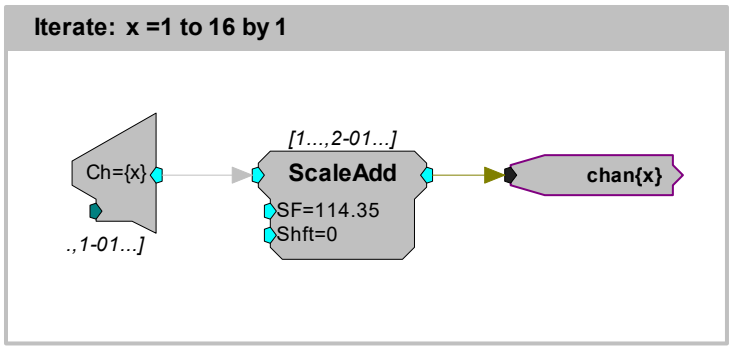
of these ports are automatically scaled accordingly. When the fiber optic inputs are used to acquire signals from other devices, such as the HTI3, the signals must be scaled according to the signal characteristics of the specific device. With the HTI interface, the signal from each channel must be scaled by 114.35. This adjusts the signal to a range of +/- 1.0 V. Additional scaling is required to convert signals on some input channels to the appropriate units or values. The table below describes the scale factor(s) for each signal input from the HTI3 and for each device.

Device	Receiver	Chan.	Data	SF (base)	SF (cm) or SF(ASCII) for err	SF (in)	SF (rad)	SF(deg)
FT	1	1	Azm	114.35	NA	NA	3.14159	180
		2	Ele		NA	NA	3.14159	180
		3	Roll		NA	NA	3.14159	180
		4	X		300	118.11	NA	NA
		5	Y		300	118.11	NA	NA
		6	Z		300	118.11	NA	NA
	2	7	Azm		NA	NA	3.14159	180
		8	Ele		NA	NA	3.14159	180
		9	Roll		NA	NA	3.14159	180
		10	X		300	118.11	NA	NA
		11	Y		300	118.11	NA	NA
		12	Z		300	118.11	NA	NA
	1	13	err		16384.2			
		14	err		16384.2			
		15	err		16384.2			
		16	err		16384.2			
FOB	1	1	Azm	114.35	NA	NA	3.14159	180
		2	Ele		NA	NA	3.14159	180
		3	Roll		NA	NA	3.14159	180
		4	X		91.44	36	NA	NA
		5	Y		91.44	36	NA	NA
		6	Z		91.44	36	NA	NA
	2	7	Azm		NA	NA	3.14159	180
		8	Ele		NA	NA	3.14159	180
		9	Roll		NA	NA	3.14159	180
		10	X		91.44	36	NA	NA
		11	Y		91.44	36	NA	NA
		12	Z		91.44	36	NA	NA
	1	13	NA					
		14	NA					
		15	NA					
		16	NA					

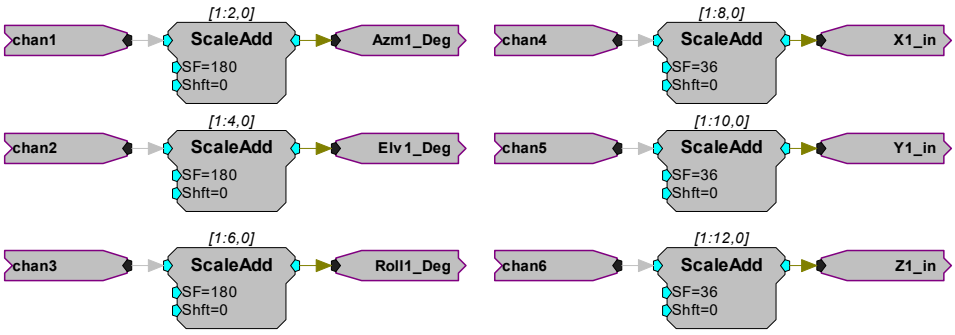
Note: The scale factor for the FT error codes converts the values to ASCII codes.

These scale factors must be incorporated into any circuit design. The circuit below performs the initial scale factor. The circuit uses the iterate function to efficiently scale all 16 channels. The circuit uses only single processor components and works

on all devices. The iterate function duplicates the construct 16 times, with an input signal from channel 'x' scaled by 114.35 and then sent to a hop out.



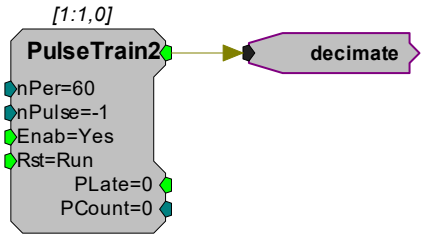
The next circuit segment scales each channel based on the table above for the FOB motion tracker. The first three channels in this example scale Azimuth, Elevation, and Roll. If the input to the HTI3 includes two motion tracker channels, then channels 7, 8 and 9 will contain the Azimuth, Elevation, and Roll information for the second motion tracker. To return this information in radians, the scale factor should be changed to 3.14159. Channels 4-6 are scaled to inches. To scale the XYZ coordinate space to centimeters the scale factor would be 91.44. This circuit can be easily modified to use with the FT motion tracker by inserting the appropriate scale factors from the table above.



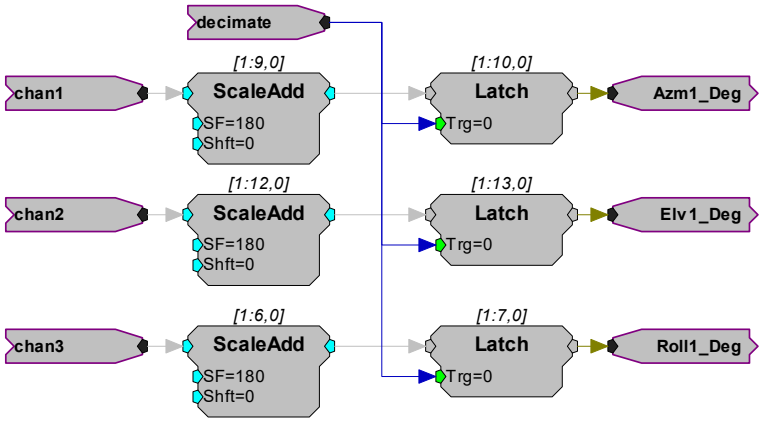
Data Storage and Visualization of Signal Input

Motion tracker signals are updated/transferred to the HTI3 at rates up to 120Hz. The HTI3 sends signals to the RX/RP device at sample rates up to 25 kHz. This means that each value from the motion tracker may be repeated on the DSP up to 200 times. To minimize the redundancy of the signal, the channel outputs can be decimated by a fixed value. This will decrease the amount of data stored on either the DSP or transferred to a computer. The construct below shows two ways to decimate the signal. One way shows real-time visualization of the signal and the other illustrates storage of the signal to disk.

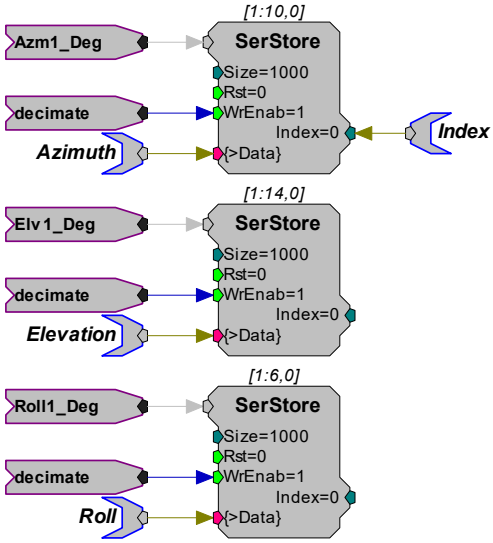
Since the following circuit segments are based on the data transfer rate of the motion tracker itself, users should review the documentation provided with their device before using the parameter values shown.



The PulseTrain2 component sends out a pulse every 60 samples. The output from the PulseTrain2 is sent to the Trigger line on a latch. Therefore the output from the latch is updated once every 60 samples. This generates an updated output that more closely matches the data transfer rate of the motion tracker. The output can then be sent to a head related transfer function (HRTF) coefficient generator (see "Using the HTI3 with HRTF Filters" on page 18-15).

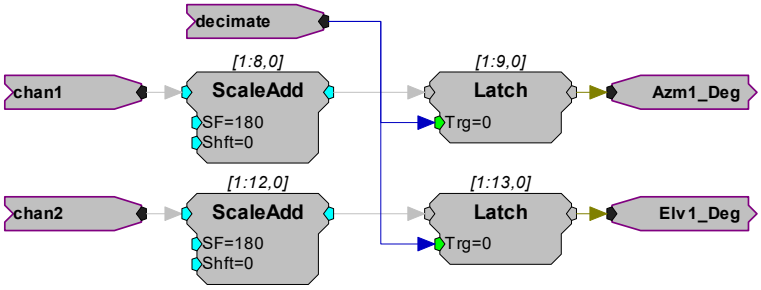


Another way to use the decimated signal would be to send it to a Serial Buffer input. In this case the values are stored once every 60 samples. If you were using this with OpenEx this would be the primary way to save the data set.

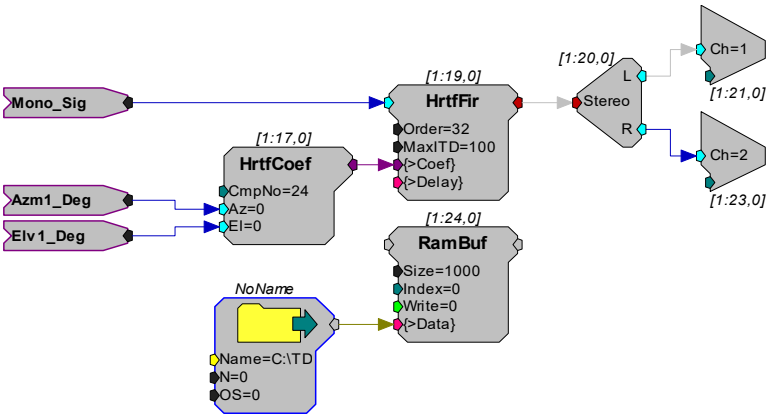


Using the HTI3 with HRTF Filters

One great advantage of the HTI3 setup is that users can connect the device to an RX6 Multifunction Processor. With the RX6 system, a virtual 3D audio environment can be generated. The following circuit uses the Azimuth and Elevation information to change the perception of a signal input. Channels 1 and 2 are latched via the PulseTrain2 decimation construct discussed earlier.



The output of the HTI3 is sent to an HRTF filter that converts the mono input into a stereo output that can be sent to Headphone buffers etc. A random access buffer stores the HRTF filter values.



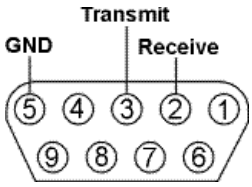
About the Sample Circuit

The sample circuit HTIFLOCKOFBIRDS.rpx illustrates the scale factors for all incoming channels from the FOB motion tracker. Page 0 shows the initial scaling and the secondary scaling for channels 1-3 (deg) and 4-6 (in). Page 1 shows the scaling of the channels relating to the optional 2nd motion tracker input (channels 7-12).

HTI3 Technical Specifications

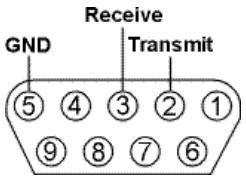
Max update rate	120 Hz
Boresight trigger	External
RS232 acquisition rate	115 kbaud

To Tracker - DB9 Pinout for Ascension Flock of Birds®



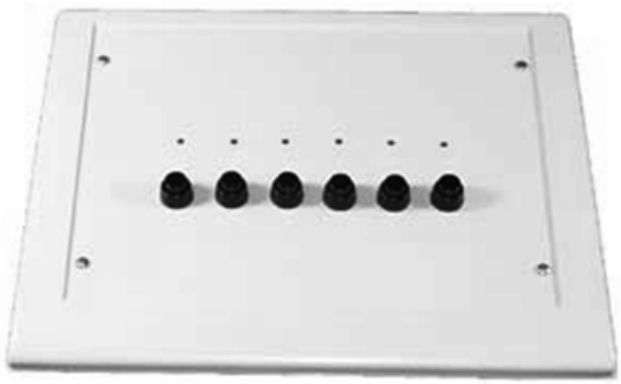
Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		6	NA	Not Used
2	Receive	Serial Receive Line		7		
3	Transmit	Serial Transmit Line		8		
4	NA	Not Used		9		
5	GND	Ground				

To Tracker - DB9 Pinout for Polhemus FASTRAK®



Pin	Name	Description		Pin	Name	Description
1	NA	Not Used		6	NA	Not Used
2	Transmit	Serial Transmit Line		7		
3	Receive	Serial Receive Line		8		
4	NA	Not Used		9		
5	GND	Ground				

BBOX Button Box



BBOX Overview

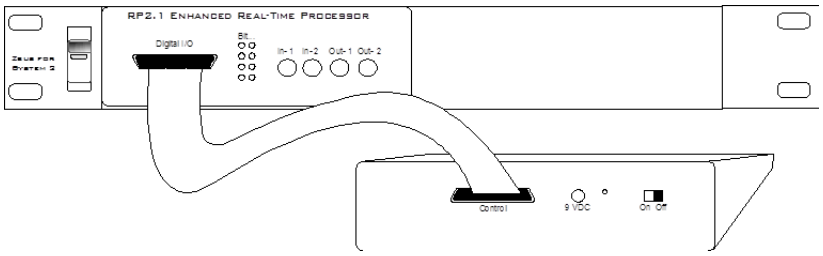
The button box is a complete subject response interface. It is an excellent system for psychoacoustics, including n-alternative forced choice, GO NO GO, Bekesy style presentation, and modified method of limits experiments. The button box provides accurate reliable performance. All inputs are debounced in the button box and a built-in rechargeable lithium-ion battery provides power for up to 24 hours of continuous use per charge.

The standard button box configuration includes six buttons and six high intensity LEDs. However, the button and LED organization can be configured to user specification. The button box can have up to eight buttons and 32 LEDs. The button box design allows experimenters a great deal of flexibility to control feedback based on subject response, reinforcing behavior for correct and incorrect choices.

The button box can be controlled from an RP2.1 or RV8 processor with button response acquisition and LED control through the digital input/output port of these modules. Data can be latched and then read from specialized RPvdsEx circuits using ActiveX and Matlab, or other programming languages. RPvdsEx circuits designed for button box control can be used with all TDT software.

Connecting the Button Box to the RP2.1 or RV8

The button box is controlled using the RP2.1 or RV8 processor. The button box connects from the DB25 connector (Control) directly to the digital input/output port on the RP2.1 or RV8 with the supplied ribbon cable. The button box is configured at the factory for the RP2.1. It can be configured for the RV8 by installing a jumper pin (Jumper for RV8) on the back of the button box.



RP2.1 to BBOX Connection

Power Requirements

The button box is supplied with a 3.3 Volt lithium-ion battery pack. This high current battery should provide up to 24 hours of continuous use per charge. The lithium-ion battery charges in under three hours with the supplied 9 Volt battery charger. The ON/OFF switch, the power connection for the battery charger, and a power indicator light are found on the back of the button box. The Power/(Low Bat) LED lights when the button box is on and flashes if the battery is low.

Important! To operate any features of the button box the power must be turned on and the device must be connected to an RP2.1 or RV8 that is powered on and connected to a PC.

Caution !

A low battery may give erroneous results. If the battery is low, the battery charger can be connected to the device. This will charge the battery and power the box at the same time.

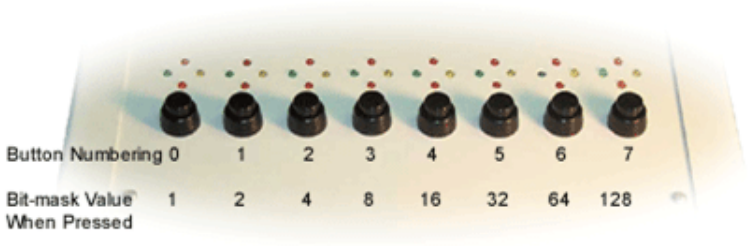
BBox Control

LEDs can be controlled and button presses can be acquired by including the necessary circuit segments in the RPvdsEx circuit that will be run on the controlling device. The button box can also be controlled using ActiveX and Matlab, or any programming language that supports ActiveX. Before designing or debugging circuits for the button box, ensure that the button box is connected to the RP2.1 or RV8 that will be used for control and that the button box power is turned on. The buttons will only operate when the button box is powered.

The remaining button box help topics provide the necessary information for basic button box control, including circuits that acquire button responses and test for correct or incorrect responses to button presses. The information provided assumes some knowledge of RPvdsEx and possibly ActiveX. Users with custom built button boxes should modify circuits based on the configuration of the buttons.

Acquiring BBox Button Presses

The most efficient way to acquire button presses is with the WordIn component in RPvdsEx. The WordIn checks all the digital input lines and returns a 16-bit value from the digital line addressed. Input values are generated as a bit-mask that determines which buttons were pressed. Users can also record the inputs from the individual digital I/O lines. The RPvdsEx examples in this topic use the WordIn method.

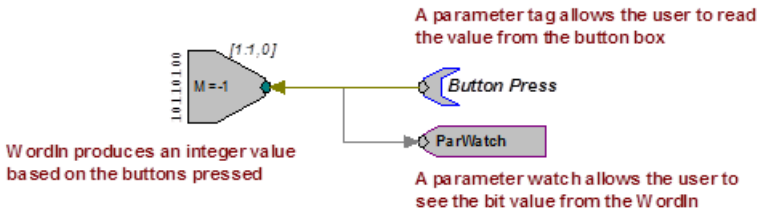


BBox Organization of Buttons

Note: The button box power supply must be turned on for the buttons to operate.

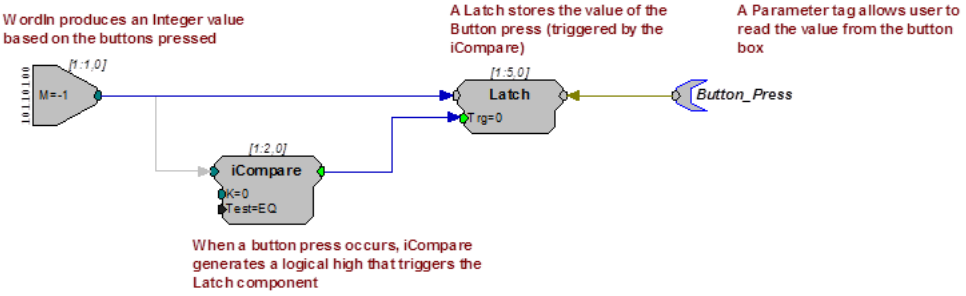
Many of the circuits shown below, as well as some MATLAB examples for use with ActiveX controls, are included with RPvdsEx (RPvdsEX | Examples | ButtonBox).

A simple circuit for acquiring button presses...



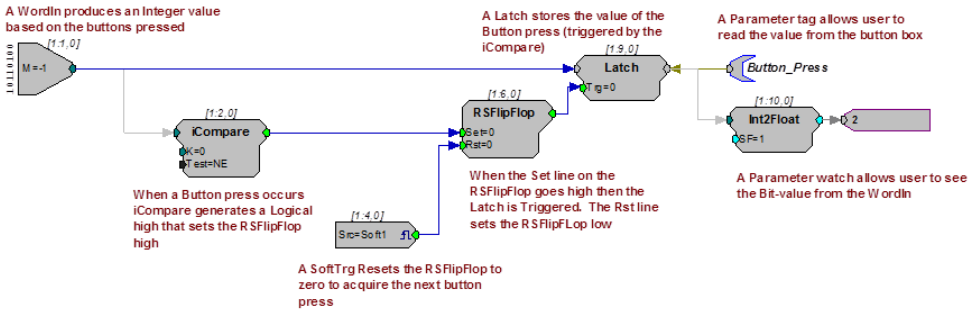
In this example, the user would continuously poll the component, from a program that acquired the value from the ButtonPress parameter, to determine which buttons are pressed. A simple circuit like this may be required if the RP2 that controls the button box is also used for stimulus presentation.

A more likely circuit design for button acquisition...



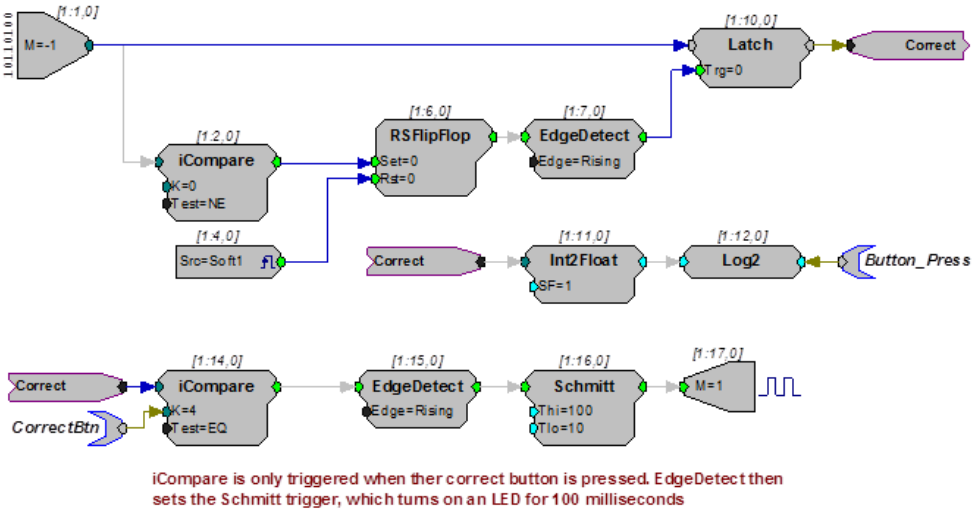
In this example, the WordIn produces an integer value based on the buttons pressed. When a button press occurs, an iCompare generates a logical high that triggers the Latch component. The Latch stores the value of the button press until the next button press occurs. The Button_Press parameter tag allows the user to read the value from the button box. If only the first button press is important then a reset line should be included in the circuit to rest the Latch.

Resetting the Latch...



In the previous examples all button presses are acquired, that is, if a person presses buttons simultaneously there is the chance that both responses will be obtained. This will happen infrequently with circuits that use an iCompare and Latch, but it is still possible. In some cases the user will want to determine if the proper button press was acquired or wait until a particular button press has happened. Additional circuitry can be added that checks for this.

Identifying the correct button press...



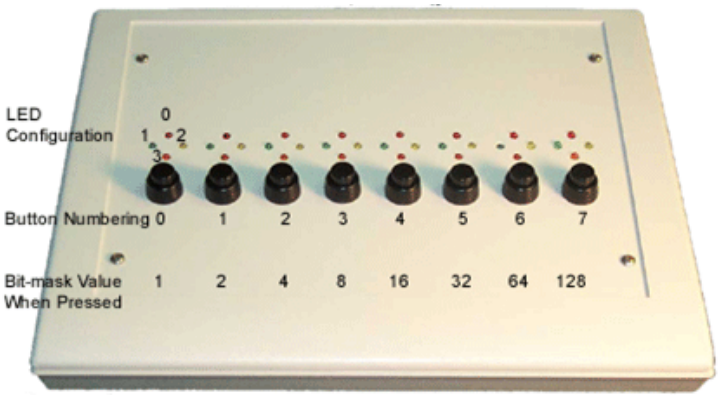
In this example, the top part of the circuit detects if a button is pressed. The button press value is also translated into a value representing which bit was read. For example, if the bit in bitmask value is 16, then Log2 converts the value to 4. This lets the user determine, via the Button_Press parameter tag, that bit 4 was high.

The lower part of the circuit tests to determine if the correct button was pressed. If so, an LED is flashed. A parameter tag is used to identify the correct button press. The iCompare is only triggered when the correct button is pressed. The EdgeDetect component then sets the Schmitt that turns on the first LED for 100 milliseconds.

Button box circuits can be incorporated in to all TDT System 3 software. For information on using the button box with other applications please see that application's documentation. If you have questions about how to design your own applications for the button box call 386-462-9622 for technical assistance.

Controlling the LEDs

Their are several methods to control LEDs. The button box may have up to four LEDs for each button and each LED can be turned on and off independently of any other. Using the LEDs involves two steps: 1) designating the LED to turn on or off and 2) turning the LED on and off. LEDs are designated by specifying the column (button number) and position (LED number).



BBox Organization of LEDs and Buttons

Bit Patterns Table

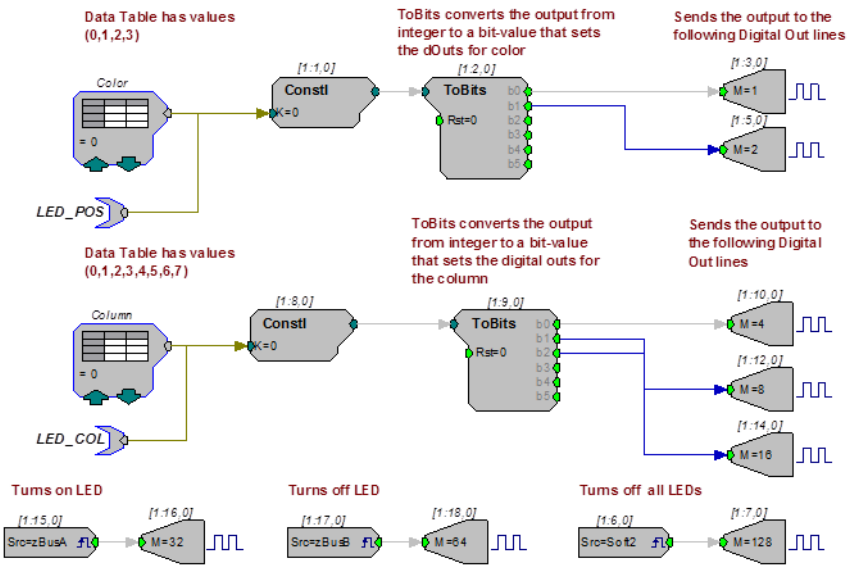
Selecting an LED	
Bits 0, 1:	Control the position within a column
Bits 2, 3, 4:	Control which column is selected
Turning on/off LEDs	
Bit 5:	Turns on selected LED
Bit 6:	Turns off selected LED
Bit 7:	Turns off all LEDs

Note: Because the button box has its own power supply, the LED's will remain on until they are turned off via the RP2 or RV8 or until the power is turned off.

The circuits shown below, as well as some MATLAB examples for use with ActiveX controls, are included with RPvdsEx (RPvdsEX|Examples|ButtonBox). In the first design the user designates the LED and the button number or column position in two separate steps. In the second the steps are combined. In the final design LED designation and on/off information are combined in a single word.

Designating the LED and button number or column position in two separate steps...

In the example below there are two sets of inputs used to specify the LED. The first controls which LED (LED position within a grouping) is lit while the second controls the column (button location) in which the LED is located. DataTables are used to test and run the circuit within RPvdsEx and parameter tags (LED_POS and LED_COL) are included to allow users to control the position and column values from another application.



To follow along with this example:

- Open the LED1 RPvdsEx file in the ButtonBox example folder (TDT\RPvdsEX\Examples\ButtonBox).

To designating and turn on/off an LED and button:

1. To set the color or position of the LED (0 = Top, 1 = Left, 2 = Right, 3 = Bottom), click the **green up and down arrows** on the DataTable labeled Color.
2. To determine which column the LED is in (0 = Far Left... 7 = Far Right), click the **green up and down arrows** on the DataTable marked **Column**.
3. To turn on the LED, press the **zBusA** trigger button in RPvdsEx. Make sure to click the **pulse**  button for the zTrig. To turn off the LED press the **zBusB**  trigger.

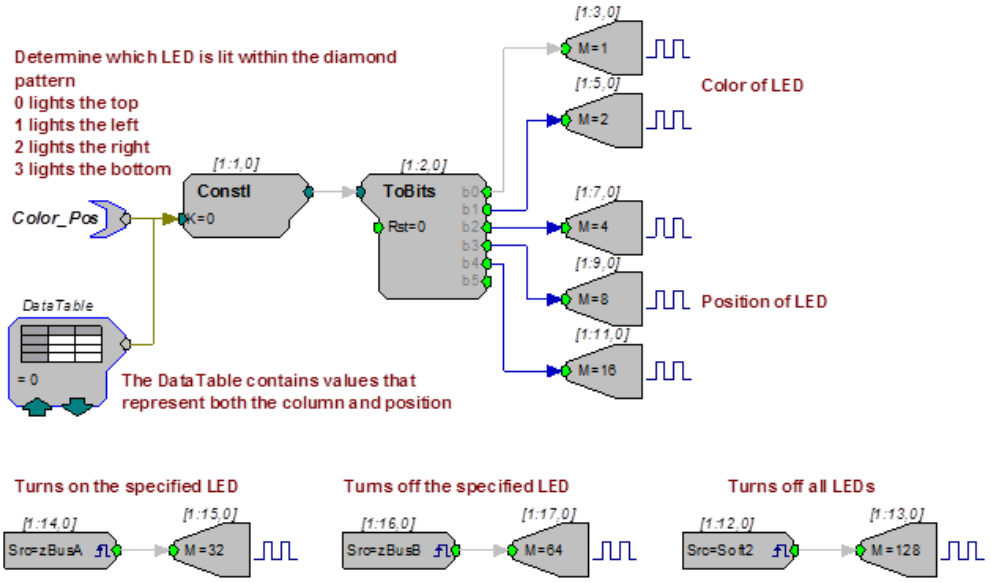
You can select (one at a time) several lights to turn on and off.

For example, to light the top LED in the first column and the bottom LED in the last column perform the following steps:

1. Set the **Color** DataTable to **0** and the **Column** DataTable to 0.
2. Turn on the LED by clicking the **zBusA** trigger button in RPvdsEx. This will turn on the top LED in the first column.
3. Set the **Color** DataTable to **3** and the **Column** DataTable to 7.
4. Click the **zBusB** trigger button in RPvdsEx. Both LED's should now be on.
5. To turn off the latter LED, click the **zBusB** trigger button.
6. To turn off all LEDs, click the **Soft2**  button in RPvdsEx.
7. To turn on all LED's in succession, set the **zBusA** trigger line high  and then cycle through the DataTable values.
8. To reverse the operation set the **zBusA** trigger low  , set the **zBusB** trigger high  , then cycle through the DataTable values.

Combining the position and column setup...

The following example combines the two data tables and uses one ToBits component to control the button box's LEDs.



The single data table used in this example contains values that combine the column and position.

For example:

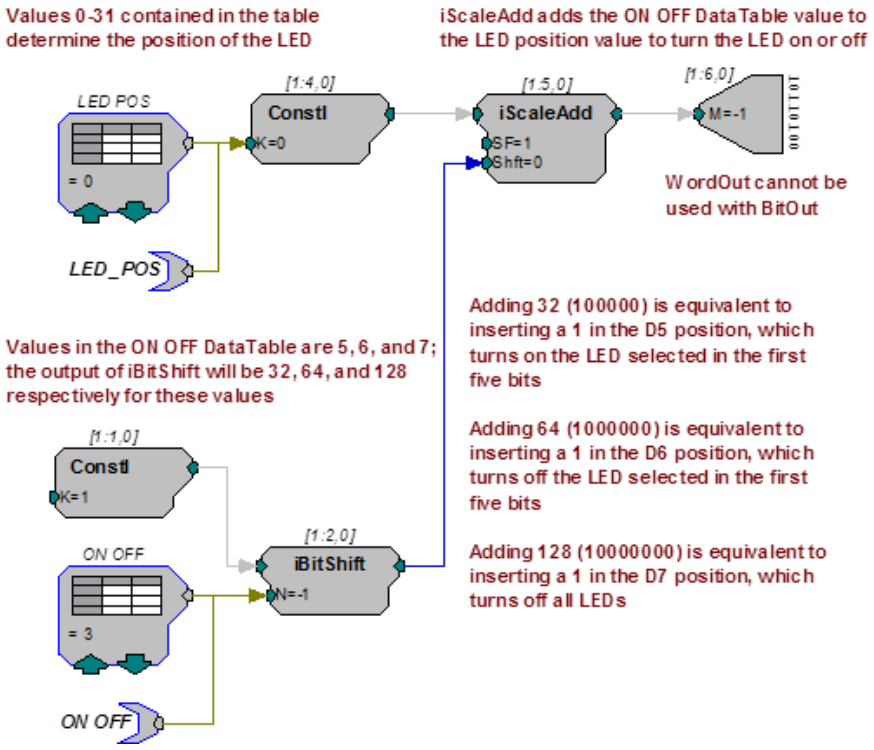
If 28 is used in the data table, the circuit selects the top LED in the seventh column. That's because the top position in the seventh column is represented by the digital number 11100 (as shown below), which equals 28.

Column Select Lines			LED Position Select Lines	
D4	D3	D2	D1	D0
1	1	1	0	0

To learn more about this example, open the LED2 RPvdsEx file in the ButtonBox example folder (TDT | RPvdsEX | Examples | ButtonBox).

Using a WordOut with a DataTable/ParTag for on/off actions...

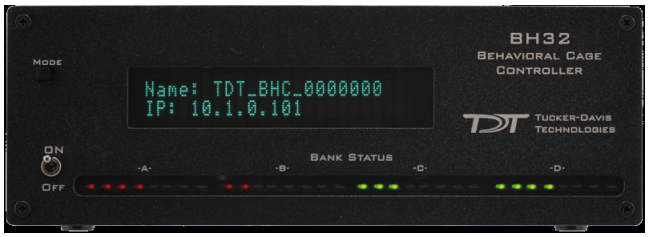
The following example uses the WordOut component similarly to the way the WordIn is used in the button press example. As before, a DataTable is used to determine which LED to light. In the LED POS DataTable, values 0 - 31 are used to determine the position of the LED. In addition, another DataTable is used to set whether the LED is turned ON or OFF, all LED's are turned OFF, or if nothing is done when the LED is selected. This value gets added to the LED position value and is sent out via the WordOut component. The values for the second DataTable are 0 = 0 (nothing done), 1 = 32 (LED ON), 2 = 64 (LED OFF), and 3 = 128 (all LEDs OFF). The cycle usage for this example is half the cycle usage for the one above it. Notice that there are no BitOut components used. The WordOut and BitOut components cannot be used in the same circuit.



Note: See the Bit Pattern Table for a review of how each bit position is used.

This example is found in the LED3 RPvdsEx file in the ButtonBox example folder (TDT | RPvdsEX | Examples | ButtonBox).

BH32 Behavioral Cage Controller



Overview

The BH32 Behavioral Cage Controller integrates neural signals with behavioral inputs and outputs from standard behavioral cages; such as operant conditioning boxes. The device acts as a network appliance that can be used over a LAN to control several behavioral boxes or can be directly linked to a TDT RZ device for integration with neural recordings. The device provides the end user with 32 I/O lines in banks of eight. Each bank can be configured as inputs or outputs. End users can drive standard 5 Volt devices or power the device with an external supply to deliver up to 30 Volts, 3 A.

Features

Molex Pin and Socket Connectors

The BH32 uses 1.57 mm Diameter Standard Molex Pin and Socket connectors on the top panel. For pinouts, see “BH32 Technical Specifications” on page 18-39.

Power

The BH32 logic board is powered by either a 6-9V, 3A center-negative adapter connected to the power input on the back panel of the device or by Power over Ethernet (PoE) through the Ethernet Port (see “Ethernet Port” on page 18-28).

The BH32 Molex outputs can be driven by either the same power source as the logic board (5V) or by an external power source connected to the ‘External Power’ connectors on the top of the device. The ‘External Power’ connectors allow you to drive higher voltages/currents to external devices that require it, One connector can be used to input a 5-30V, 3A external power source that is shared among all Molex output connectors. A toggle switch on the back panel of the device determines which power source is used for the Molex outputs. The Molex connector outputs are always Active-Low.

Important! The two External Power Molex connectors on the top panel are shorted together; do not use more than one external power source. The second external power connector can be used to jumper the external power source to another BH32

Voltage Mode Toggle

This back panel switch toggles between 5 V and external power supply source for all Molex output banks. Use 5 V mode for connections to mains power or PoE. Use External Voltage mode for other external power sources up to 30 V.

Power Source	Mode	Max Total Output
Mains power	5 V	200 mA
PoE	5 V	100 mA
External power up to 30 V	External Voltage	3 A

Power Switch

The On/Off toggle switch turns the BH32 power off or on. The LED display will be illuminated when the power is on.

Status Display

The front panel display screen reports system status. The Mode button to the left toggles the display modes.

The display modes include:

1. Device Number - how the BH32 is recognized on the network by other devices
2. Bank Status - bank direction and current state of all bits in each bank
3. NetBIOS name and IP address
4. IP address of paired RZ device (if paired). See "RZ Configuration" on page 18-30.

Push and hold the Mode button for two seconds then release to automatically cycle through all of the display items, displaying each for one second.

Push and hold the Mode button for 10 seconds to reset the Device Number.

Push and hold the Mode button while powering on the BH32 for 10 seconds to reset the BH32 to factory settings.

I/O Control

The BH32 is a net appliance that was designed to be used under a variety of conditions, not all of which are available from vendors of behavioral control systems.

At the most basic the TDT BH32 system can replace existing devices such as the Med Associates, Colburn or Lafayette systems that interface to a standard operant or behavioral box with input and output lines, where the output lines drive feeders, lick meters and other devices that require more than a digital trigger. At the more complex level the TDT system can be used to send and receive complex signals to control multiple hardware devices.

Replicating an Existing Behavioral Control System

The TDT system provides a unifying interface for sending and receiving behavioral information from a behavioral control box without the need for the external devices from these other companies.

TDT provides a default set up that uses standard Molex pins, an External power source to drive high current and high voltage devices (such as feeders, water delivery systems, foot shock systems, etc) or to accept inputs from such devices. The hardware states of these particular interfacing devices are fixed and the BH32 bank directions and logic levels must be configured to match (see "Digital I/O " on page 18-27).

More Complex Custom System Configuration

Information can be sent and received from the Molex interface in the following ways.

Note: Molex Banks A and B can be used as outputs and only outputs. Molex Bank D can be used as inputs and only inputs. The direction and logic level of each bank is configured through the BH32 web interface (See "Controller Configuration" on page 18-31). When using the BH32 in Synapse, these should be left at their default factory settings.

Important!: Attempting to drive an input from both the digital input and Molex connectors will damage the device.

Controlling the Molex outputs with UDP/Serial (banks A & B only)

Configure the bank as an output. The Molex outputs are high when active.

Monitoring the Molex inputs with UDP/Serial and Digital I/O (bank D only)

Configure Bank D as an input. Active-Low means that when the Molex input is low, the value is 1. The digital output logic mirrors the Molex input logic.

Controlling the Molex outputs with Digital inputs (banks A & B only)

Configure the bank as an input, to bypasses the internal processor and control the Molex lines directly. Molex output logic is the inverse of the digital input.

Using Digital and UDP/Serial I/O only

If the Molex connectors are not being used, then all four banks of digital I/O can be used to send receive signals with the UDP/Serial interface with no restrictions on bank direction.

Digital I/O

The BH32 includes 32 bits of programmable I/O grouped in four 8-bit banks. Digital I/O lines are accessed via the Digital IO-1 and Digital IO-2 25-pin connectors on the back panel. Digital inputs accept +5V TTL inputs. Digital outputs are +5V. For pinouts, see "BH32 Technical Specifications" on page 18-39.

Status Lights

A row of 32 status lights on the front panel report the state of the individual input/output bits and are labeled to show banks A – D. When a bit is active, the corresponding bit light glows red.

Ethernet Port

The Ethernet port allows direct connections to a PC or network for communication over UDP. The BH32 supports Power over Ethernet (PoE) technology using the 802.3AF PD standard. Use of Cat 5 (or greater) Ethernet cable recommended. The BH32 can connect directly to a PC, an RZ device, or a network. If connecting directly to an RZ device, a crossover Ethernet cable is required. See "Legacy BH32 RPvdsEx Circuit Design" on page 18-34, for more information on communicating with the BH32.

RS 232

The BH32 can communicate with other devices over a serial port. See "Legacy BH32 RPvdsEx Circuit Design" on page 18-34, for more information.

DTE – E Switch

This toggle switch determines whether the BH32 serial port is in master or slave mode. This selects which wires on the BH32 serial port will be send and which will be receive.

BH32 Configuration

This section discusses configuring the BH32 networking communication and hardware interfaces. See "RZ-UDP Communications Interface" on page 1-51, for more information on the basics of networking and the various protocols.

Initialization

The BH32 will attempt to locate a DHCP server that will dynamically assign an IP address to the device.

If no DHCP server responds, the following static IP configuration is used:

IP Address: 10.1.0.101

IP Mask: 255.0.0.0

Gateway: 10.1.0.1

In either case, dynamic or static, the interface IP address is associated with a unique NetBIOS name set by TDT.

NetBIOS Name

All BH32 devices will use this standard NetBIOS Name structure:

TDT_BHC_32_XXXX

XXXX = last 4 digits of the BH32 device serial number.

For Example:

A BH32 with a serial number of 1234 uses a NetBIOS name of: TDT_BHC_32_1234.

Although a default NetBIOS name is assigned, the name can be changed using the BH32 Web Interface. See below for more information.

Note: When connecting the BH32, be sure the network mask is set to a Class C or smaller network. A Class A network mask (255.0.0.0) will disable NetBIOS naming on the PC Ethernet interface. In such cases, the IP address of the BH32 must be used instead.

Configuration through the Web Interface

Every BH32 contains a minimal web server which is used for configuration and monitoring. Options can be set here if no DHCP server is available. If a DHCP server exists, the NetBIOS name associated with the dynamically assigned IP address can be configured using the BH32 server.

To connect to the BH32 server:

Make sure there is an active connection from the PC to the Ethernet port on the back of the BH32 then open an Internet browser such as Internet Explorer, Chrome or Firefox.

- Enter the device's IP address as the web address (e.g. http://10.1.0.100) and press **Enter**.

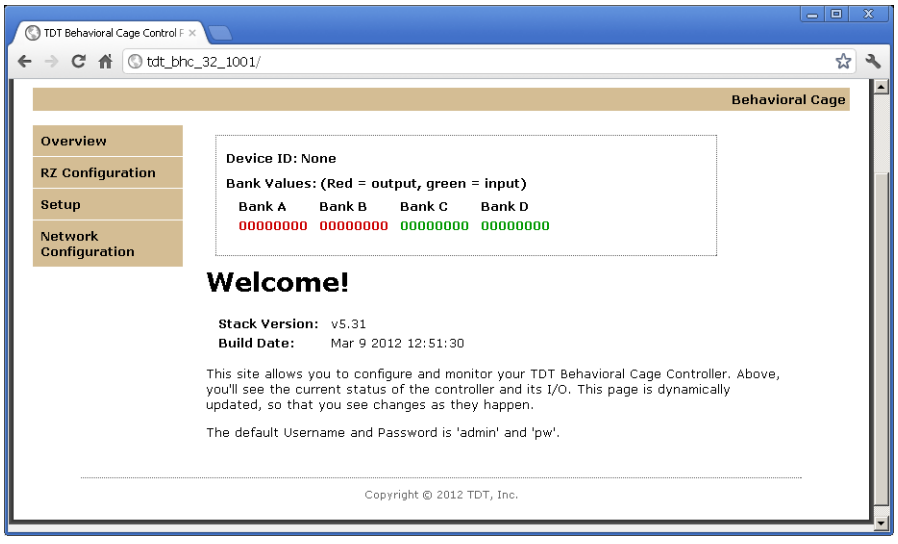
  or

- Enter the NetBIOS name as the web address (e.g. TDT_BHC_32_1001) and press **Enter**.

Once connected, navigation to the BH32 web interface loads the Welcome page. Clicking the links to the left of the web interface loads the corresponding page.

Welcome

The Welcome page provides basic information, allows real-time control of the BH32, and provides feedback on the status of each Bank.



Device Box

The status of individual bits is displayed for each bank. Clicking bits on an Output bank (red 0 or 1) will toggle that output bit and the corresponding LED on the front panel of the BH32. This can be used to manually control the output of the BH32 for testing a device connected to that output.

Firmware Version

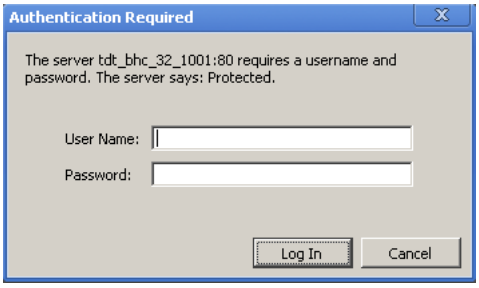
Stack Version and **Build Date** refer to the version of software running on the BH32.

Username and Password

Server pages that modify the device configuration, such as the Setup and Network Configuration pages, can only be accessed using a username and password. The default values are displayed in the Welcome message. This login information can be changed on the Network Configuration page.

To access a page that requires authentication:

1. Click the navigation link for the page.
2. When prompted, enter the username and password in the dialog box then click **Log In**.

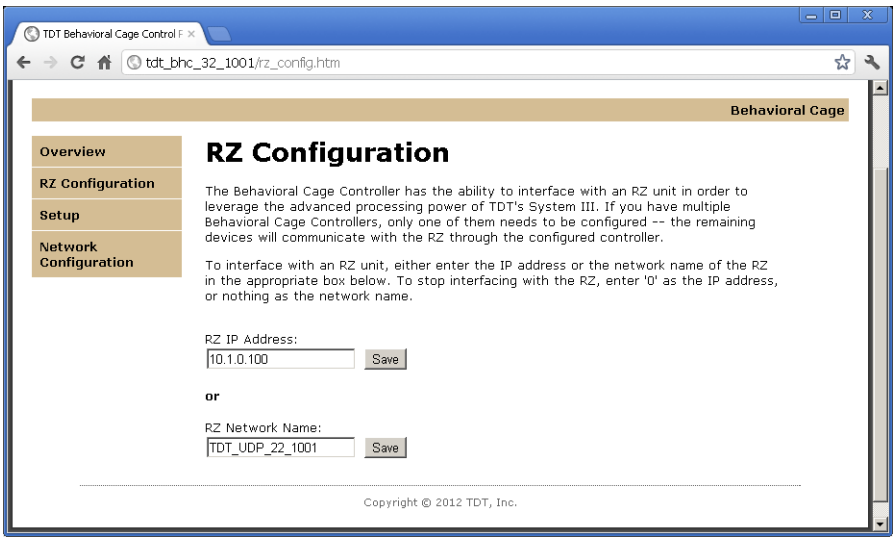


Default Username: **admin**

Default Password: **pw**

RZ Configuration

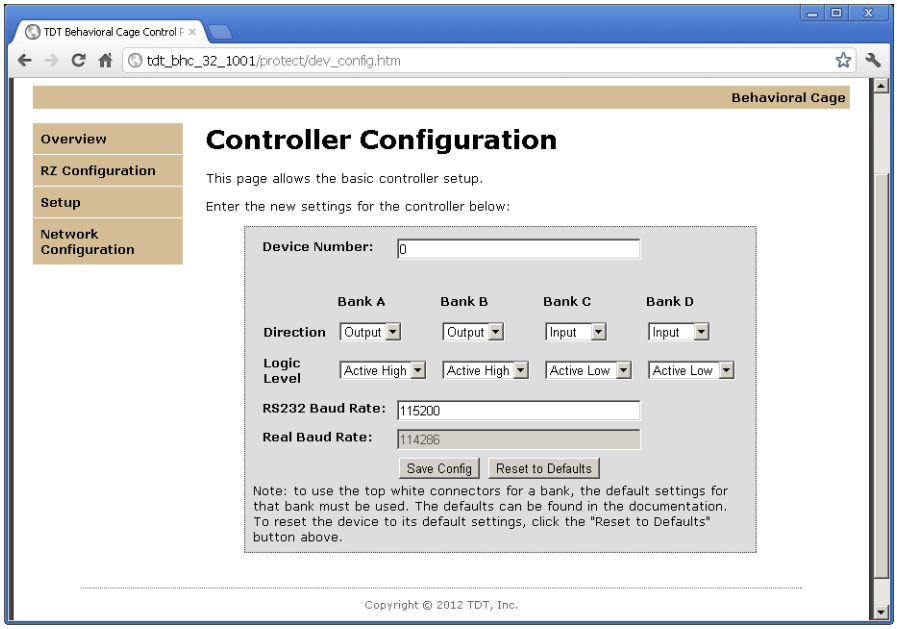
The BH32 can be paired with an RZ device that has a UDP interface. When any of the BH32's I/O bits changes state, a 32-bit integer (one bit per I/O) is sent via UDP packet to the RZ. Once this data is received on the RZ, it can be time stamped and/or processed to provide real-time feedback.



Controller Configuration

Note: This page may require authentication. See "Username and Password" above, for more information.

The Controller Configuration Page is used to configure properties of the BH32 hardware, including the Device Number, RS232 Baud Rate, and the behavior of individual banks when accessed via the DB25 connectors on the back panel.



Device Number

The Device Number is used to identify the BH32 among a network of BH32s. For single BH32 use, this value should be set to 1 or 0. If using the BH32 in Synapse, be sure to set your Synapse Rig BH32 device number to match.

Direction

Each Bank can be configured as either Input or Output. If using the BH32 in Synapse, please keep the direction of the banks at their default settings for compatibility.

Logic Level

Each Bank can be configured to Active High (1 = True) or Active Low (0 = True).

Baud Rate

The desired rate can be entered in the RS232 Baud Rate box. The actual realizable rate will be displayed in the Real Baud Rate box after the configuration has been updated.

Saving or Resetting the Configuration

Changes to the configuration are not implemented until they are saved and can be reset to the default settings at any time.

To make changes to the configuration:

- Type or select the desired values then click the **Save Config** button. The Save Config button saves the current configuration settings and performs a soft reset of the BH32 interface to load the settings.

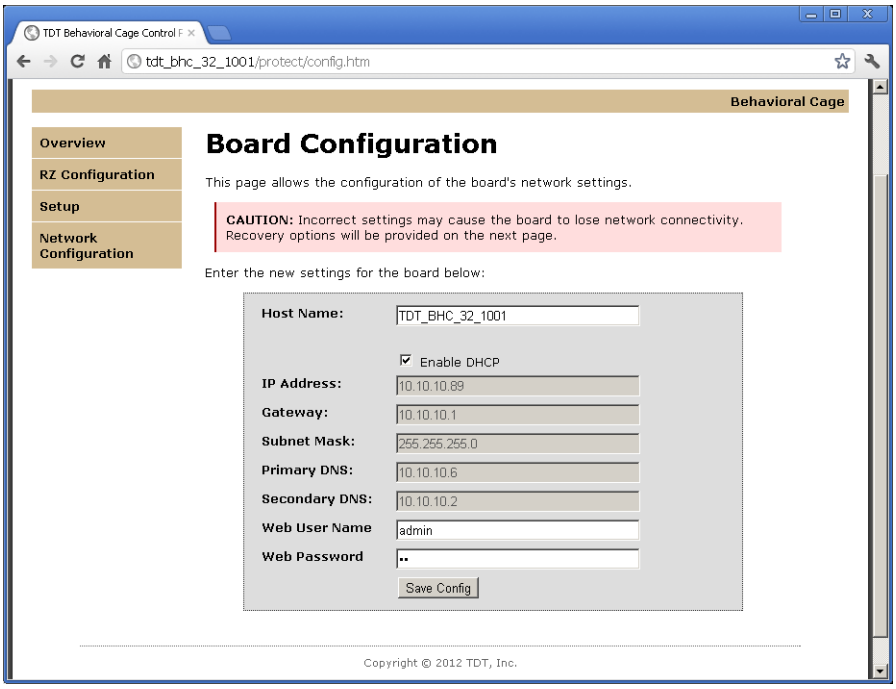
To restore the default values:

- Click the **Reset to Defaults** button.

Network Configuration Page

Note: This page may require authentication. See "Username and Password" on page 18-30, for more information.

The BH32's IP Address, host name and web username and password can be changed on this page.



If the Enable DHCP check box is checked, the **IP Address**, **Gateway Address**, **Subnet Mask**, and **DNS** server address values are overridden and automatically configured by the DHCP server if available.

Note: These settings are reserved for connections that cannot locate a DHCP server. If no DHCP server can be detected, contact your network administrator for applicable settings.

To change the username and password:

1. Enter the desired new username and password in the **Web User Name** and **Web Password** boxes.
2. Click the **Save Config** button.

   Note: Once changed, you may need to re-enter the new username and password to access pages that require authentication, such as the Network Configuration or Setup pages.

To Change the Host name (NetBIOS name):

- Type the desired host name in the **Host Name** box and click the **Save Config** button.

  Note: The Host name can be no greater than 15 characters long and cannot contain spaces or the following characters: \ / : * ? " ; | -

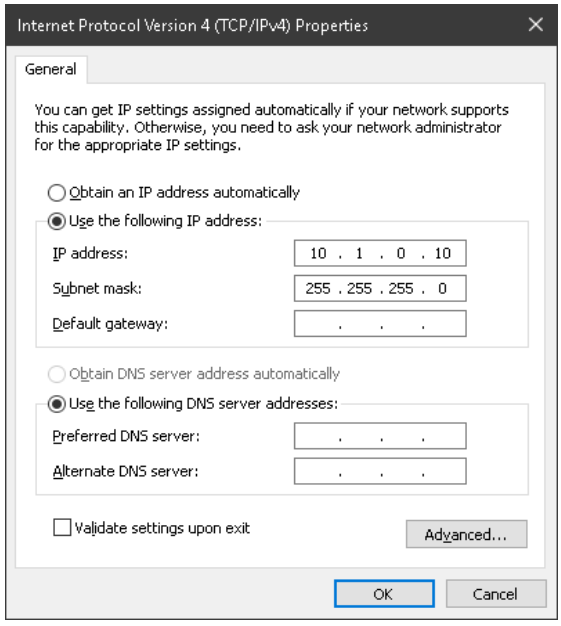
Direct Connection to a PC

The BH32 interface can be connected directly to a PC or laptop. Once connected, several steps are required for the PC to recognize the BH32 interface connection. This method may be performed on any operating system which supports TCP/IP.

To initialize the PC for a direct connection in Windows 7 or 10:

1. Physically connect the BH32 interface and the PC via an Ethernet crossover cable.
2. Open **Control Panel** then double-click **Network and Sharing Center**.
3. Click the desired connection link (this is usually a Local Area Connection).
4. In the status dialog, click the **Properties** button.
5. In the item list, select Internet Protocol (TCP/IP) or if there are multiples, select Internet Protocol (TCP/IPv4).
6. Click the **Properties** button.
7. Select **Use the following IP address** and enter these values:

   IP address: 10.1.0.x, where x can be any value, 1-254, except 100 or 101
   Subnet mask: 255.255.255.0
   Default gateway: Leave empty



8. Click **OK**.

The BH32 interface connection should now be recognized by the PC. Cycle power on the BH32 device, the IP address of the BH32 will be 10.1.0.101

BH32 Control

The BH32 can be controlled in the following ways:

1. Bi-directional real-time communication between the BH32 and an RZ processor UDP interface, running in Synapse.
2. Client software using the SynapseAPI to control the BH32 outputs in the above configuration.
3. Client software controlling the BH32 directly through the network port. The BH32 can optionally be on the same network as an RZ processor running in Synapse so state changes are captured and timestamped with the rest of the real-time data.

The BH32 Rig object in Synapse lets you configure how the BH32 outputs are controlled (either through real-time signals on the RZ itself or client-controlled via the Synapse API) and how to route BH32 input state changes for storage or further closed-loop processing.

Client libraries for the SynapseAPI with BH32 read/write examples can be found on the TDT website:

Matlab SDK

Python SDK

The Python SDK also includes an example of communicating with the BH32 directly from Python across the network.

Legacy BH32 RPvdsEx Circuit Design

If using the BH32 with an RZ device, Synapse provides the easiest paths to get synchronized behavioral data, but alternatives exist. OpenEx users will need to design an RPvdsEx circuit to communicate with the BH32. Synapse users can skip this section.

To communicate with an RZ device, the BH32 must first be paired with the RZ device. See “RZ Configuration” on page 18-30, for more information. Once paired, there are several circuit macros available to access the BH32 using the UDP interface on an RZ device. If using one, two, three or four BH32s on the network, use the RZ_BH_Send_1-4Ch and RZ_BH_Rec_1-4Ch macros. If using more than four BH32s, use the RZ_BH_Send_MC and RZ_BH_Rec_MC macros. All macros can be configured to specify the number of BH32s, which corresponds to the size of the underlying UDP packets.

RZ_BH_Send Macros

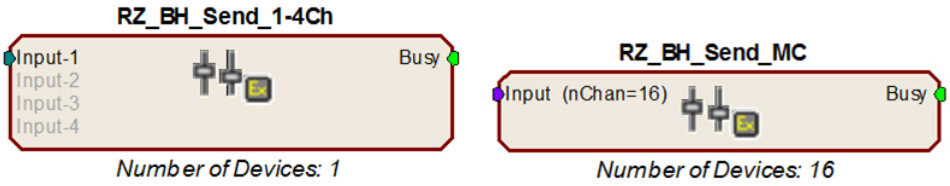
The RZ_BH_Send macros are used to send 32-bit words from the RZ over UDP to BH32 devices numbered from 1 to 4. The macro automatically sends a new packet if any of the Inputs change value. The 32-bit integer represents the current state of all I/O on the BH32 device. The ordering is as follows:

| Bit31 ..... Bit0 |

| A8 ... A1 | B8 ... B1 | C8 ... C1 | D8 ... D1 |

Example:

To change the state of D1 on BH32 Device Number 2, toggle the first bit of Input-2 of RZ_BH_Send_1-4Ch or channel two of RZ_BH_Send_MC’s Input.

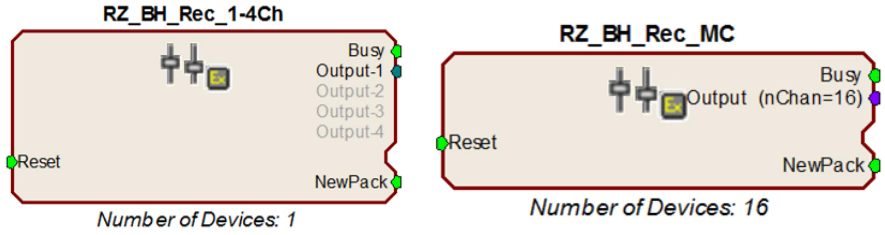


An output labeled "Busy" indicates if the macro is currently in the process of sending out a packet. The duration of the busy signal is dependent on the number of BH32 devices (it takes NumberOfDevices+2 samples to send a packet).

Note: Since the data packets are sent serially, it is recommended that the macro inputs are latched during transmission to ensure that the packet contains data from the same sample in time.

RZ_BH_Rec Macros

The RZ_BH_Rec macros are used to receive 32-bit words from networked BH32 devices through the RZ UDP port. The structure of each 32-bit word is described in the Packet Structure section below.



An incoming UDP packet is de-serialized and sent to the macro outputs. The "NewPack" output goes high (1) for one sample when a new packet header has been received. The "Busy" outputs are high (1) while the macro is de-serializing a packet. The length of this period depends on number of BH32 devices (it takes NumberOfDevices+1 sample to receive a packet). The macro outputs are latched until the next packet is received. The "Reset" input can be used to halt any data transfer and force the macro to wait for a new packet header.

Note: Since the channels are received serially, data in later channels occurred several samples before it is available on the macro Output.

The Packet Structure

This guide assumes the BH32 is communicating over UDP using the Ethernet port. BH32 devices listen on UDP port 22022 and all other UDP messages are disregarded. Communication over the RS232 serial port uses an identical packet structure and programming.

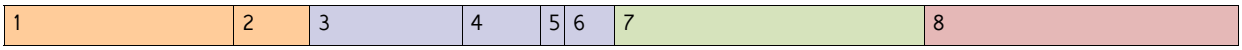
All data sent or received by the BH32 is in the form of a packet. Every packet has a standard structure which includes a header, target device and message.

The header consists of a 32-bit value; the first 24 bits are the protocol ID specific to the BH32/RZ interface and the next 8 bits are the protocol version (v1 as of this writing). This header is used by the BH32 and the RZ to identify packets that they should read and process.

The target device is identified with the next 24 bits of the packet. It consists of a 16-bit device number and an 8-bit group number in case you have more than 256 BH32 devices. This lets you target a single BH32 out of many on the network, or send batch commands to all BH32s on the network.

The message consists of a single toggle bit that identifies if the packet is to or from the device, a 7-bit message number (see "Messages" below) and a reserved 32-bit word for message parameters. Additional data can be appended to messages that require more than one parameter, such as the GET_SET_IO message that sets the output state or GET_SET_CONFIG that changes the device configuration.

The structure for the packet is shown below:



1. (24 bits) Unique protocol ID number – 0x55AB00.
2. (8 bits) Message protocol version number – this document covers protocol v. 1.
3. (16 bits) Device unit number. Devices will only process messages:
   a. Matching their unit number.
   b. With a unit number of -1.

- All devices numbered 0 are considered to be unnumbered.

4. (8 bits) Group – used in the GET_SET_IO message. Due to the maximum transmission unit constraints on most networks, each message can only contain ~256 data words. Offset provides a means of doing a bulk update in 256 device increments (e.g. update devices 256-511). This is typically set to 0.
5. (1 bit) Source – 1 means from device, 0 means device will process it.
6. (7 bit) Message number – See "Messages" below, for available commands.
7. (32 bits) Reserved word – See individual message details.
8. (0+ bits) Data word(s) – See individual message details.

Messages

Messages with a device number of -1 (0xFFFF) will be processed by all BH32s

| 0x55AB00 | 0x11 precedes all of the following messages.

"N/A" indicates that those bits are not included in the packet.

All of the GET_SET_XXXX messages are always considered a GET – i.e. devices will always reply to these messages with the corresponding information. If the message includes Data words, then the message will also be considered a SET,

updating the corresponding information on the device. In this case, the update happens before the GET so that the reply will show the updated information.

Name		Number		Description		
GET_VERSION		0		Retrieves BH32 firmware version number		
Message:	Device #	Group	0b0	0b0000000	N/A	N/A
Reply:	Device #	Group	0b1	0b0000000	0x00000000	Firmware version (32-bits)
SET_UNIT_NUM		1		Used for renumbering BH32s. Device number is set to 0, then BH32 enters PICK_UNIT_NUM mode. The starting device number is set to 1 (or the number sent in the data word). In PICK_UNIT_NUM mode, the BH32 display flashes a prompt for the user to press the input button to set the BH32 device number to the starting device number.		
Message:	Device #	Group	0b0	0b0000001	0x00000000	Starting Device # (optional)
Reply:	Device #	Group	0b1	0b0000001	N/A	N/A
PICK_UNIT_NUM		2		This message is broadcast by a device when it is in PICK_UNIT_NUM mode and the user presses the input button. After broadcasting this message, the device leaves PICK_UNIT_NUM mode and assumes the current starting device number as its own device number. If another devices is in PICK_UNIT_NUM mode, then its current starting device # is set to the number sent in the data word plus 1.		
Message:	0xFFFF	Group	0b1	0b0000010	0x00000000	Device # (32-bits)
Reply:	None					
GET_SET_IO		3		Sets or receives I/O state on one or multiple BH32s Each number in the Reply IP Address corresponds to a byte, so 10.10.10.100 ➔ 0x0A0A0A64. A Reply Address of 0x00000000 means reply to sender. A Reply Address of 0xFFFFFFFF means broadcast to all. If Device # is 0xFFFF and two 32-bit words are in the message, the first 32 bits are used by Device #0 and the rest by Device #1. The format of each 32-bit data word is as follows: | A8-A1 | B8-B1 | C8-C1 | D8-D1 | Attempting to set a pin on an input bank is ignored.		
Message:	Device #	Group	0b0	0b0000011	Reply IP Address	Desired I/O state (32-bit words, optional)
Reply:	Device #	Group	0b1	0b0000011	Reply IP Address	I/O state (32-bits)
GET_SET_CONFIG		4		Used to set various device parameters. Can directly set Device number, RS232 baud rate, and the I/O configuration. Parameters are 16 bit values, but only one is sent per 32-bit data word. A parameter number of 0 will return all configuration parameters. Parameter number 1 =: get/set device number 2-3 =: set RS232 baud rate 4-5 =: read actual baud rate 6 =: read bank-wide settings 0b0101		
Message:	Device #	Group	0b0	0b0000100	Param #	Param mask(s)/val(s) (optional)
Reply:	Device #	Group	0b1	0b0000100	Param #	Param val(s)

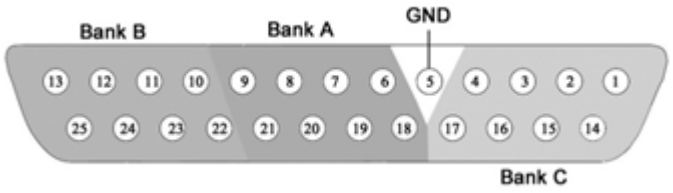
Name		Number		Description		
GET_SET_TIMESTAMP		5		Used to set/read the device's internal clock. If a data word is sent, the clock is set to the value in the data words, interpreted as a single 64-bit value in microseconds.		
Message:	Device #	Group	0b0	0b0000101	0x00000000	64-bit timestamp (optional)
Reply:	Device #	Group	0b1	0b0000101	0x00000000	64-bit timestamp
GET_SET_TRACK		6		Sets which individual pins are in TRACK mode, meaning a 64-bit timestamp is recorded every time the pins value changes. The BH32 will reply with all recorded timestamps (if any) for that pin and flush the timestamp memory for that pin. Up to 256 timestamps total for all pins can be stored in memory.		
Message:	Device #	Group	0b0	0b0000110	Pin Number	Active? (0 or 1, 32-bits)
Reply:	Device #	Group	0b1	0b0000110	Pin Number	64-bit timestamp(s)
GET_SET_NETCONFIG		7		Currently for internal TDT use only.		
GET_SET_SERIAL		8		Currently for internal TDT use only.		
GET_SET_POLL		9		When period is non-zero, the BH32 will send a POLL_EVENT message to Reply IP Address at the specified period. Set period to 0 to stop sending POLL_EVENT messages.		
Message:	Device #	Group	0b0	0b0001001	Reply IP Address	32-bit period, in ms (optional)
Reply:	Device #	Group	0b1	0b0001001	Reply IP Address	32-bit period, in ms
POLL_EVENT		10		See GET_SET_POLL for information about configuring a device to send this message.		
Message:	Device #	Group	0b1	0b0001010	32-bit period, in ms	I/O state (32-bits)
Reply:	None					
GET_SET_TRIGGER		11		When the Trigger Mask is non-zero, the device will enter TRIGGER state. A TRIGGER_EVENT message is sent whenever a pin indicated in the Trigger Mask changes value.		
Message:	Device #	Group	0b0	0b0001011	Reply IP Address	Trigger Mask (optional)
Reply:	Device #	Group	0b1	0b0001011	Reply IP Address	Trigger Mask
TRIGGER_EVENT		12		See GET_SET_TRIGGER for information about configuring the BH32 to send this message.		
Message:	Device #	Group	0b1	0b0001010	Trigger Mask	I/O state (32-bits)
Reply:	None					

Name		Number		Description		
GET_SET_RZ_IP		13		If the RZ IP Address is non-zero, the BH32 will enter RZ_CONTROLLER state. In this state, the BH32 will: Multicast a GET_SET_TRIGGER message on the network to every BH32 device in its same group, with its own IP Address as the reply address and 0xFFFFFFFF as the Trigger Mask Send a SET_REMOTE_IP packet to the RZ IP Address Enter a special TRIGGER state While in this mode, the device will respond to BH32 and RZ type packets. Whenever a GET_SET_IO, POLL_EVENT or TRIGGER_EVENT message is received, the BH32 will save the I/O state from the packet in an RZ message buffer. Every 1ms, the BH32 will check if new data has been received and transmit new data to the RZ as a DATA packet. Whenever a DATA packet is received from the RZ IP Address, the BH32 creates a GET_SET_IO message and multicasts it to the local network to its same group. If the RZ IP Address is set to 0, the BH32 will no longer be in RZ_CONTROLLER state and broadcast a GET_SET_TRIGGER message on the network with Trigger Mask 0.	
Message:	Device #	Group	0b0	0b0001101	0x00000000	RZ IP Address (optional)
Reply:	Device #	Group	0b1	0b0001101	0x00000000	RZ IP Address
GET_SET_RZ_NBNAME		14		Same as GET_SET_RZ_IP, but uses RZ's NetBIOS name as input (e.g. 'TDT_UDP_D3_2012'. If the name starts with a null character, the BH32 leaves RZ_CONTROLLER state.		
Message:	Device #	Group	0b0	0b0001110	0x00000000	Null-terminated string (up to 16 characters, optional)
Reply:	Device #	Group	0b1	0b0001110	0x00000000	Null-terminated string (up to 16 characters)
RESET_TO_DEFAULTS		126		Clears the target IP and port, thereby stopping the flow of packets.		
Message:	Device #	Group	0b0	0b1111110	N/A	N/A
Reply:	Device #	Group	0b1	0b1111110	N/A	N/A
RESET		127		Performs a software reset of the BH32		
Message:	Device #	Group	0b0	0b1111111	N/A	N/A

BH32 Technical Specifications

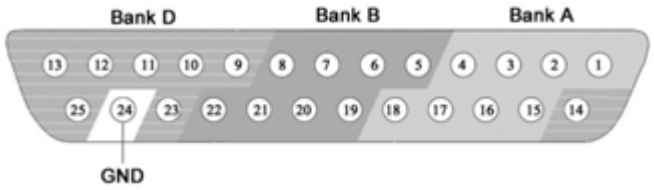
Power Input	Input for 6-9V, 3A center-negative adapter input.	
Timing Specs	Note that these timings depend on network latency.	
	UDP input to BH32 output	1 ms average
	UDP input to BH32 UDP response	4 ms average
	Digital Input to BH32 UDP response	<2 ms average

DB25 Digital IO Pinout



Pin	Name	Description		Pin	Name	Description
1	C1	Bank C Bits 1, 3, 5, and 7		14	C2	Bank C Bits 2, 4, 6, and 8
2	C3			15	C4	
3	C5			16	C6	
4	C7			17	C8	
5	GND	Digital I/O Ground		18	A1	Bank A Bits 1, 3, 5, and 7
6	A2	Bank A Bits 2, 4, 6, and 8		19	A3	
7	A4			20	A5	
8	A6			21	A7	
9	A8			22	B1	Bank B Bits 1, 3, 5, and 7
10	B2	Bank B Bits 2, 4, 6, and 8		23	B3	
11	B4			24	B5	
12	B6			25	B7	
13	B8					

DB25 Digital IO-2 Pinout



Pin	Name	Description		Pin	Name	Description
1	A1	Bank A Bits 1, 3, 5, and 7		14	D7	Bank D Bit 7
2	A3			15	A2	Bank A Bits 2, 4, 6, and 8
3	A5			16	A4	
4	A7			17	A6	
5	B1	Bank B Bits 1, 3, 5, and 7		18	A8	
6	B3			19	B2	Bank B Bits 2, 4, 6, and 8
7	B5			20	B4	
8	B7			21	B6	
9	D1	Bank D Bits 1, 2, 3, 4, and 6		22	B8	
10	D2			23	D8	Bank D Bit 8
11	D3			24	GND	Ground
12	D4			25	D5	Bank D Bit 5
13	D6					

Molex Pin and Socket Connectors

EXTERNAL POWER

V+ Positive Voltage

NC No Connection

G Ground

1.57mm Diameter Standard Molex Pin and Socket connectors on top panel.

Important! The external power connectors are shorted together; do not connect a second external power source.

I/O CONNECTORS

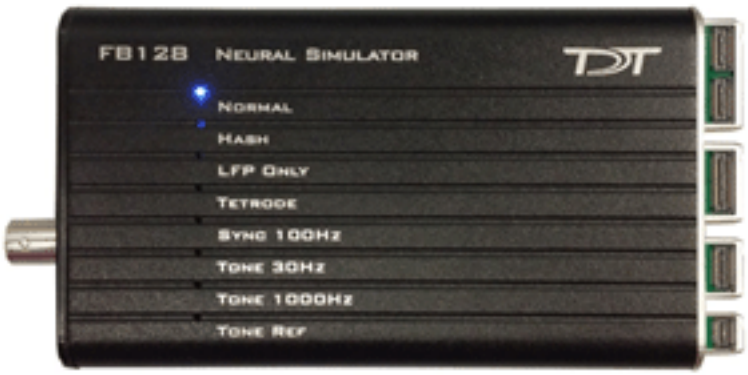
V+ Positive Voltage

S Signal

G Ground

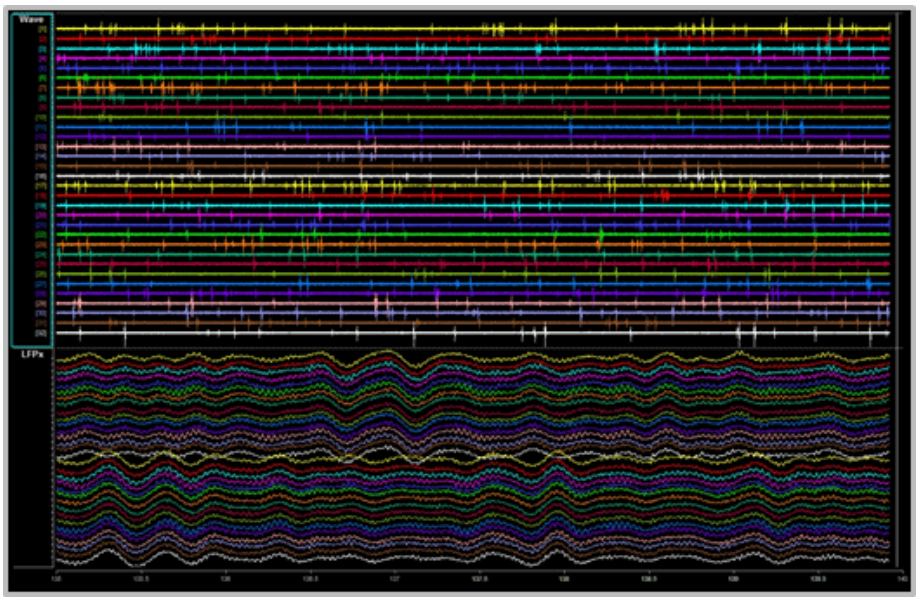
Part 19: Signal Handling

FB128 Neural Simulator



Overview

The FB128 Neural Simulator is a tool for testing experimental paradigms during the design phase and debugging problems when they arise. The compact, battery operated device simulates neurological waveforms or sine waves that can be output directly to a ZIF-Clip® headstage. Neurological simulations consist of an LFP component and spike components. Eight unique spike waveform shapes are used depending on the mode. Up to 128 channels can be output (up to 96 unique).



32 channels from FB128 – filtered for Spike (top) and LFP (bottom) waveforms

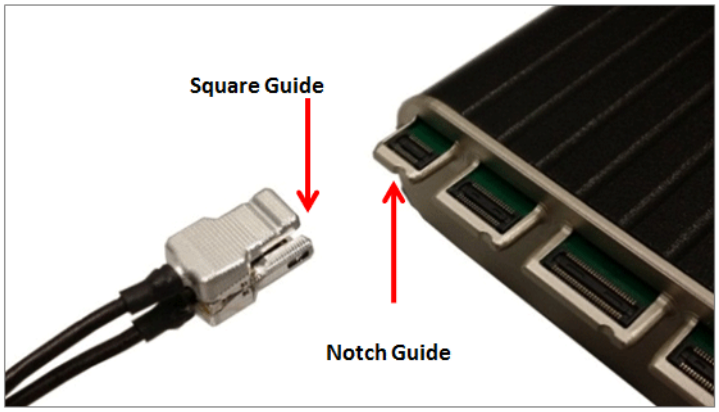
The simulator can operate in eight different modes and includes an inhibitory/ excitatory option for even more output variations. The simulation modes are listed on the face of the module and LEDs indicate which is active. Operational buttons or switches, a TTL input, and a charger input are positioned on one end of the module and output connectors for headstage connection are positioned on the other.

Hardware Set-up

When using the FB128 to test your protocol or recording hardware, set-up the recording part of your system as you would during your experiment with the FB128 in place of the subject and electrodes.

Four output connectors are positioned side-by-side at one end of the simulator. One for each size of ZIF-Clip® headstages, including one connector for the ZC16 and ZC32 and one each for the ZC64, ZC96, and ZC128.

Connect the headstage to the appropriate connector just as you would connect it to an electrode or adapter. First, line up the square guide on the headstage with the notch on the probe connector. Hold it firmly open at the wire end of the connector until it is fully in position then clamp it firmly in place.

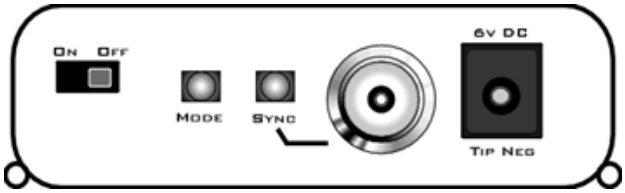


ZC32 and FB128

⚠ CAUTION! Failure to hold the clip open until it is fully in position can cause damage to the headstage connectors.

Simulation Modes

The Mode button, is positioned on the end opposite the output connectors.



To cycle through the operating modes:

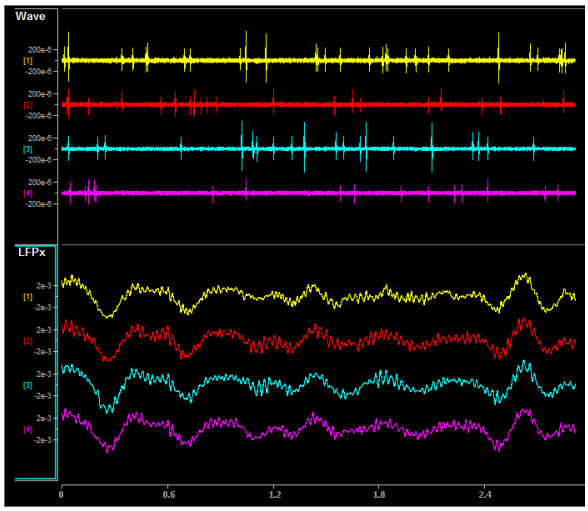
- Briefly press the **Mode** button. The active mode is indicated by a lit LED on the face of the module. If you press too long and the LED is blinking, you are in Channel Mapping Mode. See "Channel Mapping Mode" on page 19-8.

Modes of Operation

NORMAL Neurological waveforms, including spike waveforms and LFP.

Wave

LPx



Pictured waveforms were generated by the FB128 and plotted in Synapse with the following settings:

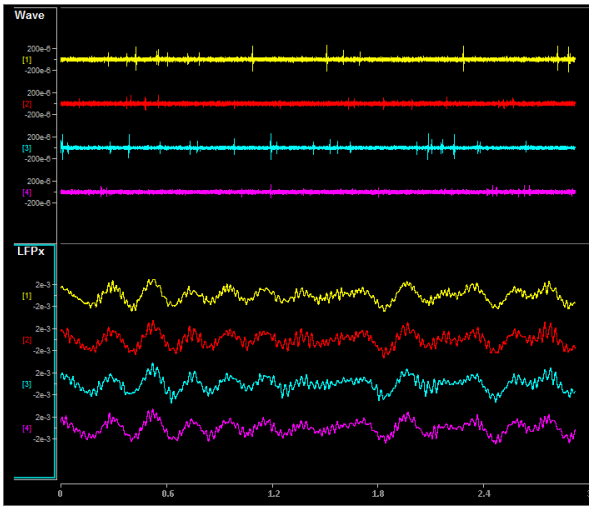
Wave Filter Settings: High Pass: 300 Hz, Low Pass: 5000 Hz

LFPx Filter Settings: High Pass: 0 Hz, Low Pass: 300 Hz

HASH NORMAL mode but with spikes scaled down by a factor of 2.

Wave

LPx



Pictured waveforms were generated by the FB128 and plotted in Synapse with the following settings:

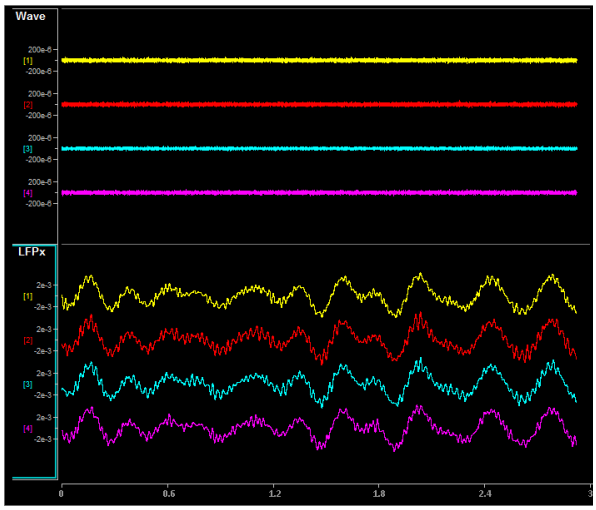
Wave Filter Settings: High Pass: 300 Hz, Low Pass: 5000 Hz

LFPx Filter Settings: High Pass: 0 Hz, Low Pass: 300 Hz

LFP ONLY NORMAL with spikes scaled to zero.

Wave

LPx



Pictured waveforms were generated by the FB128 and plotted in Synapse with the following settings:

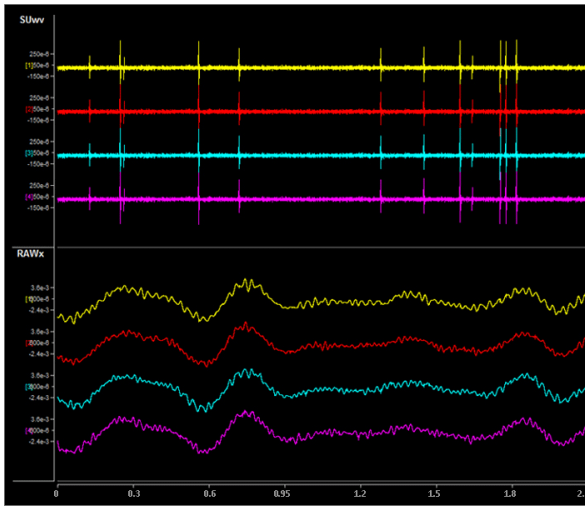
Wave Filter Settings: High Pass: 300 Hz, Low Pass: 5000 Hz

LFPx Filter Settings: High Pass: 0 Hz, Low Pass: 300 Hz

TETRODE Neurological LFP waveforms with spikes—where spikes on each group of four channels fire synchronously. Channels 1-4 fire together, channels 5-8 fire together, and so forth.

SUwv

RAWx



Shown: Tetrode + Excitatory Mode

Pictured waveforms were generated by the FB128 and plotted in Synapse with the following settings:

SUwv Filter Settings: High Pass: 300 Hz, Low Pass: 5000 Hz

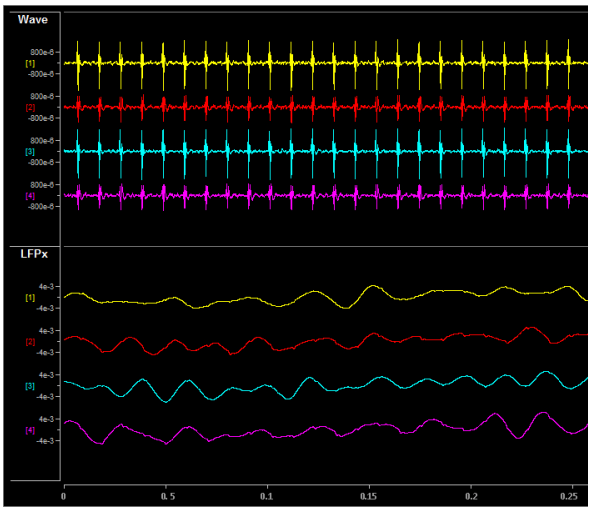
RAWx Filter Settings: Unfiltered

Note: To better view Tetrode mode (as pictured above) the channels must be re-mapped. The map for each ZIF-Clip® headstage is included in FB128Tetrode.rcx, which is bundled in the RPvdsEx zipped examples on the TDT Website at: https://www.tdt.com/files/examples/RPvdsExExamples.zip.

SYNC 100 Hz Neurological LFP waveforms with spikes on all channels firing synchronously at 100 Hz fixed rate. The spikes in this mode are always the same shape.

Wave

LFPx



Pictured waveforms were generated by the FB128 and plotted in Synapse with the following settings:

Wave Filter Settings: High Pass: 300 Hz, Low Pass: 5000 Hz

LFPx Filter Settings: High Pass: 0 Hz, Low Pass: 300 Hz

TONE 30 Hz 30 Hz sine wave at ~700 µV on all channels.

TONE 1000 Hz 1000 Hz sine wave at ~70 µV on all channels (actual frequency is ~763 Hz).

TONE REF 100 Hz sine wave at ~700 µV on Reference channel only. All other channels set 0.

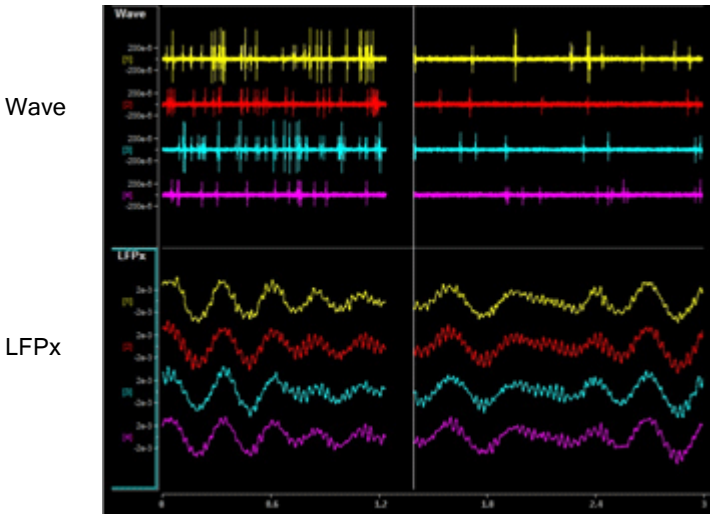
Because the reference is subtracted from all channels, the sine wave should be visible on all channels.

Note: Reference lines connected to Ground (0 V) for all modes except TONE REF.

Inhibitory/Excitatory Mode

An inhibitory/excitatory mode can be used in conjunction with all spike modes (NORMAL, HASH, TETRODE, and SYNC 100 Hz). When enabled, the base neurological waveforms (LFP) remain the same but some spike shapes are inhibited (fire less often) while others are excited (fire more often).

The Inhibitory/Excitatory mode can be activated by holding down the Sync button or it can be controlled programmatically by sending a TTL high to the Sync BNC connector. When using the Sync input, the mode change can also be timestamped in Synapse, which is helpful when testing event-related spike changes and verifying that histogram plots are working correctly.



Normal + Excitatory Mode **Normal Mode**

Pictured waveforms were generated by the FB128 and plotted in Synapse with the following settings:

Wave Filter Settings: High Pass: 300 Hz, Low Pass: 5000 Hz

LFPx Filter Settings: High Pass: 0 Hz, Low Pass: 300 Hz

Channel Mapping Mode

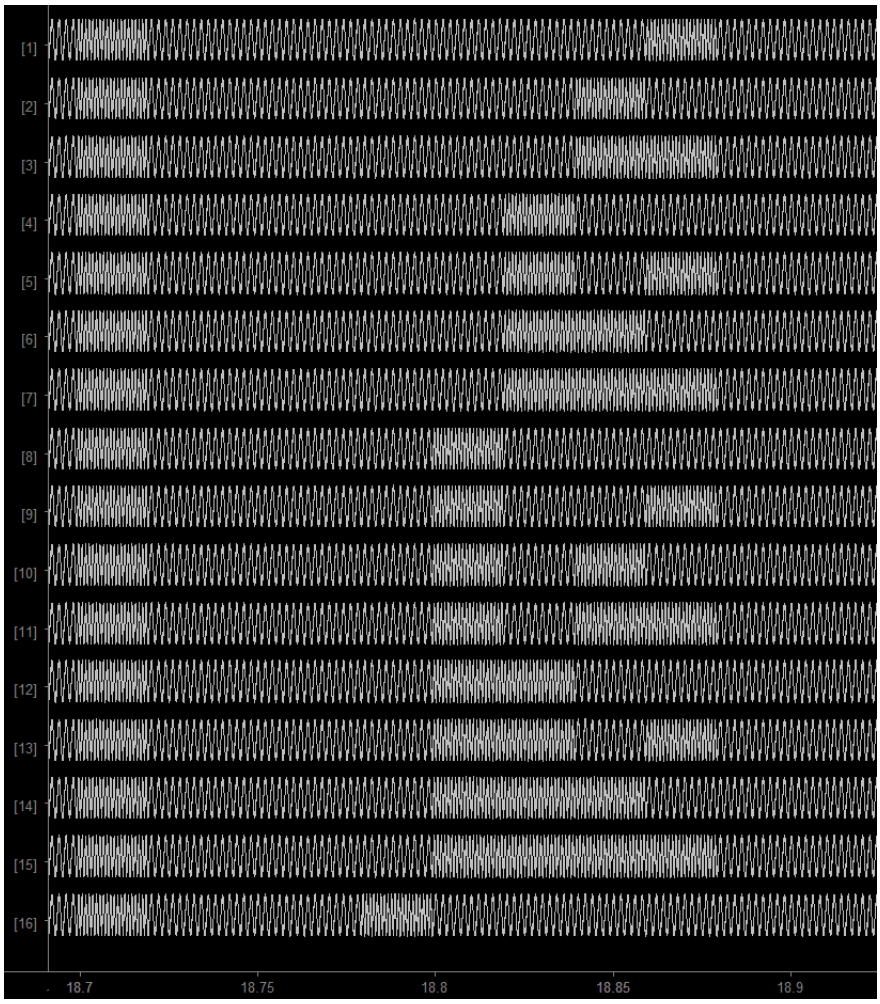
Starting with serial number 2000, the FB128 includes a diagnostic mode that presents a unique waveform on every channel. This is useful for mapping channels or for detecting shorts on the headstage.

Press and hold the MODE button on the FB128 until the LED starts flashing, which indicates the FB128 is in channel mapping mode. Each channel plays a frequency encoded waveform that creates a unique binary pattern that can be mapped to channel number. See the image below.

Briefly press the MODE button again to cycle through the available channel count options until it matches the headstage you are testing.

Flashing LED	Channel Map Mode
NORMAL	16-32 Channels
HASH	64 Channels
LFP ONLY	96 Channels
TETRODE	Lower 64 Channels of 128 Channel connector
SYNC 100Hz	Lower 64 Channels of 128 Channel connector

Power cycle the FB128 to exit Channel Mapping Mode.



FB128 Channel Mapping Mode Output

Power

The FB128 is powered by a 1950 mAh battery with a 10-hr life. A 6 Volt charger (tip negative) is supplied for charging.

Technical Specifications

Technical Specifications for the FB128 Neural Simulator.

Output	± 10 mV
Battery	1950 mAh
Battery life	10 hour life between charges, time to charge 2.5 hours
Charger	6 V (tip negative)

PP24 Patch Panel

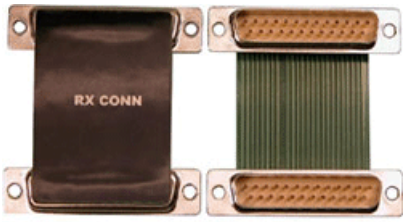
Overview

The PP24 Patch Panel provides front panel, BNC connections for easy access to the digital and analog inputs and outputs of the RX and RZ processors.

Note: The PP16 Patch Panel is recommended for use with devices such as the If using the RP2.1 or RA16BA processors, Power Multiplexer （PM2R）, or Power Amplifier （SA8）.

The PCB Adapter Advantage

The PP24 is supplied with a either an RX or RZ PCB adaptor that can be used with the corresponding processor type. The PCB provides better performance than ribbon cables, facilitating faster data transfer rates and improved signal to noise ratios.



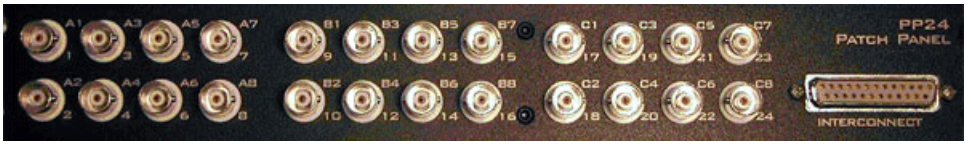
Adjustable Positioning

The PP24 is equipped with a 25-pin connector on the front panel. The PCB Adapter can be used to connect the PP24 to an RX device positioned either directly above or directly below the PP24 or an RZ processor positioned above the PP24. Four thumbscrews located on each corner of the PP24 front panel allow the user to slide the BNC array into the correct position to align the connector with the target device.

⚠ CAUTION: The thumbscrews should never be completely removed. Avoid loosening the thumbscrews too far.

Mapping the Inputs and Outputs for Each Device

The PP24 consists of 3 banks of BNC connectors, Bank A, B, and C. Each of the banks is labeled 1-8 within the set and each BNC is also numbered as part of the entire group from 1 – 24.



The following table shows the configuration of the BNC connectors for each I/O connector of the RX and RZ devices.

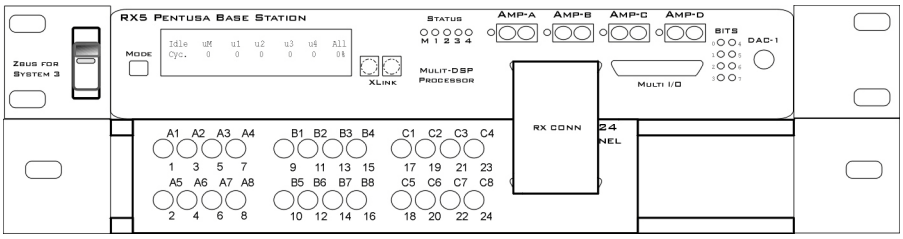
Device & Connector	A1-A8	B1-B8	C1-C8
RX5, RX6, RX7, RX8 Digital I/O Connector	Bit Addressable Digital I/O Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 8-15
RX5, RX7 Multi I/O Connector	Analog Outputs A2, A4, A6, A8 = Channels 1-4 A1, A3, A5, A7 = Not Used	Digital I/O, Byte C Channels 16-23	Digital I/O, Byte D Channels 24-31
RX8 Analog I/O Connector	Analog I/O Block A Channels 1-8	Analog I/O Block B Channels 9-16	Analog Output Block C Channels 17-24
RZ2 Digital I/O Connector	Bit Addressable Digital I/O, Port C Channels 0-7	Digital I/O, Port A Channels 0-7	Digital I/O, Port B Channels 0-7
RZ2 Analog I/O Connector	Not Used	Analog Inputs Channels 1-8	Analog Outputs Channels 9-16
RZ5, RZ5D, RZ6 Digital I/O Connector	Bit Addressable Digital I/O, Byte C Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 0-7
RZ5, RZ5D Analog I/O Connector	Not Used	Analog Inputs Channels 1-4	Analog Outputs Channels 9-12

For more information, see the diagrams for the desired device below. Note that the RX5 and RX7 use the same Digital and Multi I/O mappings.

Mapping RX5 or RX7 I/O

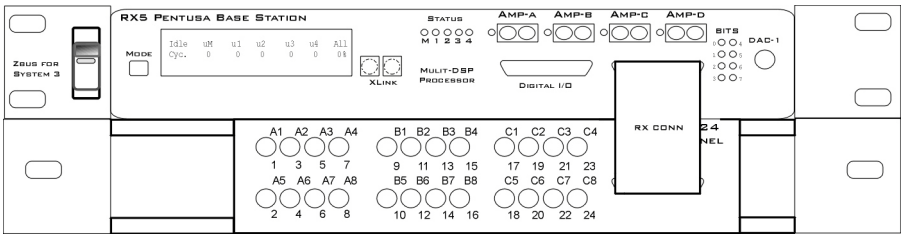
Note: The PP24 can be mounted above or below the RX5.

The diagram below maps the RX5 or RX7 **Digital I/O** connections to the PP24.



A1-A8	B1-B8	C1-C8
Bit Addressable Digital I/O Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 8-15

The diagram below maps the RX5 or RX7 **Multi I/O** connections to the PP24.

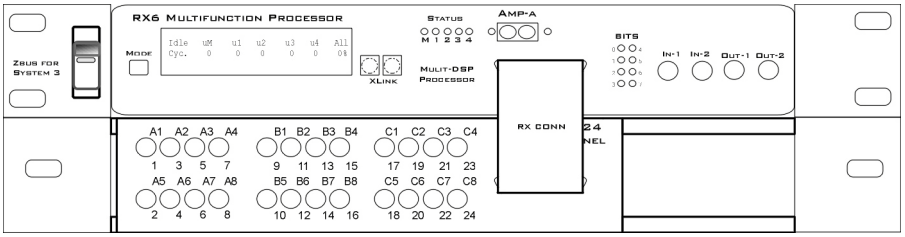


A1-A8	B1-B8	C1-C8
Analog Outputs A2, A4, A6, A8 = Channels 1-4 A1, A3, A5, A7 = Not Used	Digital I/O, Byte C Channels 16-23	Digital I/O, Byte D Channels 24-31

Mapping RX6 I/O

Note: The PP24 can be mounted above or below the RX6.

The diagram below maps the RX6 **Digital I/O** connection to the PP24.

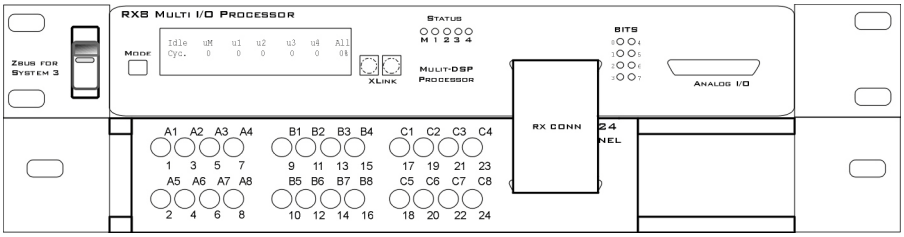


A1-A8	B1-B8	C1-C8
Bit Addressable Digital I/O Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 8-15

Mapping RX8 I/O

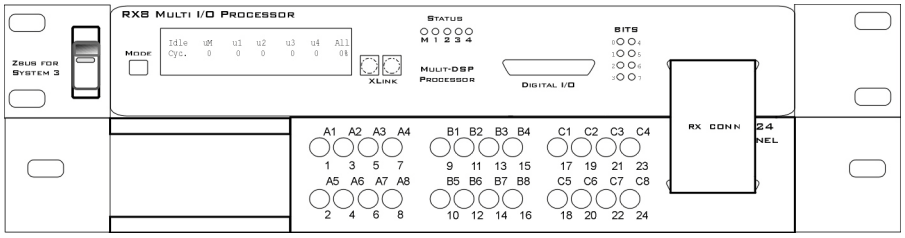
Note: The PP24 can be mounted above or below the RX8.

The diagram below maps the RX8 **Digital I/O** connection to the PP24.



A1-A8	B1-B8	C1-C8
Bit Addressable Digital I/O Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 8-15

The diagram below maps the RX8 **Analog I/O** connection to the PP24.

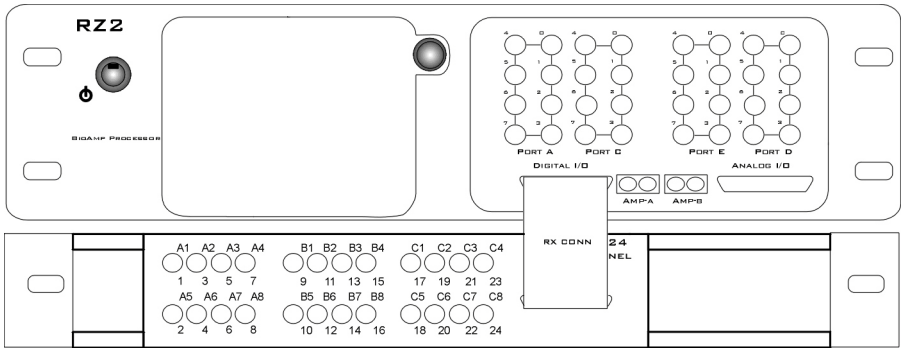


A1-A8	B1-B8	C1-C8
Analog I/O Block A Channels 1-8	Analog I/O Block B Channels 9-16	Analog Output Block C Channels 17-24

Mapping RZ2 I/O

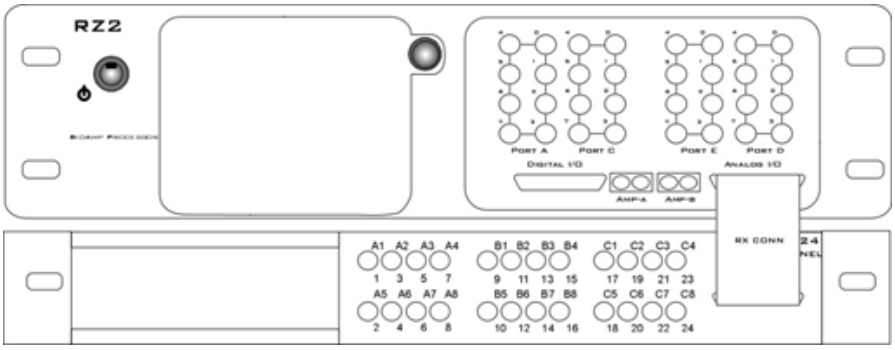
Note: The PP24 is mounted below the RZ2.

The diagram below maps the RZ2 **Digital I/O** connection to the PP24.



A1-A8	B1-B8	C1-C8
Bit Addressable Digital I/O Channels 0-7	Digital I/O, Port A Channels 0-7	Digital I/O, Port B Channels 0-7

The diagram below maps the RZ2 **Analog I/O** connection to the PP24.

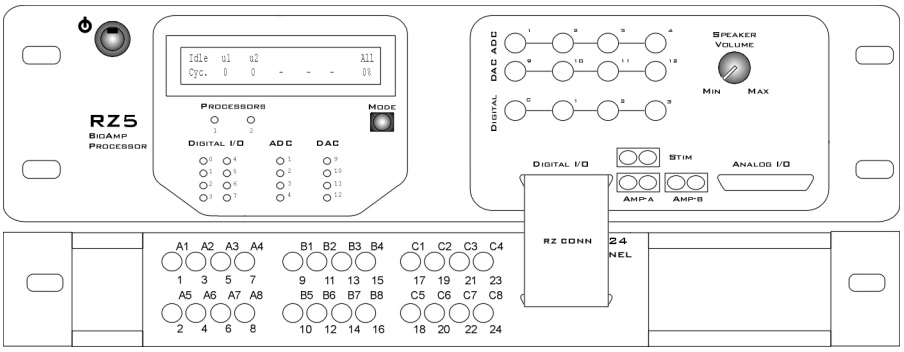


A1-A8	B1-B8	C1-C8
Not Used	**Analog Input, Port D Channels 1-8**	**Analog Output, Port E Channels 9-16**

Mapping RZ5, RZ5D I/O

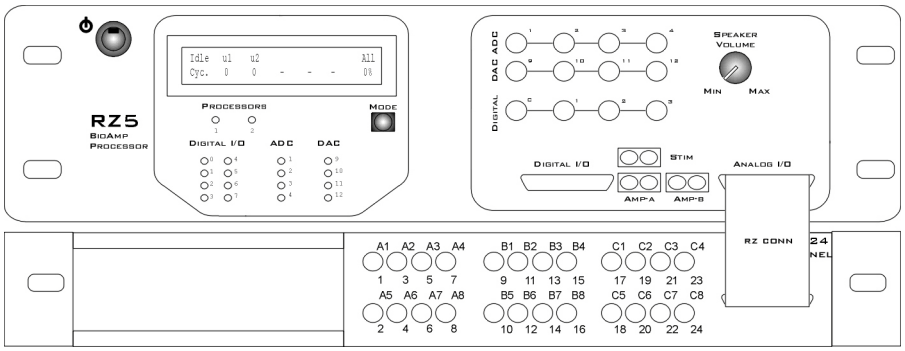
Note: The PP24 is mounted below the RZ5.

The diagram below maps the RZ5 or RZ5D **Digital I/O** connection to the PP24.



A1-A8	B1-B8	C1-C8
Bit Addressable Digital I/O Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 0-7

The diagram below maps the RZ5 or RZ5D **Analog I/O** connection to the PP24.

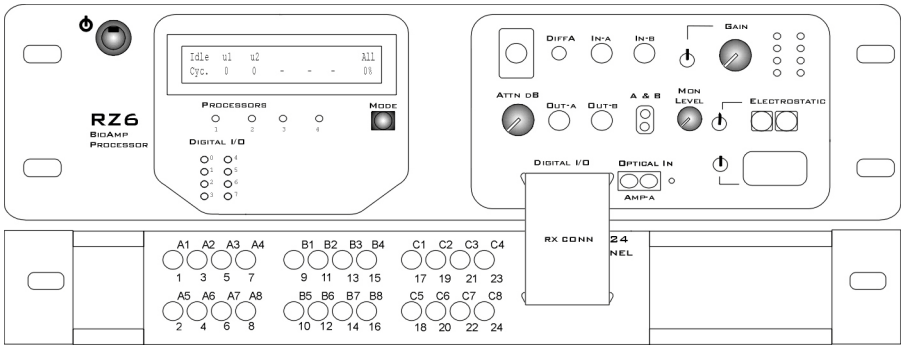


A1-A8, B5-B8, C5-C8	B1-B4	C1-C4
Not Used	Analog Input Channels 1-4	Analog Output Channels 9-12

Mapping RZ6 I/O

Note: The PP24 is mounted below the RZ6.

The diagram below maps the RZ6 **Digital I/O** connection to the PP24.



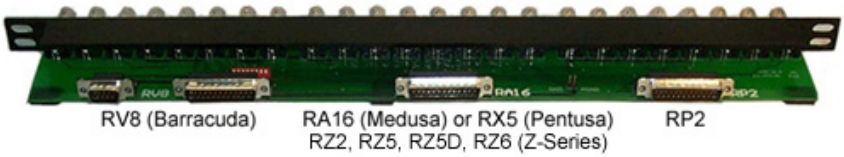
A1-A8	B1-B8	C1-C8
Bit Addressable Digital I/O Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 0-7

PP16 Patch Panel

The PP16 Patch Panel provides convenient BNC connections for easy access to the digital and analog inputs and outputs of a variety of System 3 devices. Originally designed for use with the RP2 Real-time Processor, RA16 Medusa Base Station, and RV8 Barracuda; the PP16 back edge is equipped with a nine pin and three 25-pin connectors, which have been marked with the corresponding device label to minimize the possibility of miswiring.

To connect the PP16 to a device:

Connect the male end of the 9- or 25-pin ribbon cable to the desired module and connect the female end to the correct PP16 input according to the following table.



PP16 Device Connectors

Connector:	RV8 9-Pin	RV8 25-Pin	RA16 25 Pin		RP2 25 Pin
Devices:	RV8 Optional I/O*	RV8 Digital I/O	RA16BA RA8GA SA8 RX5 RX6 RX7 RX8	RZ2 RZ6 RZ5	RP2 RP2.1 PM2R

*GND Jumper: When using the PP16 and the RV8 Barracuda, the jumper located on the PP16 connects the analog ground of the DB9 connector to the device ground on the RV8.

*DIP-Switch: The DIP-switches located on the PP16 is used to control the input of either digital signals or the output of analog signals on the RV8. When the DIP switches are in the ON position, digital input bits 8-15 are connected and will be available on the PP16 BNCs A1-A8. Do not attempt to output any analog signals from the RV8 while the DIP-switches are in the ON position. When the DIP-switches are in the OFF position the analog ouputs are available on the PP16 BNCs A1-A8.

Mapping the Inputs and Outputs for Each Device

Each device has a unique input and output configuration. The table below shows the configuration of the BNC connectors.

Device & Connector	A1-A8	B1-B8	C1-C8
RP2, RP2.1 Digital I/O Connector	Digital Inputs Channels 1-8	Digital Outputs Channels 1-8	C1=Trigger C2=Volt out (3.3v)
RA16BA Analog/Digital I/O Connector	Analog Outputs Channels 1-8	Digital Outputs Channels 0-7	Digital Outputs Channels 8-15
RV8, RV8D Digital I/O Connector	Digital Inputs Channels 8-15	Digital Outputs Channels 0-7	Digital Inputs Channels 0-7
RV8D* Optional I/O Connector	Analog Outputs Channels 1-8	Not Used	Not Used
RA8GA Analog I/O Connector	Analog Input Channels 1-8	Not Used	Not Used
PM2R Signal Out Connector	Analog Output Channels 0-7	Analog Output Channels 8-15	Not Used
SA8 Power Outputs Connector	Analog Output Channels 1-8	Analog Output Signal and Ground: Channels 1-4	Analog Output Signal and Ground: Channels 5-8

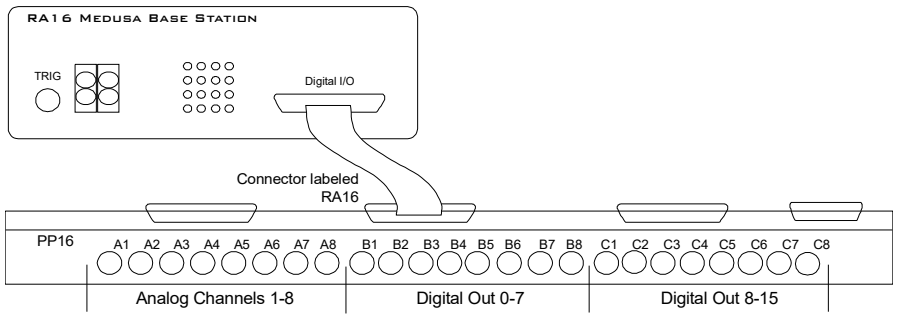
*To use the RV8D Optional I/O analog output connector, move all the DIP switch positions to the OFF setting on the PP16. Once the switches are in this position digital inputs 8-15 are not accessible. Do NOT attempt to output analog signals when the switches are in the ON position.

The PP16 can also be used with the RX and RZ devices, however, the PP24 is recommended.

Device & Connector	A1-A8	B1-B8	C1-C8
RX5, RX6, RX7, RX8 Digital I/O Connector	Bit Addressable Digital I/O Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O, Byte B Channels 8-15
RX5, RX7 Multi I/O Connector	Analog Outputs A2, A4, A6, A8 = Channels 1-4 A1, A3, A5, A7 = Not Used	Digital I/O, Byte C Channels 16-23	Digital I/O, Byte D Channels 24-31
RX8 Analog I/O Connector	Analog I/O Block A Channels 1-8	Analog I/O Block B Channels 9-16	Analog Output Block C Channels 17-24
RZ2 Digital I/O Connector	Bit Addressable Digital I/O, Port C Channels 0-7	Digital I/O, Port A Channels 0-7	Digital I/O, Port B Channels 0-7
RZ5, RZ5D, RZ6 Digital I/O Connector	Bit Addressable Digital I/O, Byte C Channels 0-7	Digital I/O, Byte A Channels 0-7	Digital I/O , Byte B Channels 0-7
RZ2 Analog I/O Connector	Not used	Analog Inputs Channels 1-8	Analog Outputs Channels 9-16
RZ5, RZ5D Analog I/O Connector	Not used	Analog Inputs Channels 1-4	Analog Outputs Channels 9-12

Mapping RA16BA I/O

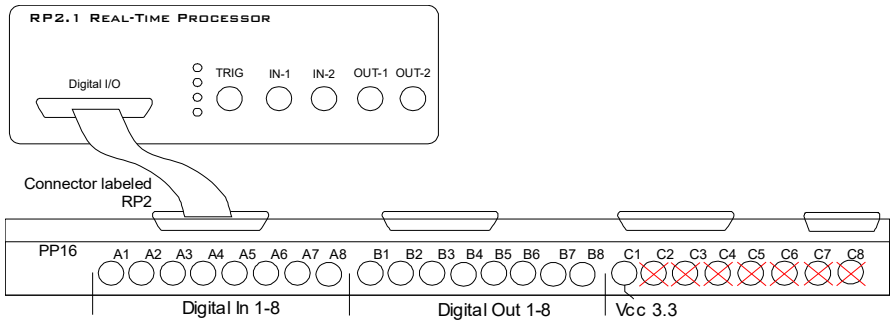
The diagram below maps the **RA16BA Digital I/O** connection to the PP16.



RA18BA to PP16 Connection Diagram

Mapping RP2/RP2.1 I/O

The diagram below maps the RP2 Digital I/O connection to the PP16. The last seven BNC connectors are not used. BNC C1 maps to VCC 3.3.



RP2.1 to PP16 Connection Diagram

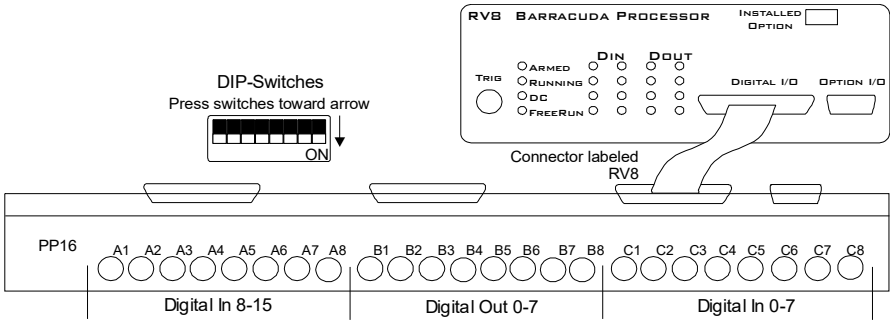
Mapping RV8 I/O

There are two connectors for the Barracuda on the rear edge of the PP16. The optional analog channels are on the DB9 connector and the digital I/O are on the DB25 connector. The PP16 is configured to accommodate 24 of the 32 inputs, outputs, and channels on the Barracuda, at any given time.

TDT ships a special cable that connects between the DB9 connector and the RV8.

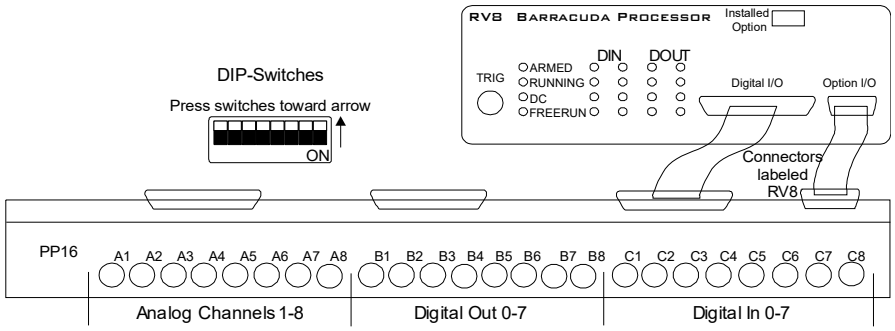
Connect the analog ground on the back of the PP16 to produce adequate signal quality.

The default connection for the Barracuda is shown below. In this format, sixteen digital inputs and eight digital outputs are configured as follows:



RV8 to PP16 Connection Diagram

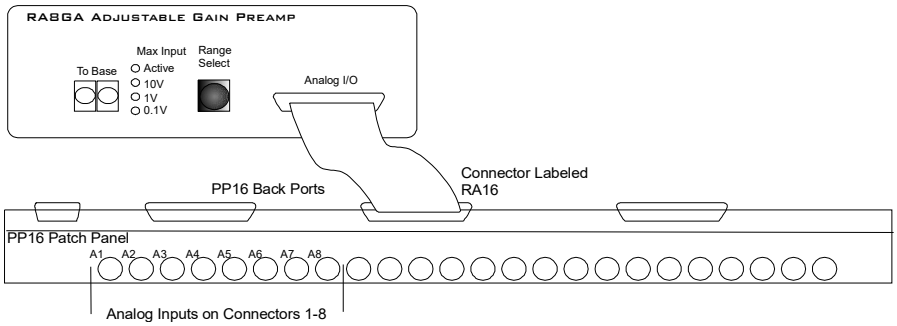
The optional connection for the Barracuda is shown below and uses both the DB25 and DB9 cables provided with the PP16. In this format, eight digital inputs, eight digital outputs, and the eight optional analog channels are configured as follows:



RV8 Optional I/O to PP16 Connection Diagram

Mapping RA8GA

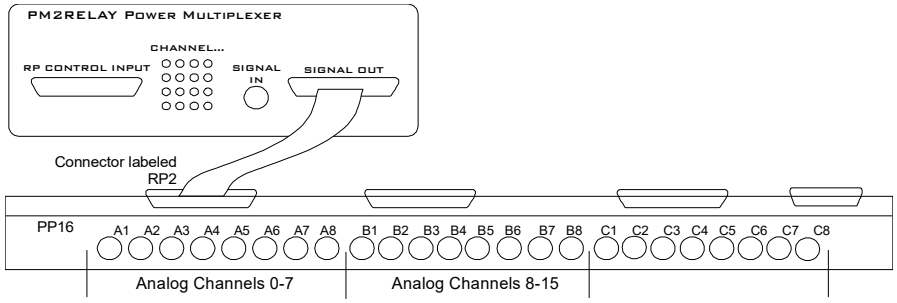
A PP16 patch panel can be used to simplify connection to the preamplifier's analog inputs. A ribbon cable can be connected from the RA8GA Analog I/O connector to the RA16 connector on the back of the PP16 allowing acquisition of signals via the first eight BNC connectors on the front of the PP16.



RA8GA to PP16 Connection Diagram

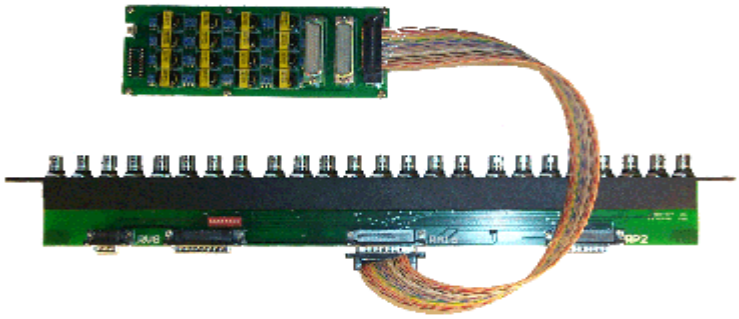
Mapping PM2R I/O

The diagram below maps the PM2R signal out connection to the PP16.



PM2R to PP16 Connection Diagram

Connect to the ETM1



ETM1 to PP16 Connection

The connector labeled J1 is used to connect the ETM1 to a PP16. Plug one end of a serial DB25 male-female cable into the J1 connector and plug the other end into the RA16 port of the PP16. Channels 1 - 8 and 9 - 16 of the headstages can be accessed through the patch panel BNCs labeled A1-A8 and B1 - B8, respectively. Also, a custom cable can be fabricated to connect the ETM1 (connector J1) to virtually any signal source.

PM2Relay Power Multiplexer

PM2R Overview

The PM2Relay (PM2R) is a 16 channel multiplexer for delivering powered and unpowered signals to a device. When coupled to a power amplifier such as the SA1, the PM2R can transfer several watts of power to standard four ohm and eight ohm speakers.

The PM2R is designed to be used as a "de-multiplexer", that is, one input switched to 16 possible outputs. However, it can also be used as a straight multiplexer (16 inputs to one output). This is accomplished by sending signals in to the 16 "signal out" channels. The selected channel will be output on the "signal in" channel. Users that are doing this should be very careful, as it is easy to exceed the maximum input values when sending in 16 input signals. **The aggregate input of all signals should never exceed two amps, or 15 Volts, because severe damage can be caused to the module.**

Each RP2 can control up to four PM2R devices and each PM2R can have one active channel. Therefore, a maximum of four signals can be played out simultaneously when using four PM2Rs.

To connect to a System 3 module, attach the 25-pin, blue ribbon cable from the RP2 device to the PM2R. Connect your powered signal source to the Signal In and connect the signal out to the RP2 connection on the PP16, or your own connectors. The channel outs on the PP16, from the left to right, correspond to the 16 channels (0-15) on the device.

Power

The device is powered via the System 3 zBus (ZB1PS). No PC interface is required.

PM2R Features

The PM2R uses a bit pattern code to control the output of a powered signal to one of sixteen output channels. The powered signal can come from any power amplifier such as the SA1 (Stereo Amplifier) or the HB7 (Headphone Buffer). The PM2R is

designed to use a bit-code pattern from an RP2 Real-Time Processor or RV8 Barracuda Processor.

RP Control Input

The male DB25 connector on the left is the interface to the RP2. A blue ribbon connector is used to directly connect the RP2 and the PM2R. The PM2R uses all the bit outputs from the RP2. If you require additional bit outs, TDT recommends purchasing an RV8.

In addition, any System 3 processor that has at least eight digital outputs, including the RX family of devices, can be used to control the PM2R (a special connector may be required).

Signal In

The BNC connector is the powered signal input. The maximum power input is a two amp, 15 Volt continuous signal or approximately 30 watts of continuous power.

Signal Out

The female DB25 connector on the right is the interface for the powered signal output. Users can also connect the PM2R output to the patch panel (PP16) connector labeled for the RP2 for easy BNC access to the powered signal.

Channel...

Sixteen LEDs indicate which channel is active. One channel can be active at a time. It is also possible to inactivate all channels.

PM2R Bitcode Pattern

The bitcode pattern from the RP2 consists of an 8-bit word that contains the following information; the device ID, the channel ID, and a set-bit. A final bit shuts off all channels. To control the PM2R, generate the bitcode pattern associated with the device and channel then send out the set-bit to change the channels. Be aware that the relays on the PM2R have a transition time of around one millisecond.

Bits 0 - 3 identify the channel number. Integer 0, or bitpattern (xxxx 0000), is channel 0 and integer 15, or bitpattern (xxxx 1111), is channel 15.

Bits 4 and 5 identify the device number. Integer value 0, or bit pattern (xx00xxxx), is device number 0 and integer value 48, or bit pattern (xx11xxxx), is device number 3. The device number is set internally for each PM2R and allows for an RP2 to control up to four PM2R modules. If only one PM2R is being used, it should have device number 0.

Bit 6 is the set-bit. When this bit is set high, the channel and device from the previous six bits is activated.

Bit 7 deactivates all channels across only the specified device.

The chart below shows the bit ID, its integer value, and its function.

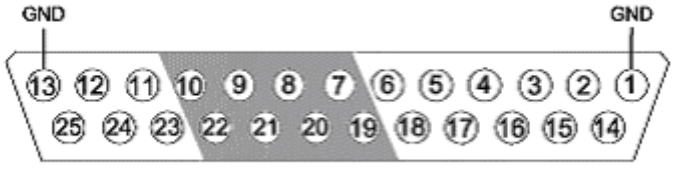
Bit Number	Integer Value	Function
0	1	Least significant bit of channel number
1	2	Bit 2 of channel number
2	4	Bit 3 of channel number
3	8	Most significant bit of channel number
4	16	Least significant bit of device number
5	32	Most significant bit of device number
6	64	Turns on the channel of the specified device
7	128	Turns off all channels on specified device only

Note: Make sure to put a delay of one sample between setting the channel number and turning the channel on. Trying to do both at the same time will not work correctly. For example, send "00000111" to select channel 7, and then send "01000000" one sample later to turn the channel on.

PM2R Technical Specifications

Switching Mode	Single 1-to-16/16-to-1
Switching Time	2 mSec
Input/output Level	+/- 15 Volts
Channel Cross-Talk	< -80 dB
S/N (typical)	90 dB
Maximum Allowable Current	2 Amps continuous

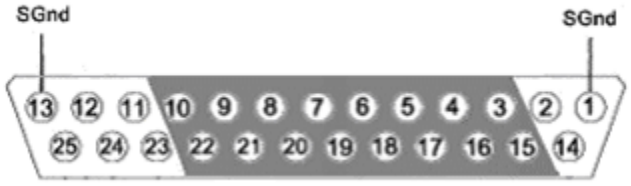
RP Control Input - DB25 Pinout



Digital Input Diagram

Pin	Name	Description		Pin	Name	Description
1	GND	Ground		14	NA	Not Used
2	NA	Not Used		15	NA	
3	NA			16	NA	
4	NA			17	NA	
5	NA			18	NA	
6	NA			19	D0	Digital Input Channels
7	D1	Digital Input Channels		20	D2	
8	D3			21	D4	
9	D5			22	D6	
10	D7			23	NA	Not Used
11	NA	Not Used		24	NA	
12	NA			25	NA	
13	GND	Ground				

Signal Output - DB25 Pinout



Analog Output Diagram

Pin	Name	Description		Pin	Name	Description
1	SGND	Signal Ground		14	NA	Not Used
2	NA	Not Used		15	A0	Analog Output Channels
3	A1	Analog Output Channels		16	A2	
4	A3			17	A4	
5	A5			18	A6	
6	A7			19	A8	
7	A9			20	A10	
8	A11			21	A12	
9	A13			22	A14	
10	A15			23	NA	Not Used
11	NA	Not Used		24	NA	
12	NA			25	NA	
13	SGND	Signal Ground				

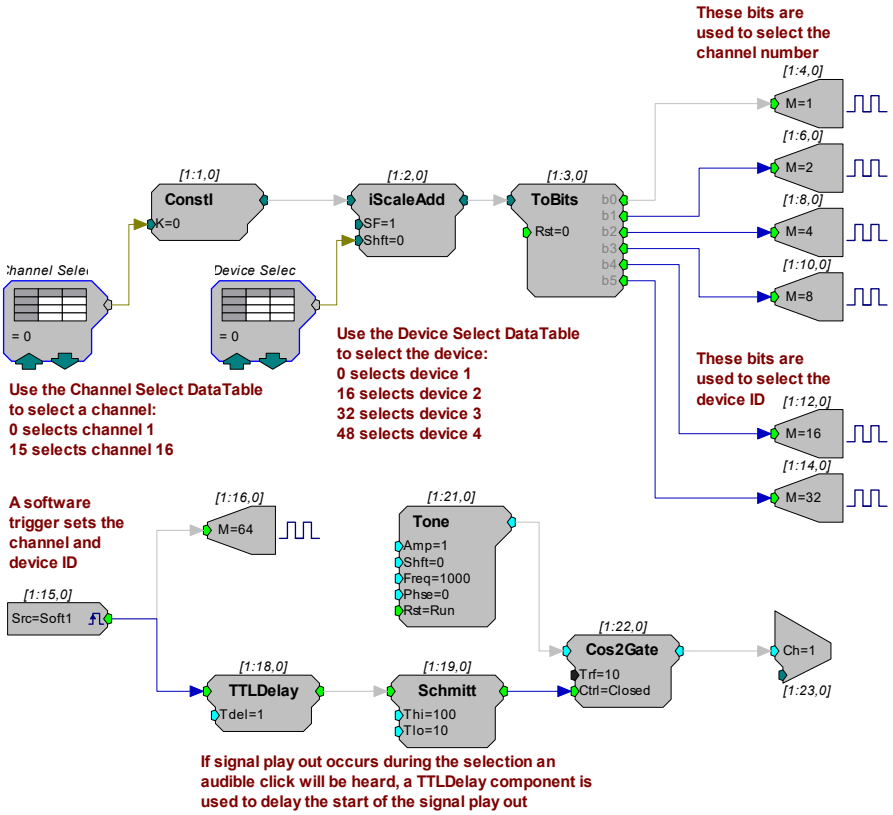
PM2R - Controlling Signal Presentation

The circuits described here use typical techniques for controlling the signal presentation when using a PM2R. These circuits have been designed as tutorials and will need to be modified to meet the needs of the individual researcher.

Controlling the PM2R with BitOuts:

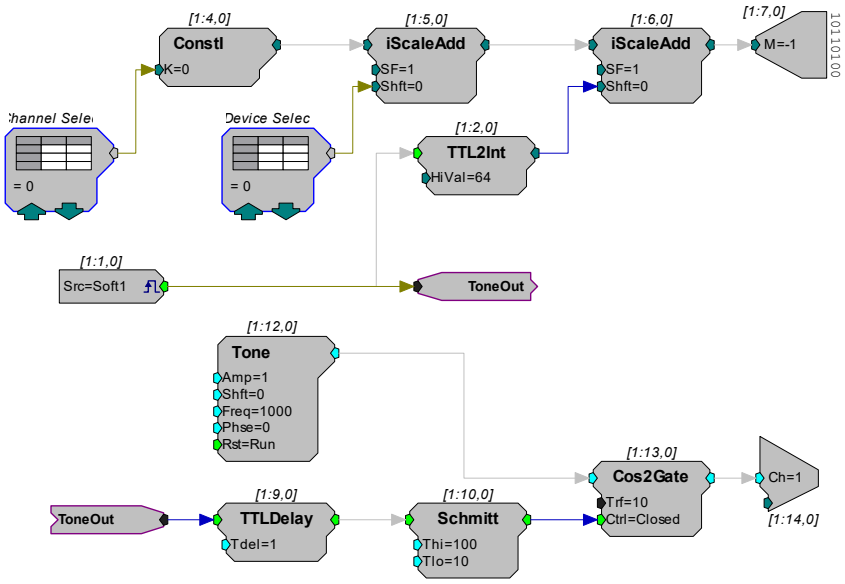
In this example several BitOuts are used to control the PM2R (via an RP2.1) from within RPvdsEx. The bit pattern is generated by two DataTable components. DataTables are commonly used to send values from the PC to the RP devices. While working in RPvdsEx, the selection can be changed by clicking the green up and down arrows near the bottom edge of the components. The first DataTable (Channel Select) stores the values for the channel number. Channel numbers start at zero and go to fifteen. Each RP2.1 is capable of controlling up to four PM2R devices. The second DataTable (DeviceSelect) stores the values for the device ID. The values in the table are 0 (device 0), 16 (device 1), 32 (device 2), and 48 (device 3). The iScaleAdd is used to add the integer values from both tables and the ToBits component changes the resulting integer to the bitcode pattern. The first four bits are used to select the channel number and the last two bits are used to select the device ID.

A software trigger is used to change devices and initiate a tone burst of 100 milliseconds duration. The software trigger causes the Schmitt trigger to open a gate for 100 milliseconds. The Schmitt trigger is delayed by one millisecond relative to the channel select. This removes the transient associated with the relays.



Controlling the PM2R with WordOut:

In this example a WordOut is used to control the PM2R (via an RP2.1) from within RPvdsEx. This simplified format decreases cycle usage. An additional iScaleAdd is required because the BitOut and WordOut components function differently and should not be used in the same circuit. As before, a software trigger initiates the start of the stimulus presentation. The triggered signal adds 64 to the output to change the channel.



Controlling the PM2R from a run-time application:

The examples described here could easily be modified to allow control from run-time applications. Parameter tags can be included and used in other applications such as BioSigRP or OpenEx.

SM5 Signal Mixer

SM5 Overview

The SM5 is a three-channel signal mixer. The relative contribution of the three inputs to the final output can be adjusted using a variable gain for two of the inputs. In addition, the signal on the two adjustable channels can be inverted before addition. The input signal range is ± 10 V for each channel, with the additional caveat that the amplified signal for each channel may not exceed ± 10 V without clipping. The range for the summed output is ± 10 V.

Power

The SM5 Signal Mixer is powered via the System 3 zBus (ZB1PS). No PC interface is required.

SM5 Features

The SM5 Signal Mixer is a three-channel weighted summer with variable input weighting and channel inverting. The SM5 is a zBus rack mounted device, through which it receives power.

Inputs

Three signals input channels (A, B, and C), with a range up to ±10 V peak, are accessed through front panel BNC connectors. Input channels A and B are multiplied by a weighted, signed constant, K, before being added to the final output. The weighting range for these two channels is adjustable from -20 dB to +20 dB (i.e. |K| = 0.1 to 10) using a GAIN knob on the front panel. The sign of K for channels A and B can also be selected using front panel toggle switches, labeled INV-A and INV-B.

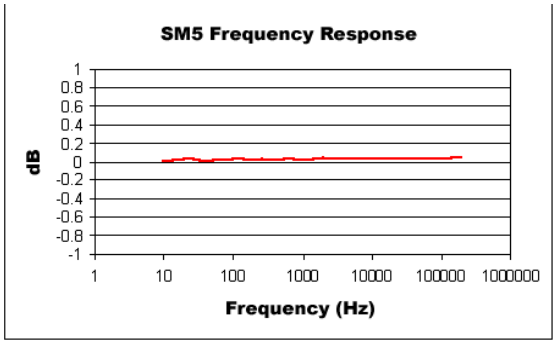
If an input is not being used, it should be grounded by attaching a shorted BNC cable. This will prevent unwanted noise from being added to the output.

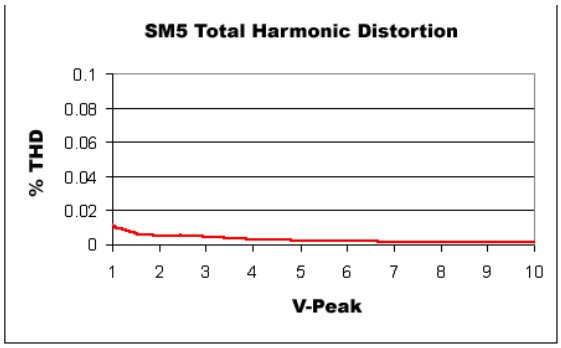
Clipping

The variable weighting provides a great deal of flexibility in input and output signals. However, care should be taken to avoid clipping any signal component. The SM5 output signal = (Ka∗A) + (Kb∗B) + C is limited to ±10V peak. In addition, the raw inputs, A, B, and C, as well as the weighted inputs, Ka∗A, and Kb∗B, are limited to ±10V peak.

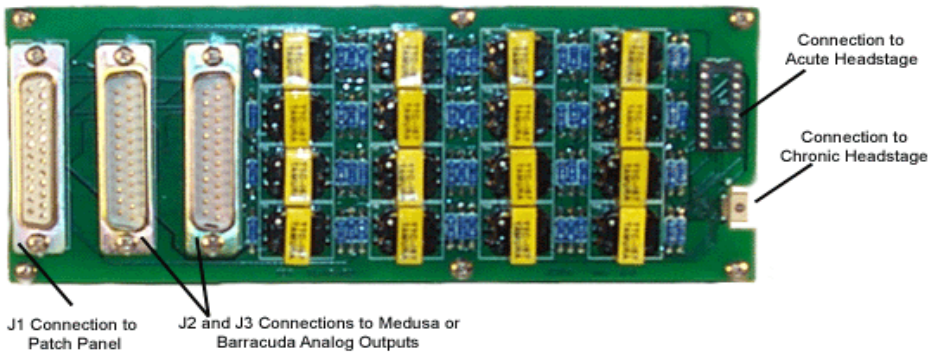
SM5 Technical Specifications

Input Signal Range	± 10 V peak
Weighting Range	-20.0 to +20.0 dB
Max Output	± 10 V
Spectral Variation	< 0.1 dB from 10 Hz to 200 kHz
S/N (typical)	111 dB (20 Hz to 80 kHz)
THD	< 0.002% (1kHz tone +/- 7V peak)
Noise Floor	19 µV rms
Output Impedance	20 Ohm
Input Impedance	10 kOhm
Inversion	Channels A & B





ETM1 Experiment Test Module



Overview

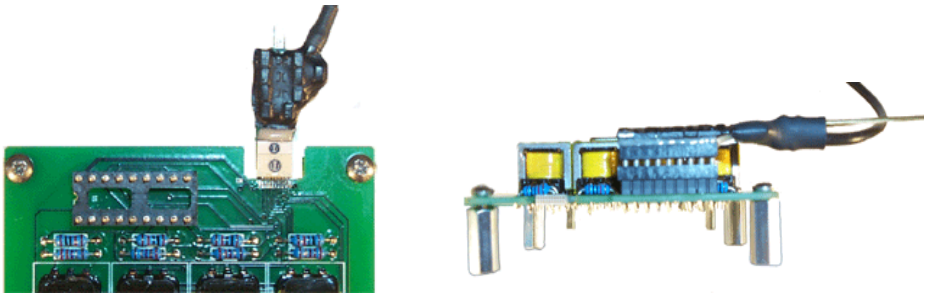
The Experiment Test Module (ETM1) allows you to design and test experimental protocols before running critical experiments and can be used to input signals into either the chronic (RA16CH) or acute (RA16AC) headstages from the analog outputs of the Medusa (RA16BA) or Barracuda Processor (RV8). The ETM1 also accepts signals via the Patch Panel (PP16). A processor can be used to generate signal spikes that simulate a physiological recording. The simulated spike signals can then be passed through the ETM1 and acquired by the connected headstage. The ETM1 also includes a connection to receive signals via the Patch Panel (PP16). Using the PP16, virtually any signal source can be used. The ETM1 allows the experimental setup to be tested without using a subject.

There is 1000 to 1 signal attenuation in the ETM1. Therefore, 1 V on the input is equivalent to 1 mV on the output to the headstage. The ETM1 uses transformer isolation of the incoming signal to the resulting output to the headstages.

Inputs, or processor and patch panel connections, are located on one end of the device and output, or headstage connections, are located on the other end of the device.

Connecting the Headstage

Connect the headstage to the corresponding connector on the ETM1.



Chronic Headstage connected to ETM1 Acute Headstage connected to ETM1

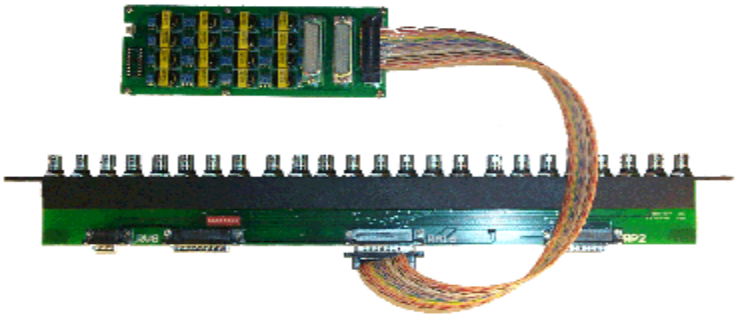
Connecting the Signal Source

The connectors labeled J1, J2 and J3 are used to connect the ETM1 to signal sources. The first eight-headstage channels (1-8) are wired to connector J2. The other eight-headstage channels (9-16) are wired to connector J3. All 16 channels are wired to connector J1. See "ETM1 Technical Specifications" on page 19-33, for pinouts.

Connecting to an RA16BA or RV8

For headstage channels 1-8, plug one end of a serial DB25 male-female cable into the J2 connector and plug the other end into the Analog/Digital I/O Port of an RA16BA or RV8. For headstage channels 9-16 plug one end of a serial DB25 male-female cable into the J3 connector and the other end into the Analog/Digital I/O port of a second RA16BA or RV8.

Connecting to the PP16



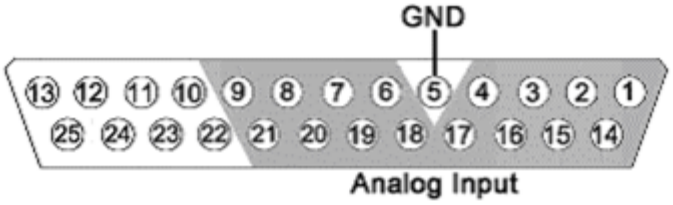
The connector labeled J1 is used to connect the ETM1 to a PP16. Plug one end of a serial DB25 male-female cable into the J1 connector and plug the other end into the RA16 port of the PP16. Channels 1 - 8 and 9 - 16 of the headstages can be accessed through the patch panel BNCs labeled A1-A8 and B1 - B8, respectively. Also, a custom cable can be fabricated to connect the ETM1 (connector J1) to virtually any signal source.

ETM1 Technical Specifications

Maximum Input	Should not exceed the maximum input for your amplifier (such as 4V for the RA16PA)
Frequency Response	Flat from 500 - 20,000 Hz
Highpass Filter (Fc)	20 Hz
S/N (typical)	70 dB
THD (Typical)	0.01% for 1 kHz input at 1 V peak-to-peak
Cross-Talk	< -70 dB
Attenuation	60 dB

J1 DB25 Pinout

Analog input channels 1-16. The J1 connector is typically used to input signals from the PP16 Patch Panel.



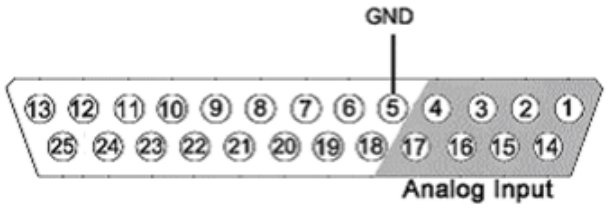
Note: Female pin-in shown.

Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		14	A2	Analog Input Channels
2	A3			15	A4	
3	A5			16	A6	
4	A7			17	A8	
5	NA	Not Used		18	A9	
6	A10	Analog Input Channels		19	A11	
7	A12			20	A13	
8	A14			21	A15	
9	A16			22	NA	Not Used
10	NA	Not Used		23		
11				24		
12				25		
13						

J2 DB25 Pinout

Analog input channels 1-8. Typically used to input signals from the RA16BA or the RV8.

Note: Female pin-in shown.

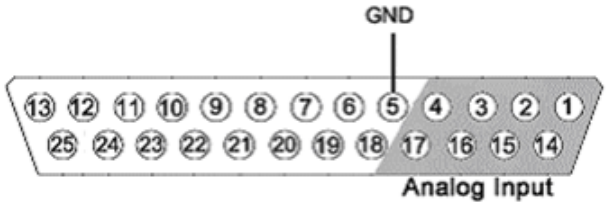


Pin	Name	Description		Pin	Name	Description
1	A1	Analog Input Channels		14	A2	Analog Input Channels
2	A3			15	A4	
3	A5			16	A6	
4	A7			17	A8	
5	GND	Ground		18	NA	Not Used
6	NA	Not Used		19		
7				20		
8				21		
9				22		
10				23		
11				24		
12				25		
13						

J3 DB25 Pinout

Analog input channels 9-16. Typically used to input signals from the RA16BA.

Note: Female pin-in shown.



Pin	Name	Description		Pin	Name	Description
1	A9	Analog Input Channels		14	A10	Analog Input Channels
2	A11			15	A12	
3	A13			16	A14	
4	A15			17	A16	
5	GND	Ground		18	NA	Not Used
6	NA	Not Used		19		
7				20		
8				21		
9				22		
10				23		
11				24		
12				25		
13						

Part 20: PC Interfaces

Interface Transfer Rates

Transfer rates depend on a number of factors, including the device accessed the type of transfer, and cycle usage.

The table below includes typical transfer rates for the Optibit and USB interfaces at a 50% cycle usage with RP/RX and RZ devices. All values are MB/s.

Interface	Transfer Type	RP/RX	RZ
PO5/PO5e/FO5/LO5	Read	1.5/4.0	8.0
	Write	1.0	8.0
UZ3	Read	Not Supported	6.0*
	Write	Not Supported	6.0*
UZ2	Read	1.5	Not Supported
	Write	1.0	Not Supported

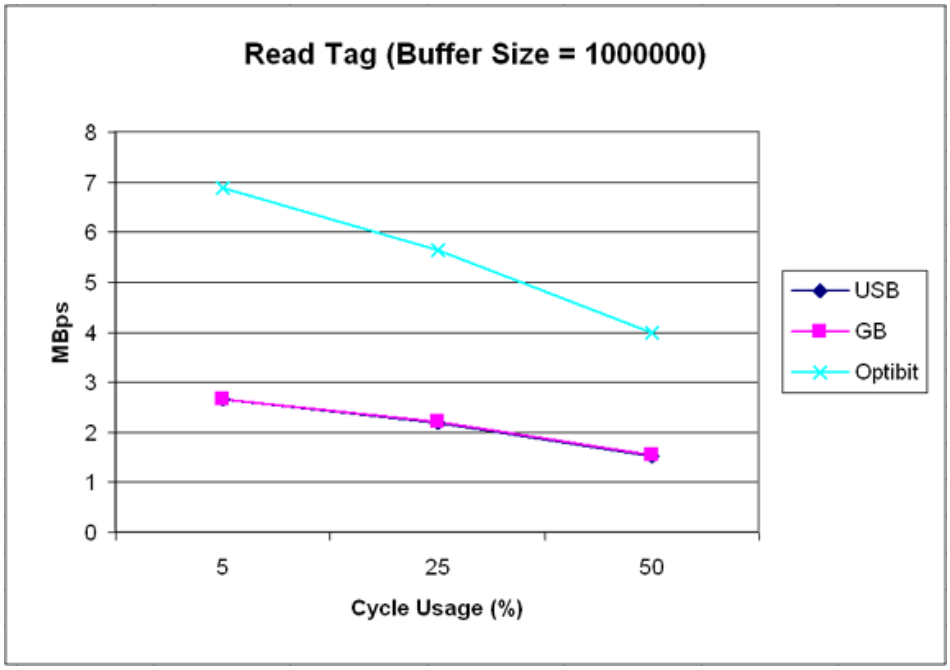
***UZ3 transfer rates are highly dependent on the specs of the computer.**

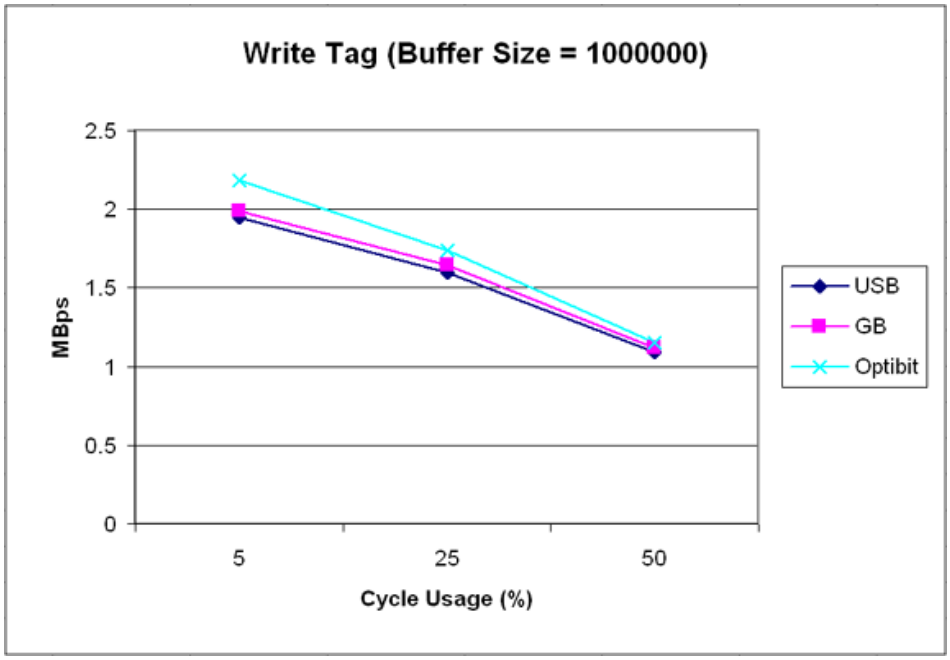
Because of the overhead required to poll the hardware or run single commands with the USB interface, users should be aware of the following relationships when performing small data transfers with the UZ2.

Interface	Transfer Type	RP/RX
UZ2	Snippet Transfers (~100)	0.3 MB/s
	Single Commands	1000 Commands/s

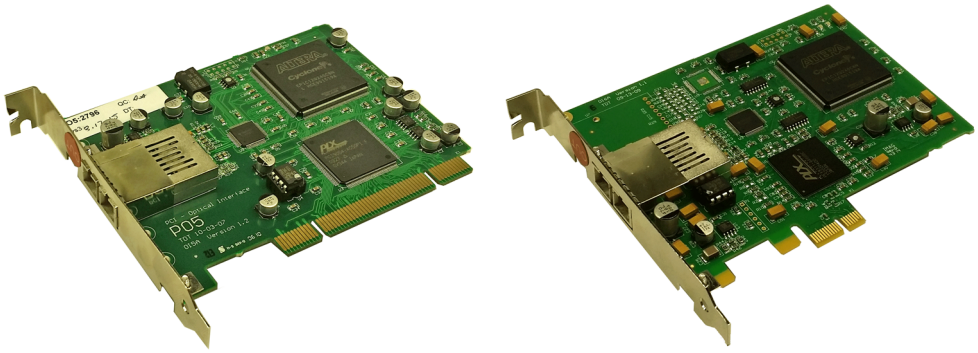
Cycle Usage and Large Transfers

The following graphs show how the cycle usage affects the transfer rate for large transfers with the Optibit, Gigabit, and USB 2.0 interfaces with an RX device. The data was collected using a buffer size of 1,000,000 for the Read Tag and Write Tag commands. The transfer rates were tested using both the RP2.1 (a single processor device) and only the main processor of an RX6 and using circuits generating cycle usages of 5, 25, and 50 percent.





PO5/PO5e Optibit Interface



PO5 (left) and PO5e (right)

Optibit Overview

The Optibit system (Optical Gigabit) is designed for users that require high-speed real-time control of System 3 devices or precise system-wide device synchronization. The Optibit interface consists of a PCI card (PO5) or PCIe card (PO5e) that must be installed in the computer and one or more Optibit-to-zBus interface modules (FO5) that mount in the rear slot of a zBus device chassis or is built into RZ Processors. The Optibit interface is up to 8x times faster than the original Gigabit interface and also reduces the system's susceptibility to EMF. Also, when using the Optibit interface, all devices (across all chassis) are automatically phase locked to a single clock.

Part Numbers:

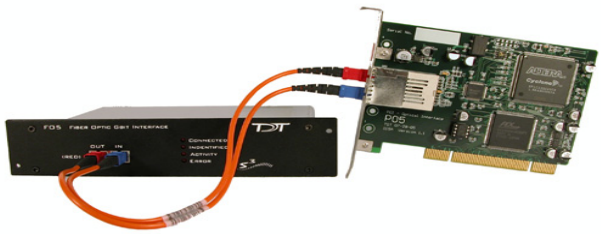
PO5—Optical PCI Card for Hardware/Software Control

PO5e—Optical PCI Express Card for Hardware/Software Control

FO5—PO5 to zBus Interface

Fiber Optic Connection

Devices are connected in a simple loop using provided high speed noise immune fiber optic cabling. See the *System 3 Install Guide* for installation instructions.



FO5 Status LEDs

Four status LEDs on the face of the FO5 indicate the connection status of the interface.

Connected The Connected LED is lit when the interface is powered on and the fiber optic cable labeled IN is connected properly. Although the Connected LED will light if only the IN cable is connected, both cables have to be connected properly for communication to take place.

Identified The Identified LED lights when a software signal sent from the PC is recognized by the interface. This takes place when launching TDT software such as zBusMon, RPvdsEx or loading an OpenEx project.

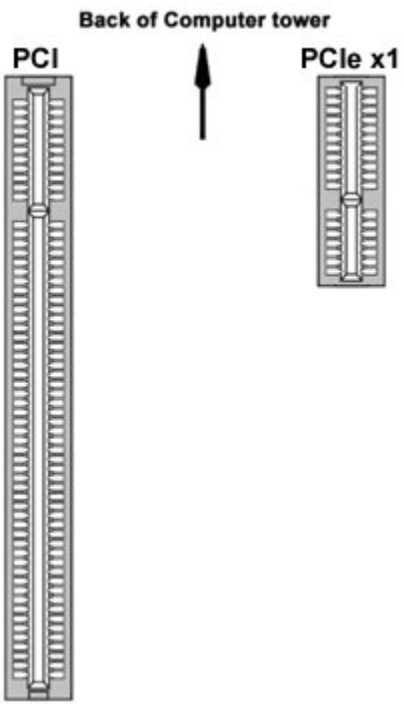
Activity The Activity LED is lit when data is being sent to or from the TDT hardware.

Error The Error LED lights when there is a connection or communication error. For example, this LED will light if the fiber optic cables are not connected properly.

PO5/PO5e Technical Specifications

Interface transfer rates vary by transfer type and device. See "Cycle Usage and Large Transfers" on page 20-4, for more information.

Below is a diagram of the compatible PCI and PCIe slots used with the PO5 and PO5e Optibit Interface cards.



PO5e

The PO5e must be installed in a PCI Express slot. The PO5e card uses a single lane (x1) but may be used in any PCIe slot size (x1, x2, x4, x8 or x16).

PO5

The PO5 zBus to PC interface card must be installed in a standard size, compliant 3.3 V slot. The PO5e zBus to PC interface card must be installed in a PCI Express slot.

Notes:

Do not install in a PCI-X slot—the interface might fail.

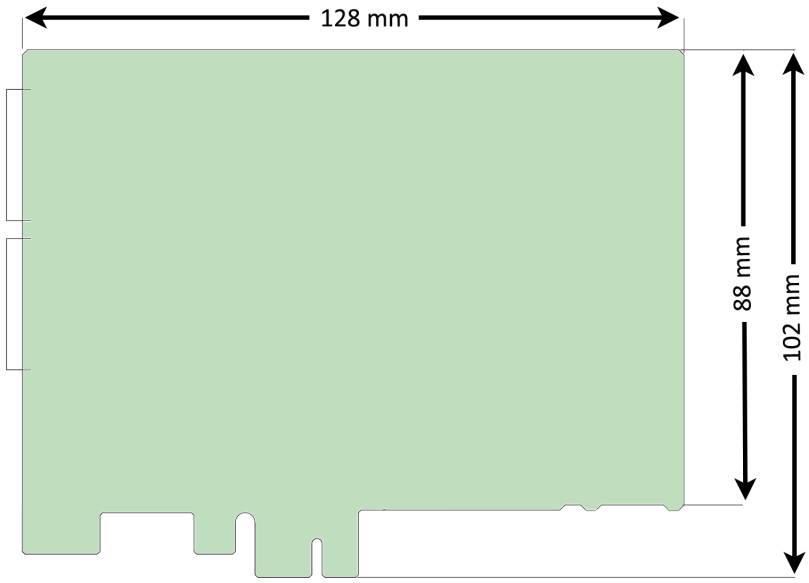
Do not attempt to install in low-profile PCI slots. While low profile and standard PCI cards maintain the same electricals, protocols, PC signals, and software drivers as standard PCI expansion cards, the low profile bracket is not compatible with standard cards.

Fiber Optics

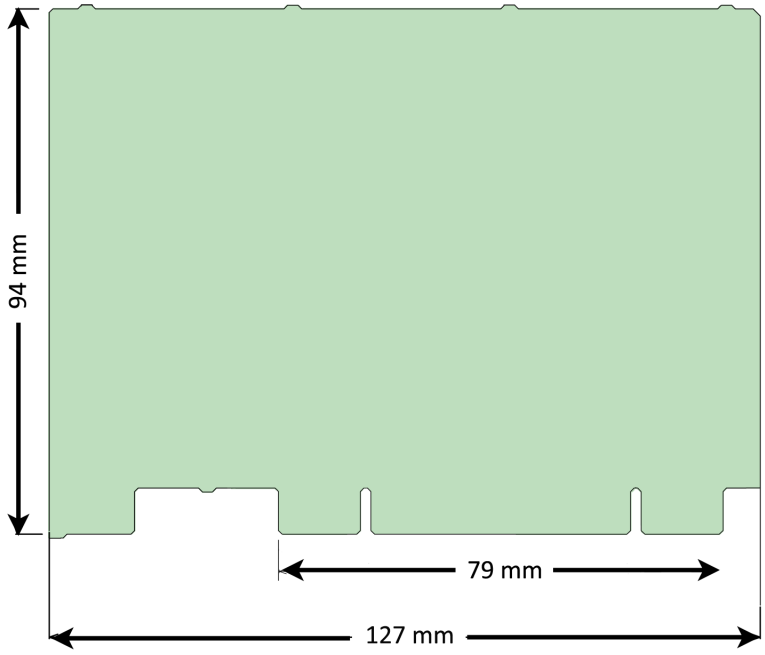
Maximum cable length: 30 meters

Dimensions

PO5e



PO5



Technical Specifications for the PO5e PC Interface:	
Standard Cable Length	5 meters (longer cables available on request)
Computer Interface	PCIe card, size 1x or larger, full height

UZ3 USB 3.0 Interface for Optibit

UZ3 Interface

UZ3 Overview

The UZ3 is a fiber optic interface to a high speed USB 3.0 port on your laptop or PC. It can connect to one or more RZ Processors. RX and RP devices are not supported by this interface.

A USB Type C-C cable and C-A adapter are included.

Part Numbers:

UZ3—USB 3.0 Interface

UZ3 Technical Specifications

Interface transfer rates vary by transfer type and device. See “Cycle Usage and Large Transfers” on page 20-4, for more information.

The UZ3 can handle roughly 50-75% of the data rate of the PO5/PO5e card and should not be used for high channel count applications. The actual maximum rate is dependent on your PC specs.

The status LED is on by default when connected and flashes off when there is transfer activity.

Note: In UZ3 serial number 1021 and below, the LED is off by default and flashes on when there is activity.

Do not use with a USB 2.0 port. Use zBusMon software to measure the transfer rate to see if you are getting high speed data transfer.

The UZ3 dimensions are 31mm x 21mm x 106mm.

UZ2 USB 2.0 Interface

Overview

The USB 2.0 zBus Interface mounts in the rear bay of a zBus device chassis and handles communication and data transfer between your computer and zBus mounted programmable devices, such real-time processors or programmable attenuators. Most nonprogrammable devices, such as speaker drivers or signal mixers, do not require an interface. You will need a USB2.0 port available on the host PC for each UZ2 in a multi-chassis system. We recommend upgrading to an Optibit interface if a system requires more than three chassis.

Note: If using the USB 2.0 interface on a 64-bit operating system, you must install version 76 TDT drivers or greater.

Connecting the UZ2

The UZ2 connects to your computer with standard USB 2.0 A to B cables (provided with each module). Interface drivers are bundled with the TDT Drivers and will be installed when the device is connected to the host computer for the first time. The UZ2 can be safely connected or unconnected while the computer is running.

Important! Wait ten seconds after devices have gone through the boot sequence or 30 seconds after turning on devices (with the computer already running) before running applications that use TDT devices. We also recommend using zBUSmon to verify the logical order of devices before beginning any experiment. See "Boot Up Sequence" below, for more information.

Sync

The Sync allows users to synchronize several modules that are mounted in different device chassis. Each USB module has its own clock. Clocks on multiple USB devices will drift relative to each other. The Sync line uses the clock from one USB module, the master, to synchronize the clocks across all zBus device chassis.

To connect several zBus chassis, one module (the highest logical module) is designated as the master and the other clocks are slaved to the master clock. Connect the Sync Out of the master clock to the Sync In of the slave with a short

patch cable. To connect several device chassis, daisy-chain the connections between the slave chassis as shown below. When the Sync lines are connected correctly the LED to the left of the Sync connectors should be lit on each slave devices. The LED on the master will remain unlit. The LED should only flash when the Sync lines are not connected.

Sync LEDs	Indicates
Flashing (on slave)	Connected incorrectly
Master device not lit and slave devices lit	Connected correctly
No devices lit	Not synced to any device

Logical Order of Devices

The logical order of devices is determined each time the zBus chassis are powered on. You can verify the current logical order using the zBUSmon software.

Boot Up Sequence

The boot up sequence for the USB 2.0 interface is driven from the PC and follows the communication protocol described below.

The first time the hardware is turned on a device driver is loaded to the interface. Depending on your operating system, the PC might beep to indicate that the device driver has been loaded.

A second set of drivers will be loaded and the devices will reboot.

The TDT hardware is queried to determine the logical order of the devices and zBus chassis.

Important! If the zBus is accessed during step three, the devices will fail to ID. To ensure that step three is completed, wait ten seconds after the devices have rebooted (step two) before loading any TDT application or viewing the devices in zBUSmon. If the hardware fails to ID shut down the TDT hardware and restart the device.

LO5 ExpressCard to zBus Interface

LO5 Overview

The LO5 ExpressCard to zBus Interface model provides a means of controlling System 3 devices from a laptop (or any computer with an ExpressCard slot) and offers performance comparable to the Optibit system (Optical Gigabit).

The entire interface system consists of a 34mm (26 pin) ExpressCard that is attached with a cable to a free standing fiber optic interface module. The module can then connect to the zBus optic port on any RZ device or via an FO5 housed in a zBus chassis. When connecting to a multiple device system, devices are daisy-chained together with multiple fiber optic cables.

The LO5 module requires AC power.

Part Numbers:

LO5—ExpressCard to zBus Interface module (includes express card)

LO5 Technical Specifications

The ExpressCard must be installed in a 34mm (26 pin) slot.

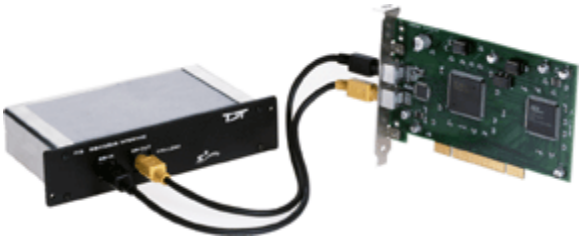
Standard fiber optic cable length: 5 meters (30 max available)

Interface Transfer Rates vary by transfer type and device. See "Interface Transfer Rates" on page 20-3, for more information.

Hardware Set-up

The System 3 hardware, LO5, and ExpressCard should all be connected before turning on the laptop. If the system is not connected before boot-up, the LO5 may fail to initialize and will not appear in zBUSmon. If the LO5 does not initialize, unplug the system and reconnect to the ExpressCard. If the LO5 still does not initialize, ensure all devices are connected and powered on, then reboot the laptop.

Gigabit Interface



PI5 Overview

The Gigabit system is no longer available. It consists of a PCI card (PI5) that fits in the computer and one or more GBit-to-zBus interface modules (FI5) that mounts in the rear slot of a zBus device chassis. Devices are connected in a simple loop using provided cabling. When using the gigabit-interface all devices (across all chassis) are automatically phase locked to a single clock. Over 100 devices can be connected in a single Gigabit loop with automatic device identification and system initialization.

Part Numbers:

PI5—PCI Card for Hardware/Software Control

FI5—PI5 to zBus Interface

PI5 Technical Specifications

The PI5 zBus to PC interface card must be installed in a standard size, PCI v 2.2 or greater, compliant 3.3 V slot.

Maximum cable length: 30 meters

Interface Transfer Rates vary by transfer type and device.

Notes: Do not install in a PCI-X slot—the interface might fail.

Do not attempt to install in low-profile PCI slots. While low profile and standard PCI cards maintain the same electricals, protocols, PC signals, and software drivers as standard PCI expansion cards, the low profile bracket is not compatible with standard cards.

Gigabit Anomalies and Tech Notes

The PI5 is not compatible with the WindowsXP and 2000 Standby and Hibernate features. We recommend configuring PC Power Options to never use these modes for any PC used to run TDT applications.

Problems loading drivers may occur when the C:WINNT/inf folder is not visible. In Windows Explorer choose Tools|Folder Options, then choose View|Hidden Files and Folders, and select Make Visible.

When data is being transferred from the TDT hardware to the computer, CPU usage on the computer goes up to 100%. The computer is still usable (can ran other programs, etc.) despite the high CPU usage, however, other programs that are running on the computer may slow down.

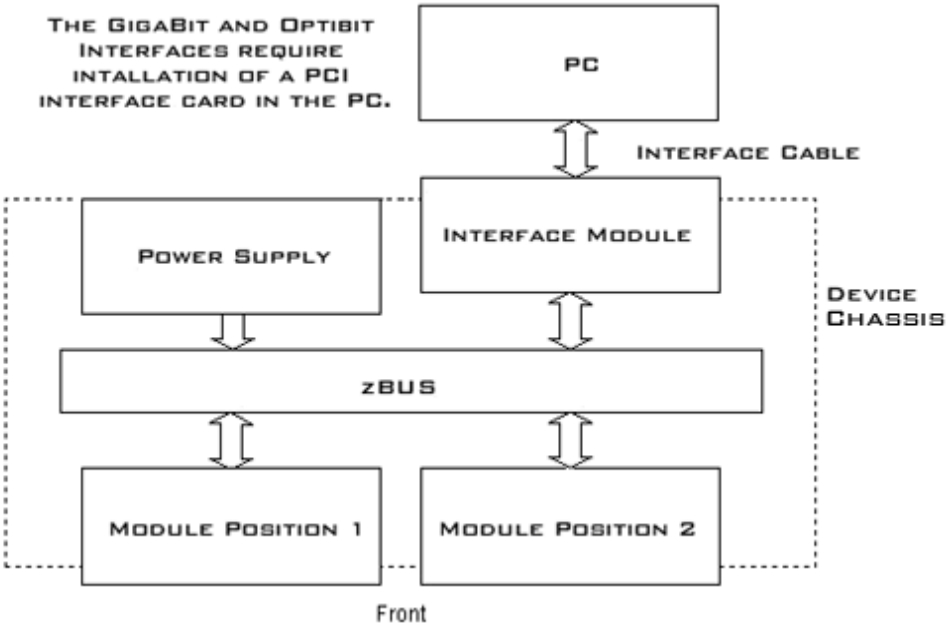
After installing the Gigabit PCI card in your computer, there may be a conflict with how the PC communicates with the card and other devices in the system. This could lead to the following error message when performing a transfer test in zBUSmon: "System Test Error: Cycle power on system and test again." If you experience system problems and find the IRQ number to be the same on another device, then you should move the PI5 card to another PCI slot in your machine.

Part 21: The zBus and Power Supply

ZB1PS - Powered zBus Device Chassis

Overview

zBus is TDT's high-speed, low-noise bus for System 3 modules. The bus is integrated into a device chassis, which serves as a rack mountable housing for most modular devices in the System 3 line. As seen in the functional diagram below, the bus distributes communication and power throughout the system.



zBUS Functional Diagram

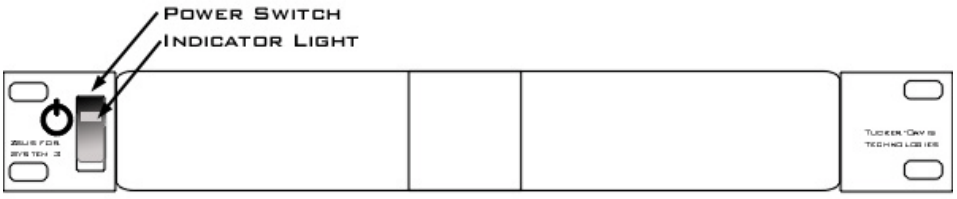
One or two modular devices can be mounted in the chassis' front bays, providing easy access to front panel connections. An interface module can be mounted in the second rear bay for chassis housing a programmable device. Multiple chassis can be interfaced for custom system configurations and individual modules can be added or removed as needed.

Power Supply

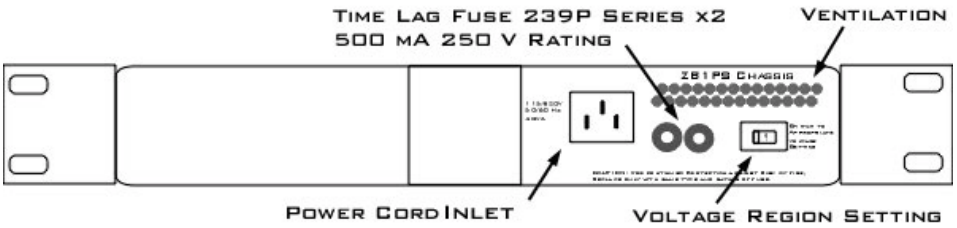
The ZB1PS chassis features an onboard, switchable (115V/220V) power source. The power supply is integrated into the chassis and cannot be removed. A small fan is located inside of the power supply and provides cooling while the power supply is active.

See the *ZBPS1 Operations Manual* for power and safety information.

Using the ZB1PS



Front View



Back View

Applying Power to the Chassis

CAUTION! Allow at least 2 cm clearance from each side of the chassis for proper cooling. A ventilation fan is provided on the right side of the chassis. Ventilation holes are also provided on the power supply panel and another internal fan is provided inside the power supply housing. Installation of the chassis with the ventilation obstructed may cause a malfunction or fire.

CAUTION! Use only the supplied power cord.

To turn the ZB1PS on:

1. Position the chassis so that both the power switch and power cord may be accessed easily.
2. Ensure that the power switch is off then connect the power cord.
3. Ensure that the voltage region switch is set correctly. For standard outlets in the United States it should be switched to 115 V.
4. Turn the power switch on. The power switch's green LED should be illuminated.

The Indicator Light

A front panel switch turns on the chassis power supply and includes an indicator light. The power switch's green LED will illuminate when the chassis is switched on. The light will flash rapidly when it receives a command from software and slowly to indicate a communications error (check all cable connections).

Disconnecting Power from the Chassis

CAUTION! When removing the power cord from either the power supply or socket outlet, grasp the plug, not the cord, in order to avoid damaging the cable.

To disconnect the ZB1PS:

1. Turn off the power switch.
2. Disconnect the power cord from the power supply.
3. Disconnect the power cord from the wall socket plug.

Adding and Removing Modules

Before adding or removing modules, make sure the zBus is powered off.

To remove a module from the chassis:

1. Unscrew the two thumb screws on the corner of the module faceplate.
2. Pull straight out on the front-panel BNC connectors. A BNC 'T' connector makes a great handle for removing zBus devices.

To add a module to a chassis:

1. Insert the module into an empty bay and push straight back until it seats onto the connector.
2. Hold the module in place with the thumb screws.

ZB1PS Technical Specifications

Chassis	
Height	1U
Width	Standard 19" (482.6 mm) rack mount
Power Supply (Integrated)	
Maximum Working Voltage	HI to earth ground 230 V max LO to earth ground 230 V max
Main Voltage Rating	115/230 V, 50/60 Hz, 40 VA AC
Installation Category	CAT II
Environmental	
Operating Temperature	0 to 45°C
Storage Temperature	5 to 40°C
Humidity	80% for temperatures up to 31°C, decreasing linearly to 50% RH at 40°C
Maximum Altitude	2,000 m
Pollution Degree	2 (Indoor use only)
Power Supply Fuses	
Time Lag Fuse 239P Series	2 fuses
Operating Temperature	-55℃ to 125℃
Ampere Rating	0.500 A
Voltage Rating	250 V
Interrupting Rating	10,000 amperes at 125 VAC, 0.7-0.8 power factor 35 amperes at 250 VAC, 0.7-0.8 power factor

ZB1 Device Caddie and PS25F Power Supply

The ZB1 and PS25F are TDT's legacy zBus chassis and power supply. The ZB1 device chassis is similar to the newer ZB1PS; however, it does not have onboard power and must be used in conjunction with the PS25F.

WARNINGS! The PS25F power supply must be placed in the right hand bay of a ZB1 Device Caddie as you look at the back of the chassis. It can damage the system if it is placed in any other bay.

No other power supply can be used to power the zBus.

The two voltage switches should be switched to the mains voltage for your country. For example, in the United States these should both be switched to 115 V.

Part 22: System 3 Utilities

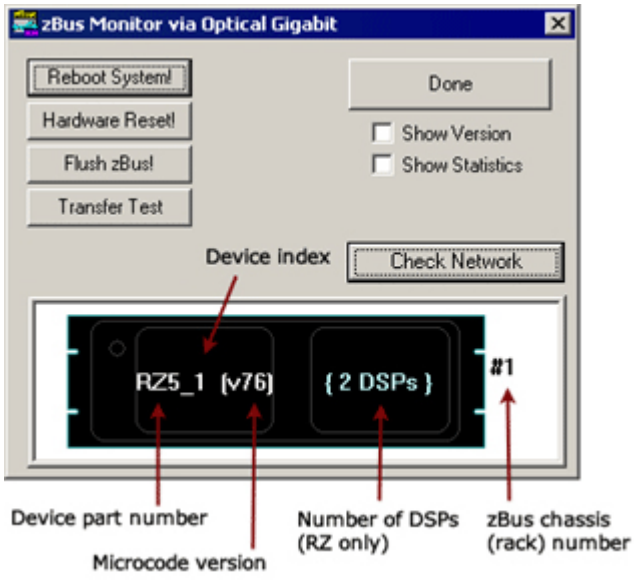
zBUSmon Interface Testing Software

The zBus Monitor program is a tool used to test the USB, Gigabit, or Optibit connection to System 3. It is also be used to update the microcode firmware on programmable devices.

This program is installed in the C:\TDT\zDrv3 directory by default and a shortcut is added to the Desktop and to the TDT Sys3 Directory in the Start menu.

The zBUSmon Window

When the utility is run a small monitor window is opened. All correctly connected zBus or built-in device chassis housing a programmable device, such as the RZ2 and PA5, are represented in the system diagram. Chassis housing non-programmable devices, such as the SM5 or HB7, are not displayed.



The device part number and index for each device along with the zBus chassis numbers are displayed in the system diagram. The version number of each programmable device's firmware (TDT Microcode) is also displayed within parentheses next to each device. See "Updating the Microcode" on page 22-6, for more information about the microcode.

For RZ devices, the number of installed DSPs detected is displayed on the right side of the device in the diagram. "{DSP ERROR}" is displayed in red if a DSP is expected but not identified.

Reboot System!

The **Reboot System!** button resets all hardware in the system and reloads device drivers.

To reboot a single chassis (rack) within the system, right-click it in the diagram and click **Reboot Rack** on the shortcut menu.

Hardware Reset!

The **Hardware Reset!** button resets connected hardware and clears all circuits and zBus triggers.

Flush zBus!

The **Flush zBus!** button flushes interface line of commands or data.

Transfer Test

The **Transfer Test** button tests communication between the TDT modules and the PC. This will test data transfer both to and from the PC. A progress bar is displayed indicating how much time is remaining in the test. The button text changes to "Cancel Test" during a transfer test. Click this button to end the test early.

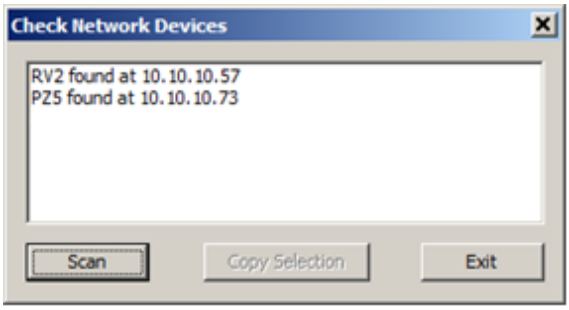
Update All Devices

The Update All Devices button automatically programs any out of date devices in the system with the current microcode. See "Updating the Microcode" on page 22-6, for more information about the microcode (displayed only when multiple devices connected).

Check Network

The **Check Network** button searches across an available network connection and identifies other system 3 devices with an IP address; such as the PZ5 Amplifier, RV2 Video Tracker, or RS4 Data Streamer.

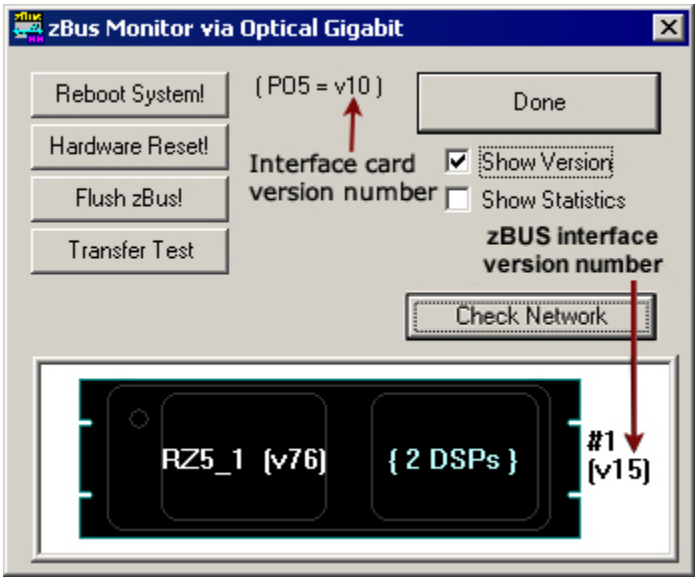
The user can click **Scan**, to rescan the network for newly connected devices.



The **Copy Selection** button enables users to place the line of characters (including the IP address) onto the windows clipboard, making it available to paste in other applications. To copy the characters, select the desired device, then click the **Copy Selection** button.

Show Version Check Box

When the **Show Version** box is checked, the version numbers of the PC to zBus interface firmware are displayed in the hardware diagram (see figure below). The FO5/PO5 interface shows v10. The RZ interface shows v15. Do not worry if these numbers don't match.

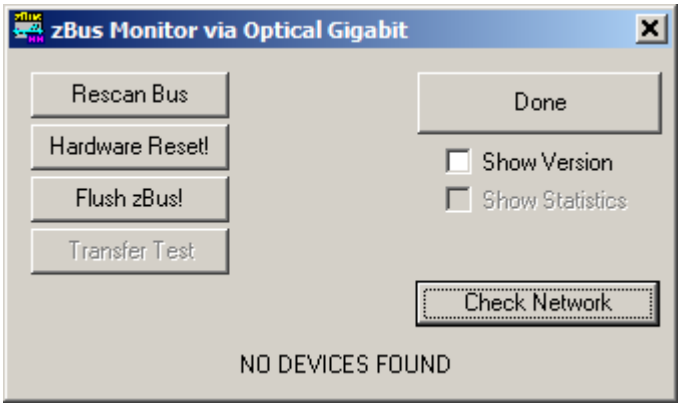


Show Statistics

The zBUSmon program, when used with the Optical Gigabit (PO5 or PO5e) interface, provides an additional option to view system statistics. When **Show Statistics** is checked, the window expands to display the amount of data transferred and error codes if necessary. Rebooting the system, resetting the hardware, or cycling power on the zBus racks will reset the data in the expanded window.

Rescan Bus

If no device is found when zBUSmon is run, a NO DEVICES FOUND message is displayed in place of a system diagram and the **Rescan Bus** button is displayed. This button can be used to scan for devices that have been connected or turned on after zBUSmon was launched.

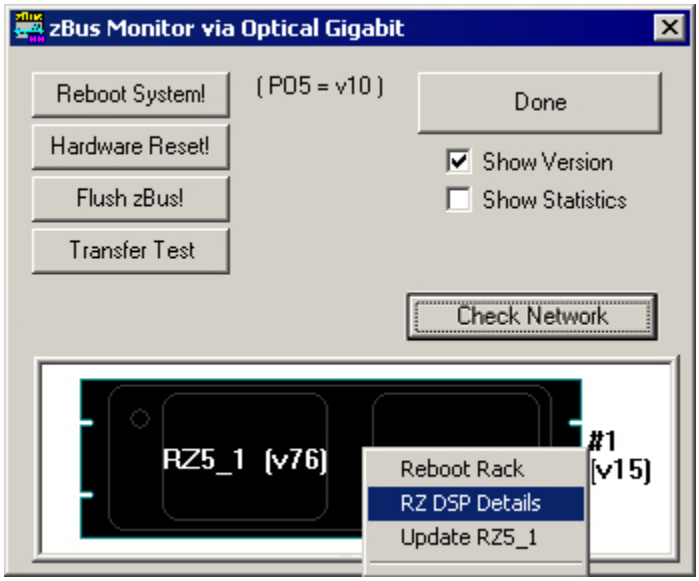


Viewing Microcode Version for all DSPs on an RZ DSP Device

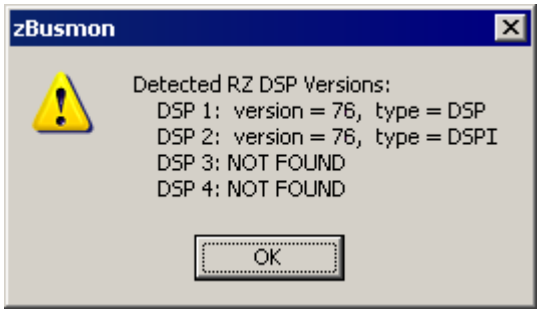
If a device has more than one DSP, the system diagram displays the number of DSPs and the microcode version for the first DSP.

To confirm the microcode version for each DSP:

1. Right-click the device in the diagram.



2. Click **RZ DSP Details** on the shortcut menu.



   The zBUSmon DSP version list is displayed including the type of DSP (DSP for regular DSPs; DSPI, DSPP, DSPS, or DSPV for optical DSPs).

   Note: Only optical DSPs built or reprogrammed by TDT after 12/18/12 will display the correct DSP type.

3. Click **OK** to close the pop-up window.

Updating the Microcode

Programmable devices use low-level software called microcode that resides in their flash memory. The microcode contains low-level hardware instructions. The microcode for processor devices contains the DSP instructions for the RPvdsEx processing components. Because the System 3 design allows users to update this software quickly and efficiently, users can take advantage of the latest software tools available without purchasing new equipment or sending devices to our manufacturing facility for upgrades.

When you install TDT Drivers, microcode with a matching version number is stored in .dxe files on the PC. The zBUSmon utility uses these files to update or reprogram processor devices in the system. The current microcode version number for each device is displayed in the utility's system diagram. For processor devices, the version number shown should be the same as the version number of the TDT Drivers installed on the PC (Note: this does not apply to the PA5, which is fixed at v30).

If any device (or any RZ DSP) is programmed with microcode that doesn't match the currently installed release, the microcode version number will appear in red and the 'Update All Devices' button will also appear below the 'Transfer Test' button. Devices with outdated Microcode versions should be updated immediately.

The **zBUSmon Utility** can be used to update the microcode on one or more devices. There are three options for updating:

- The **Update All Devices** button automates the process of updating all devices in a system.
- The **Update {device name}** command automates the process of updating a specified device.
- The **Program {device name}** command allows the user to select the microcode file when specifying a device to program.

Updating All Devices in a System

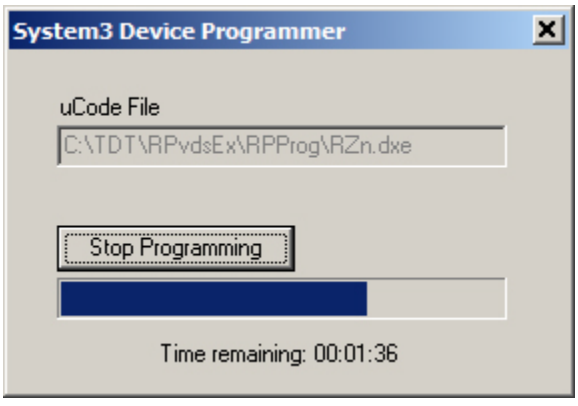
Note: For instructions on updating an RL2 contact TDT Support.

To quickly update all devices in the system:

1. In the zBUSmon utility window, click the **Update All Devices** button.

   A time warning will be displayed. Most processors can be programmed in four minutes; however, the RZ processors may take up to 40 minutes (five minutes per DSP). If your system contains several devices this process could take significant time.

2. Click **Yes** to continue.



The System3 Device Programmer window is opened and programming automatically begins. Devices are programmed sequentially. A bar at the bottom of the window indicates progress for each device as it is updated.

Note: The PC should not be used for other tasks while devices are being reprogrammed.

If the automatic update process detects an **RX device**, a message will be displayed. Press and hold the **Mode** button on the front panel of the RX device and then click **Retry**. Release the **Mode** button when the front panel of the RX device displays **Firmware: BLANK** or **Firmware: Burning**.

If there are multiple RX processors in the system, they will be programmed in the order in which they are connected in the system. To determine the order, check the device index numbers in the zBUSmon system diagram.

The **Stop Programming** button will halt programming, but the device will need to be programmed before it can be used. It may show up as a G21K device if programming is interrupted prematurely, in which case you will have to manually program it. See Programming a Single Device Manually below.

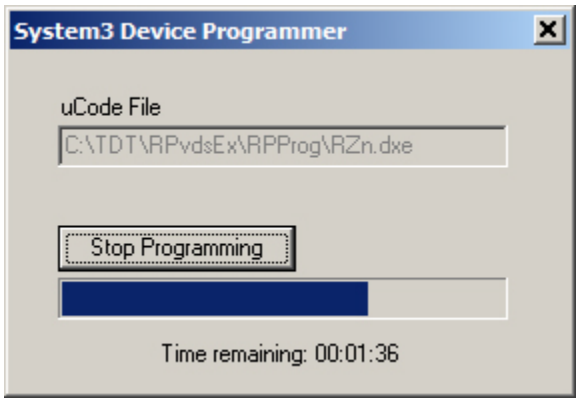
3. The dialog will close when programming has completed.

Updating a Single Device Automatically

To automatically update a single device:

1. For all devices except RX-Series Processors, right-click the device in the system diagram, then click **Update {device name}** on the shortcut menu. If a time warning is displayed, after reading the message click **Yes** to continue.

   For **RX-Series Processors only**, press and hold the **Mode** button on the front panel of the device, right-click the device in the system diagram, then click **Update {device name}** on the shortcut menu. When **Firmware: BLANK** or **Firmware: Burning** is displayed on the front panel of the device, release the **Mode** button.



   The System3 Device Programmer window is opened and programming automatically begins. A bar at the bottom of the window indicates progress.

   Note: The PC should not be used for other tasks while devices are being reprogrammed.

   The **Stop Programming** button will halt programming, but the device will need to be programmed before it can be used.

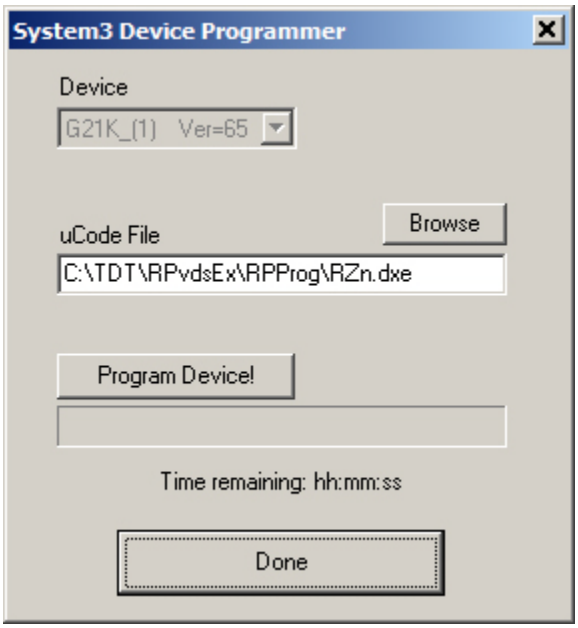
2. The dialog will close when programming has completed.

Programming a Single Device Manually

To manually program a device:

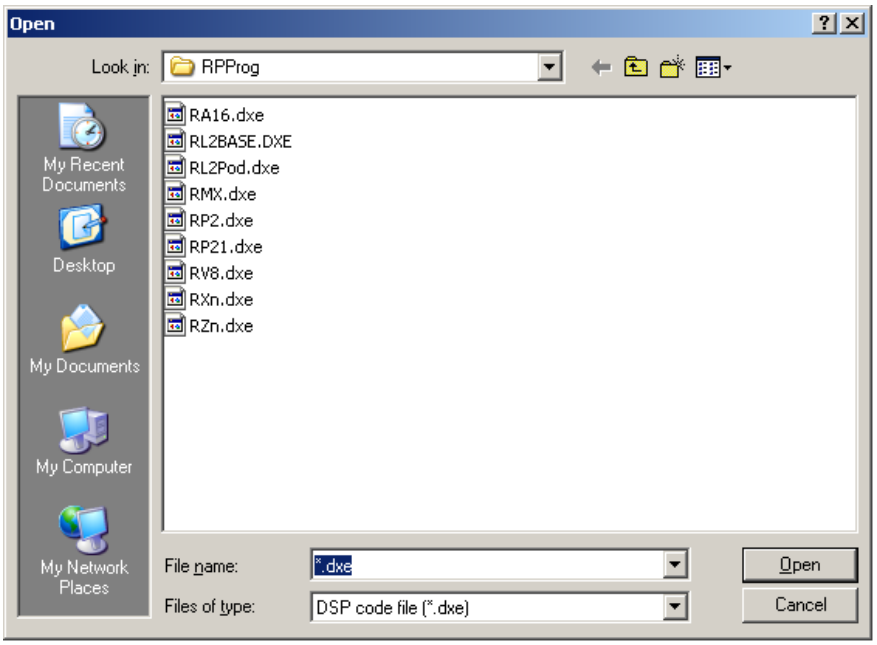
1. In the **zBUSmon** utility window, hold down the shift key and right-click the device in the system diagram.

2. Click **Program {device name}** on the shortcut menu.



The System3 Device Programmer window is opened. In this window you can choose the desired microcode file.

3. Next to **uCode File**, click the **Browse** button.



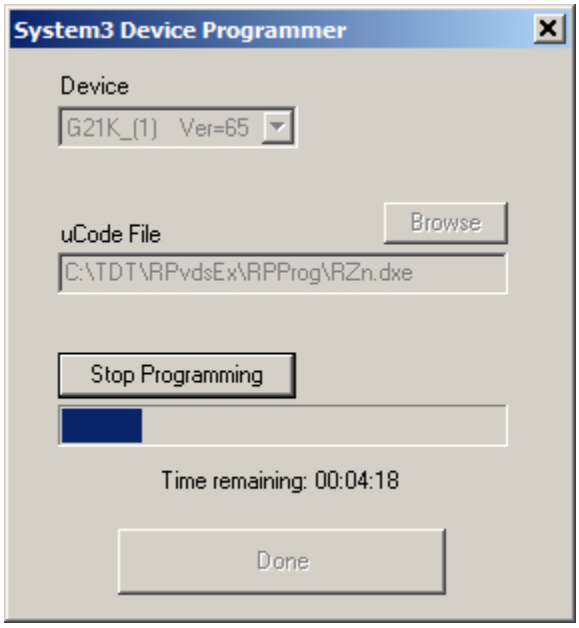
The default location for .dxe files is opened and you can select the desired file for the selected device or browse to an alternate location. The available files should include:

File	Device
RP2.dxe	RP2 Real-Time Processor
RP21.dxe	RP2.1 Enhanced Real-Time Processor
RA16.dxe	RA16BA Medusa Base Station
RV8.dxe	RV8 Barracuda Processor
RMX.dxe	RM1/RM2 Mobile Processors
RXn.dxe	RX Processors
RZn.dxe	RZ Z-Series Processors

4. Once you have selected the desired file, click **Open**. The Open window is closed and the selected file appears in the **uCode File** box.

5. For all devices except RX-Series Processors, click **Program Device!**. For **RX-Series Processors only**, press and hold the **Mode** button on the front panel of the device then click **Program Device!**. When **Firmware: BLANK** or **Firmware: Burning** is displayed on the front panel of the device, release the **Mode** button.

   Programming begins and the progress bar displays the estimated time to complete the task.



   Note: The PC should not be used for other tasks while devices are being reprogrammed.

   The **Stop Programming** button will halt programming, but the device will need to be programmed before it can be used.

6. When the Device Programmed message is displayed, click **OK**.

Corpus System 3 Hardware Emulator

Corpus is a software program that runs on any Windows PC. The Corpus program provides robust and seamless emulation of TDT's System 3 hardware via the standard driver interface. Corpus allows users to run any TDT or user program that relies on System 3 hardware without the physical hardware connected.

The Corpus version is synchronized with the TDT driver package releases. Corpus is available in TDT Drivers v86 and above. Corpus is free to all TDT customers and is automatically installed with TDT Drivers.

Hardware Emulation and PC Processor Capacity

Corpus operates via the same driver interface used to control standard TDT System 3 hardware. If the Corpus program is running when a program attempts to connect to System 3 hardware, the interface will be redirected to the software emulator and any connected hardware will not be accessed.

For Synapse users, Corpus will emulate the hardware configuration specified in the Rig Editor. The *.synrig file that contains the Rig Editor configuration can be found here: C:\Users\{username}\AppData\Local\Tucker-Davis Technologies\Synapse\.

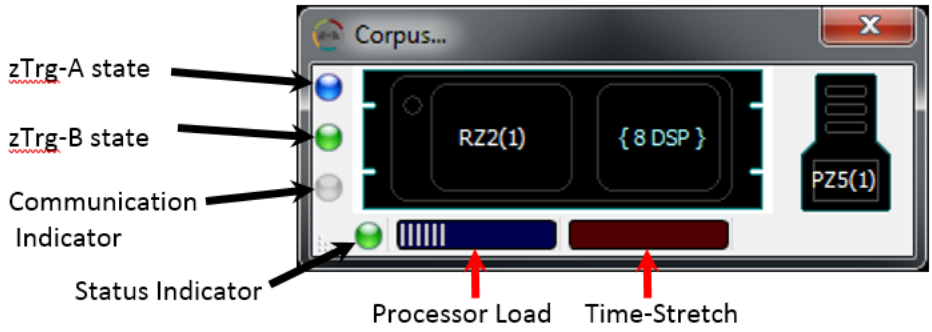
For non-Synapse users, if this file is not found the rig file located at C:\TDT\Corpus\Corpus.synrig file will be loaded. The default file will emulate a PZ5-32 connected to an RZ2 equipped with 8 standard DSPs.

Corpus emulation capabilities are dependent on the processing power of a user's PC. The emulator will automatically assign cores and threads to realize optimal performance on a given platform. Corpus can be used efficiently on almost any machine, from laptops to high-end desktops, without being limited to the type of TDT hardware being emulated.

The core usage on a user's computer is not one-to-one with the emulation of standard RZDSPs. Indeed, Corpus would allocate the same resources if it was emulating one DSP or eight quad DSPs (QZDSPs).

Corpus can simulate hardware function in "pseudo" real-time. The emulator will block process chunks of discrete time samples, as would real hardware. Thus, if something does not work in Corpus, it likely will not work using real hardware. Unlike real hardware, however, Corpus will slow down processing and stretch time as its processing limits are exceeded. Status indicators, as shown in the Corpus window below, give feedback on processor load and speed, as well as other mode and error indicators.

The Corpus Window



Corpus Main Window

The System 3 devices that are supported by Corpus are listed below.

Device Name	Corpus Emulation Support
RZ2/RZ5x	Fully supported, but some hardware features not simulated or emulated
RZ6	Fully supported, excluding audio features
PZn	Can generate simulated neural signals, but not all device features fully emulated
UDP	Fully simulated, packets will be sent and received via host computer's Ethernet port
RS4/PO8e	Device is recognized but cannot be emulated
IZ2	Device is recognized but cannot be emulated
RV2	Device is recognized but cannot be emulated
RXn	Device is not supported by Corpus
RP2.1	Device is not supported by Corpus
RA16BA	Device is not supported by Corpus

Most DSP components have been implemented, however some components are either not appropriate for emulation or are not yet supported. If an unsupported RPvdsEx component is detected, the Status Indicator will turn red. Clicking on the indicator will show a debug window that lists the offending component(s).

Inputting Fake Data

Corpus allows you to load data files onto the emulated hardware and play them out, sample for sample, as if they can in on the actual hardware inputs.

A complete list of accepted file extensions and their associated hardware devices is shown in table 2.

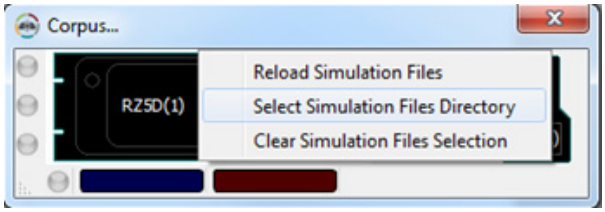
Hardware	Component	File Prefix	File Extension
RZn	ADC	adc	mat, wav
RZn	ADC	adcN	mat, wav, f32, i32, i16, txt
RZn	Digital I/O	Bits	mat, wav, f32, i32, i16, txt
PZn	PZ	chan	mat
PZn	PZ	chanN	mat, f32, txt

The scale factor for each data type is uniquely dependent on the hardware device being emulated. A table of scale factors for each type of hardware and device is shown below.

File Type	Hardware	Scale
mat	RZn	1e-1
	PZn	PZ5: 1e9/4 Other PZn devices: 1e9
wav	RZn	1e-1
	PZn	N/A
f32	RZn	1e-1
	PZn	PZ5: 1e9/4 Other PZn devices: 1e9
i32	RZn	ADC: (2^31)/10, DIO: 1 (bits), 2^16 (words)
	PZn	N/A
i16	RZn	ADC: (2^15)/10, DIO: 1 (bits), 2^8 (words)
	PZn	N/A
txt	RZn	1e-1
	PZn	PZ5: 1e9/4 Other PZn devices: 1e9

For certain file prefixes, the user may, and sometimes must, specify the specific channel N that the data will be loaded on. For example, *.f32 files must have a specified channel onto which they are loaded onto an RZ device. Thus, the file must be named "adc1.f32" if the user wishes to load the data into channel 1 of an RZn ADC port.

To load fake data files, the user must direct corpus to an appropriate directory that contains the intended hardware device and the files to the simulated on that device. The folder tree should be formatted as C:\TDT\Corpus\SimulationFiles\<experiment>\<hardware_device_name>. The user can load the appropriate directory by right-clicking in Corpus and choosing "Select Simulation Files Directory," and browsing to the highest folder in the desired directory (typically the <experiment> folder). A new window should appear when corpus is loading and completes loading the data.



The maximum files size for loading simulation data into Corpus is 256 million samples. If a user's file is too large, Corpus will not load any of the data and instead provide a message in the loading dialog box.

Learn More About Corpus

TDT support offers a suit of Synapse-based instructional videos, which includes one dedicated to Corpus, on their website found here: https://www.tdt.com/training-videos/

Part 23: Computer Workstation

WS4/WS8 High Performance Computer Workstation

Workstation Includes Keyboard and Mouse - Not Pictured

WS Overview

The TDT WS computer workstations are rack-mountable and purpose-built for research applications, experiment control and data analysis. Each WS is equipped with a TDT Optibit interface and 240 GB Solid State Drive (SSD) with preinstalled TDT software, and 64-bit Windows 10®.

The WS also includes at least one 1 TB hard drive. The drives are removable from the front panel. Additional storage drives are available from TDT.

The WS is available in two configurations. The WS-8 is optimized for the most demanding applications, including high-channel count neurophysiology. The WS-4 is targeted for less demanding applications, such as ABR and DPOAE testing with BioSigRZ software. Both form factors include two Gigabit Ethernet network ports for integration with existing lab infrastructure or external device support.

Power and Interface

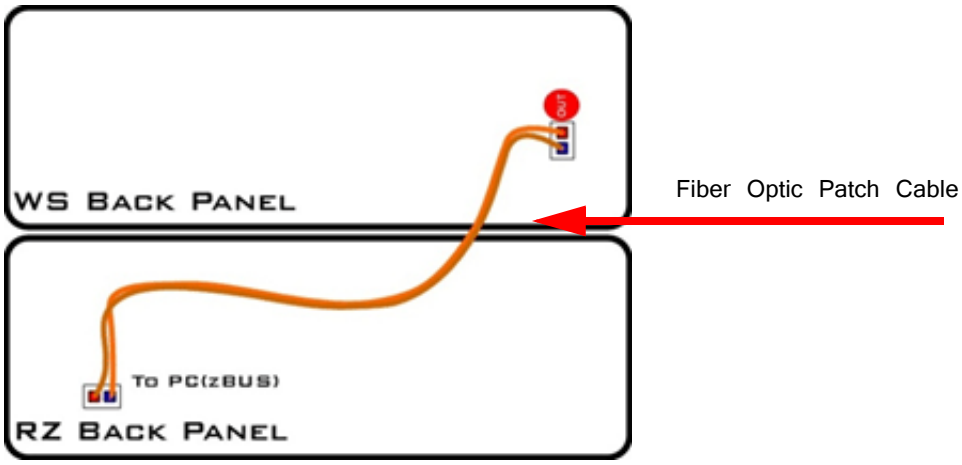
The WS comes factory installed with an Optibit optical interface card.

The power supply is auto-switching for 110 V or 220 V. A soft on/off button is provided on the front panel and a hard power cutoff switch is provided on the back panel.

WS Hardware Setup

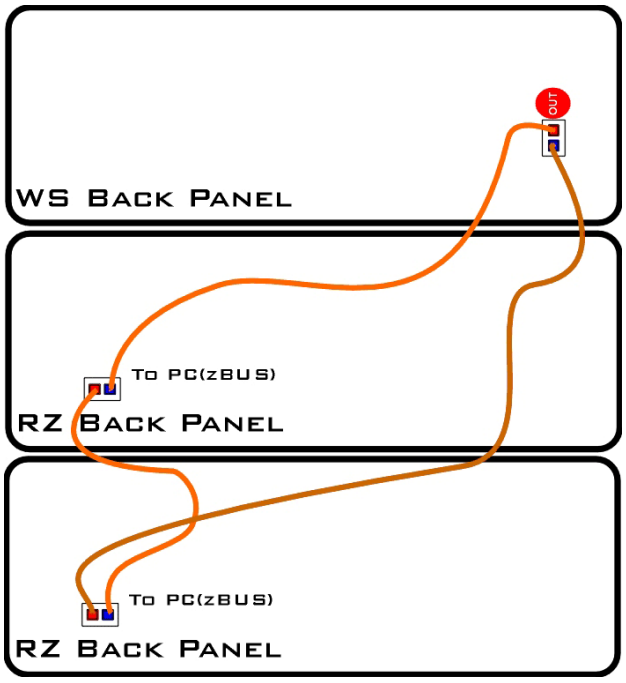
Use the provided duplex fiber optic patch cables (orange) to connect the WS's factory installed, Optibit optical interface card to a TDT processor device. The fiber

optic ports on each device and the patch cables are color-coded and use key and notch connectors to ensure correct wiring.

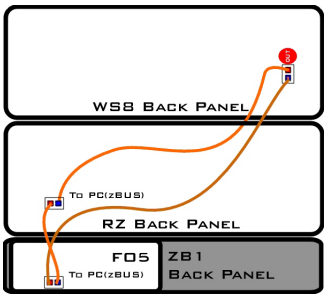


Connecting Multiple Devices

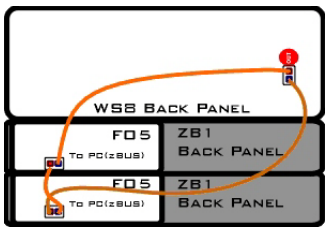
Multiple processors (or other interface-dependent devices mounted in a zBus chassis) can be connected to the WS's Optibit interface in a communications loop. The most common configuration consists of multiple RZ devices, such as multiple RZ2s used for processing higher-channel counts. The strands of the duplex cable can be separated as needed to make the required connections. See the diagrams below for additional configurations.



Multiple RZ Processors



Mixed RZ and RX or RP Processors



Multiple ZB1 Mounted Devices (RX, RP, PA5)

WS Features

LED Display

The LED display provides visual representation of system performance. The display includes 12 angled lines of LEDs representing percentage of performance capacity in use, from 0 – 100%, for each system element. Lines are labeled for quick identification and include indicators for the system elements listed below.

NET-A	Ethernet Port A
NET-B	Ethernet Port B
1-4	Processor Threads 1 – 4
5-8	Processor Threads 5 – 8 (WS-8 only)
HDD	System Hard Drive
MEM	RAM Usage

System Hard Drive (C:)

The system hard drive is pre-loaded with Windows 10® and TDT Software. It is labeled as the C: drive and is accessible from the front panel. This is a removable drive, but must be in place for system operation. A blue LED indicates connection and a purple LED indicates when the drive is being accessed.

Data (D: & E:)

The WS supports up to two removable data drives for storage of experiment data. The drives slots are accessible from the front panel and are labeled D: and E:. The standard system ships with one storage drive and additional drives may be purchased separately. A blue LED indicates connection and a purple LED indicates when the drive is being accessed.

To remove/insert drives:

1. Turn off the WS.
2. Press upward on the silver button near the bottom of the drive door then lift the door up to open.
3. Pull the drive out or push it into place.
4. Close the drive door, pressing firmly until it snaps into place.

CAUTION! Do not remove or insert drives while the WS is running.

USB Ports

WS serial number 2000 and above include one front panel USB 3.0 port, six USB 3.0 ports on the back, and two USB 2.0 ports on the back.

WS serial number < 2000 include one front panel USB 2.0 port and four USB 3.0 ports on the back. See the Connector Panel diagram below for port location. Two USB extension cables are included so keyboard and mouse can be away from the WS.

Video Support

The WS-8 and WS-4 each include a high-performance video card. The WS-8 card supports up to two monitors, with a 'primary' port that must always be used and a second port to be used for a second monitor. One or two DVI cables are provided.

Important! Standard video connections are disabled when the video card is in use.

Input/Output Connections

The WS includes standard connections for keyboard, mouse, and audio input/output lines. Two Gigabit Ethernet ports and an RS232 type serial port are also provided.

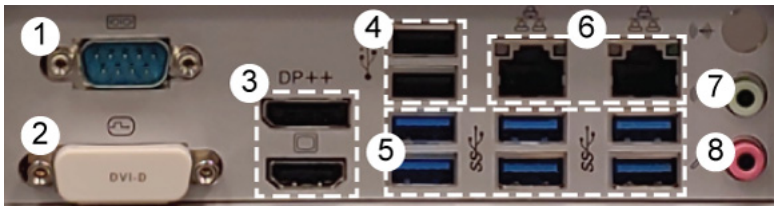
Back Panel Connections

WS serial number 2000 and above

1. AC Power Cord Input
2. On/Off Switch
3. Connector Panel (see below)
4. Video Card with Dual(WS8 only) Link DVIs and HDMI-mini
   a. Primary Video Connection
   b. Secondary Video Connection
5. PO5e Optical Port
6. Unavailable
7. Open PCIe x4, Half-Length Slot

Note: The provided keyboard and mouse connect via USB ports.

Connector Panel



1. Serial (RS232) port
2. DVI-D *
3. Display Port / HDMI *
4. USB 2.0
5. USB 3.0
6. Gigabit Ethernet
7. Audio Line Out
8. Mic In

***Note:** 2 and 3 are disabled when using the video card.

WS-8 Technical Specifications

CPU	s/n > 2000: 4.0 GHz Intel® Core™ i7-6700K (4 SMT Cores for 8 processor threads running at 4.0 GHz in parallel) s/n < 2000: 3.4 GHz Intel® Core™ i7 (4 SMT Cores for 8 processor threads running at 3.4 GHz in parallel)
Memory	8 GB DDR3 SDRAM
Video Card	s/n > 2000: GeForce GTX 1050Ti with 4 GB GDDR5 s/n < 2000: GeForce GTX 650 with 2 GB RAM
OS Hard Drive	240 GB Solid State Drive (SSD)
Data Storage	s/n > 2000: 1 TB SSD, removable(1 included) s/n < 2000: 1 TB HDD, 7200RPM, removable (1 included)
Network	Two Gigabit Ethernet ports
TDT Interface	s/n > 2000: PO5e card s/n < 2000: P05 card
Open Slot	PCIe x4, half-length
Keyboard	Das Keyboard Model S Professional Click Pressure Point Mechanical Keyboard with two port USB hub
Mouse	Mad Catz R.A.T.3 Optical Gaming Mouse
Operating System	64-bit Windows 10®
Software	TDT Drivers, RPvdsEx, and other TDT software as requested

WS-4 Technical Specifications

CPU	s/n > 2000: 3.5 GHz Intel® Core™ i5-6600K s/n < 2000: 3.4 GHz Intel® Core™ i5-3570
Memory	4 GB DDR3 DRAM
Video Card	s/n > 2000: GeForce GT 1030 with 2 GB RAM s/n < 2000: GeForce GT 730 with 2 GB RAM
OS Hard Drive	240 GB Solid State Drive (SSD)
Data Storage	s/n > 2000: 1 TB SSD, removable (1 included) s/n < 2000: 1 TB HDD, 7200RPM removable (1 included)
Network	Two Gigabit Ethernet ports
TDT Interface	s/n > 2000: PO5e card s/n < 2000: P05 card
Open Slot	PCIe x4, half-length
Keyboard/Mouse	Microsoft USB Keyboard and Mouse
Operating System	64-bit Windows 10®
Software	TDT Drivers, RPvdsEx, and other TDT software as requested