I/O Delays

Sample Delays for TDT System 3 Hardware I/O

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I/O Delays

Every signal path through a TDT system carries a small, fixed delay. Part of that delay comes from the software processing chain and part of it comes from the analog and digital I/O of the hardware itself. Most experiments never need to account for these delays, but they matter for processing paths that include many gizmos or components, for custom user gizmos, and anywhere timing is critical.

Where the Delays Come From

	Delay Source	Where to Look
Software	The processing chain you build	Synapse for gizmo delays, or RPvdsEx and OpenEx for component delays
Hardware	The I/O of the device itself	Device Delays for ADC, DAC, and amplifier delays

Hardware delays are a property of the device, so the Device Delays tables apply no matter which software you use to build your processing chain.

Synchronizing Processing

When synchronized processing is required, outputs or inputs can be synchronized using delay components provided in RPvdsEx. See Delay Functions in the Component Reference section of the RPvdsEx Manual for more information.

Synapse users can also synchronize outputs or inputs with User Gizmos. See Creating User Gizmos in the Synapse Manual.

Quick Reference

I/O	Delay
Digital Input	2 samples
Digital Output	3 samples
Gizmo Connections (Synapse)	2 samples
RZ2 Data Pipe	2 samples
Inter-DSP zHop Pairs	2 samples
Analog Input (ADC)	Device specific
Analog Output (DAC)	Device specific
Amplifier	Device specific

I/O Delays in Synapse

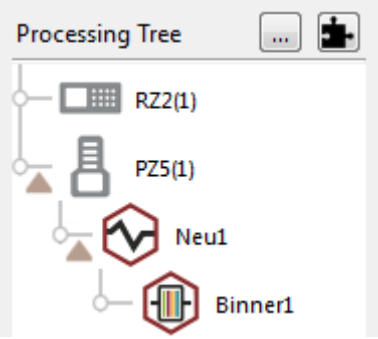
There are two types of delays Synapse users should be aware of: gizmo delays and fixed sample delays associated with the I/O of their hardware devices. When synchronized processing is required, Synapse users can synchronize outputs or inputs using User Gizmos and delay components provided in RPvdsEx. See Creating User Gizmos in the Synapse Manual and Delay Functions in the Component Reference section of the RPvdsEx Manual for more information.

Delay Source	Delay
Gizmo Connections	2 samples
Digital Input	2 samples
Digital Output	3 samples
ADC Delays	Device specific*
DAC Delays	Device specific*

* See Device Delays for hardware specific delays.

Gizmo Delays

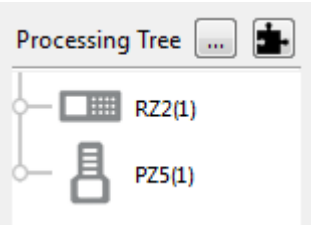
Each branch in the Synapse Processing Tree represents a signal flow or processing path. Each link in a branch adds exactly **two samples** of delay to that path. The path pictured below, from the PZ5 to the Binner, will have a four sample delay. You'll need to be aware of these small delays for experiments with complex processing paths that include many gizmos, custom user gizmos, or where timing is critical.



2 + 2 = 4 sample gizmo delays

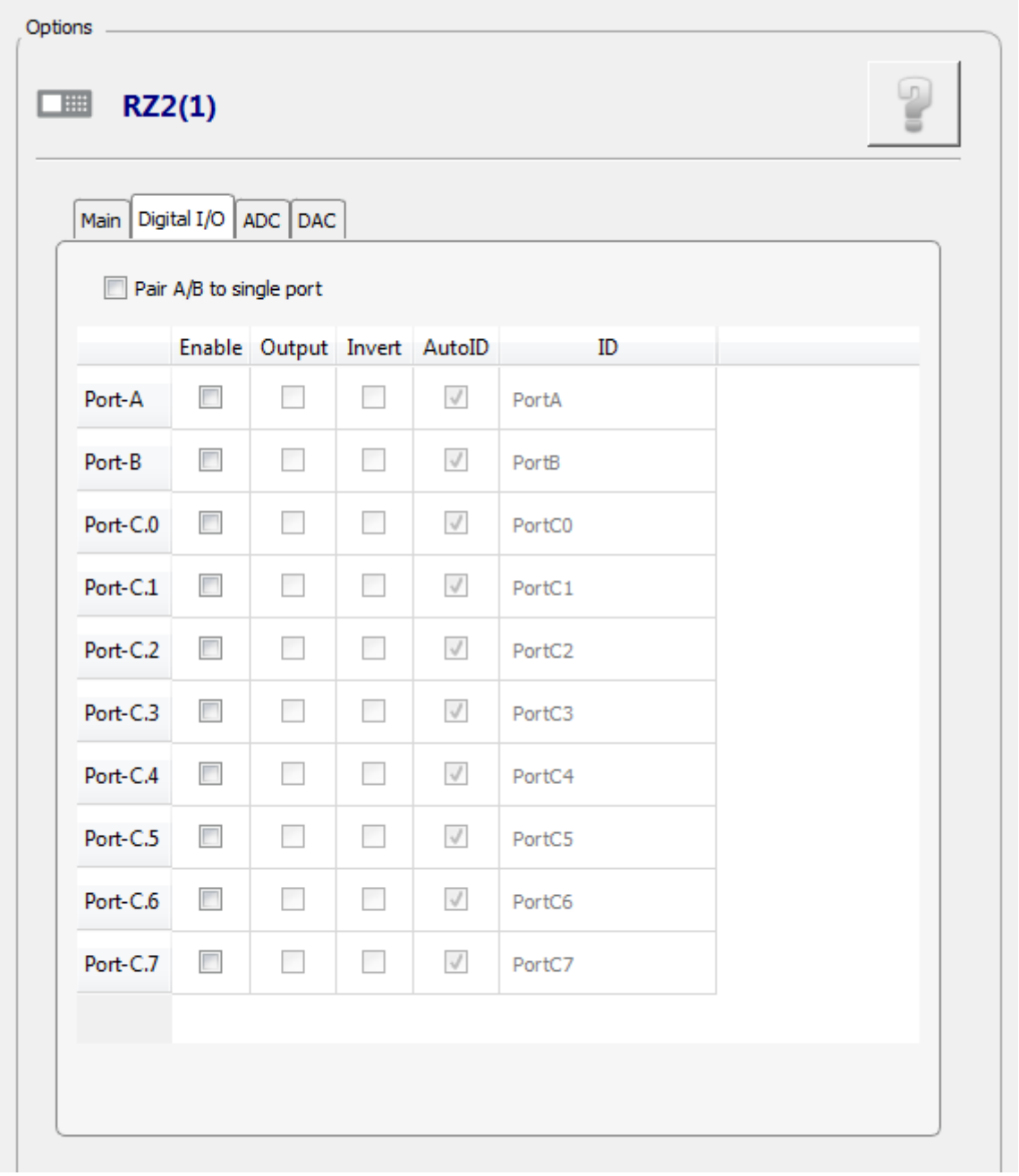
Hardware Delays

In Synapse, I/O for your processor is configured in the hardware HAL. These settings are displayed and arranged on Tabs in the Options area when the device is selected in the Processing Tree.



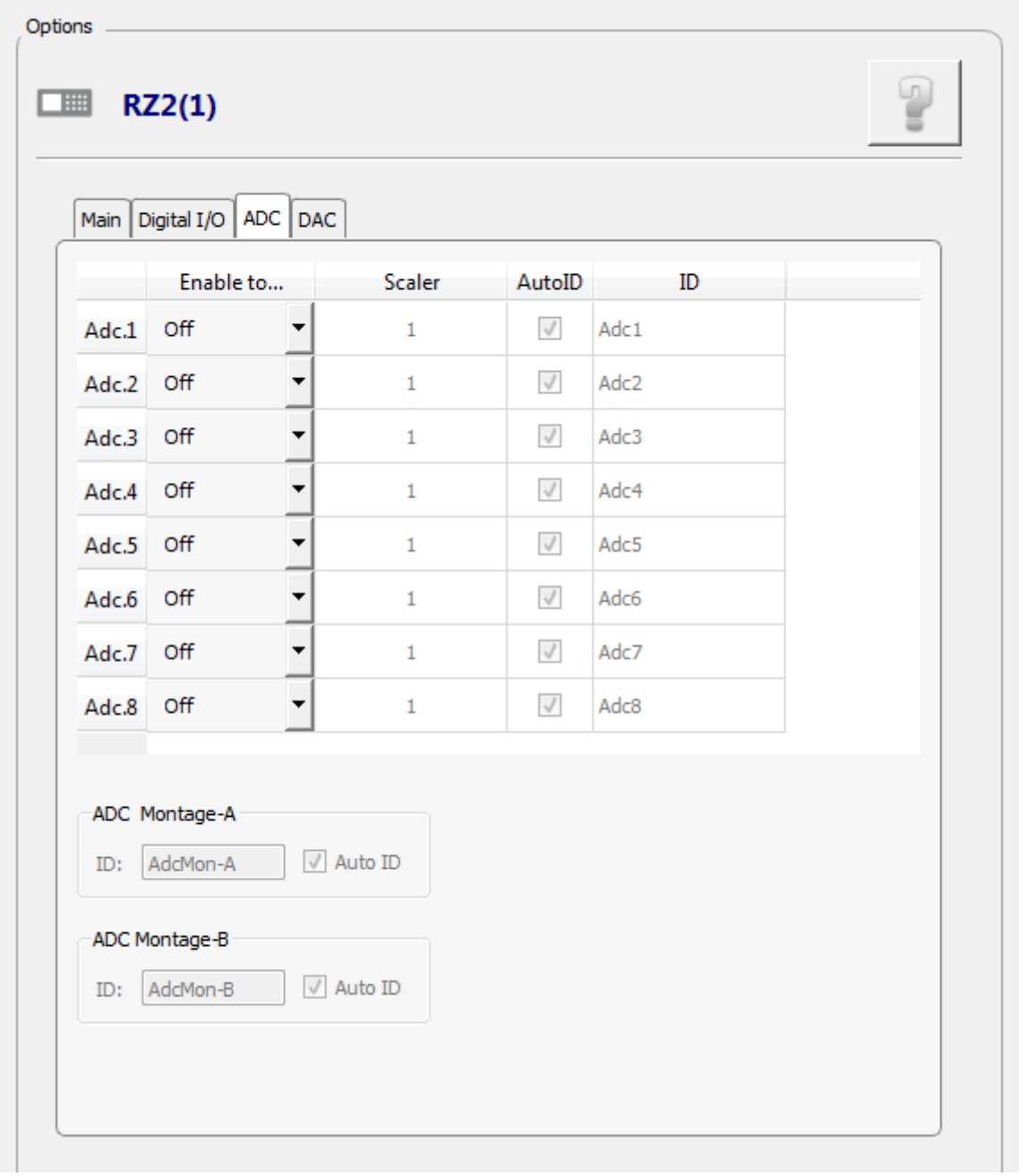
Digital I/O

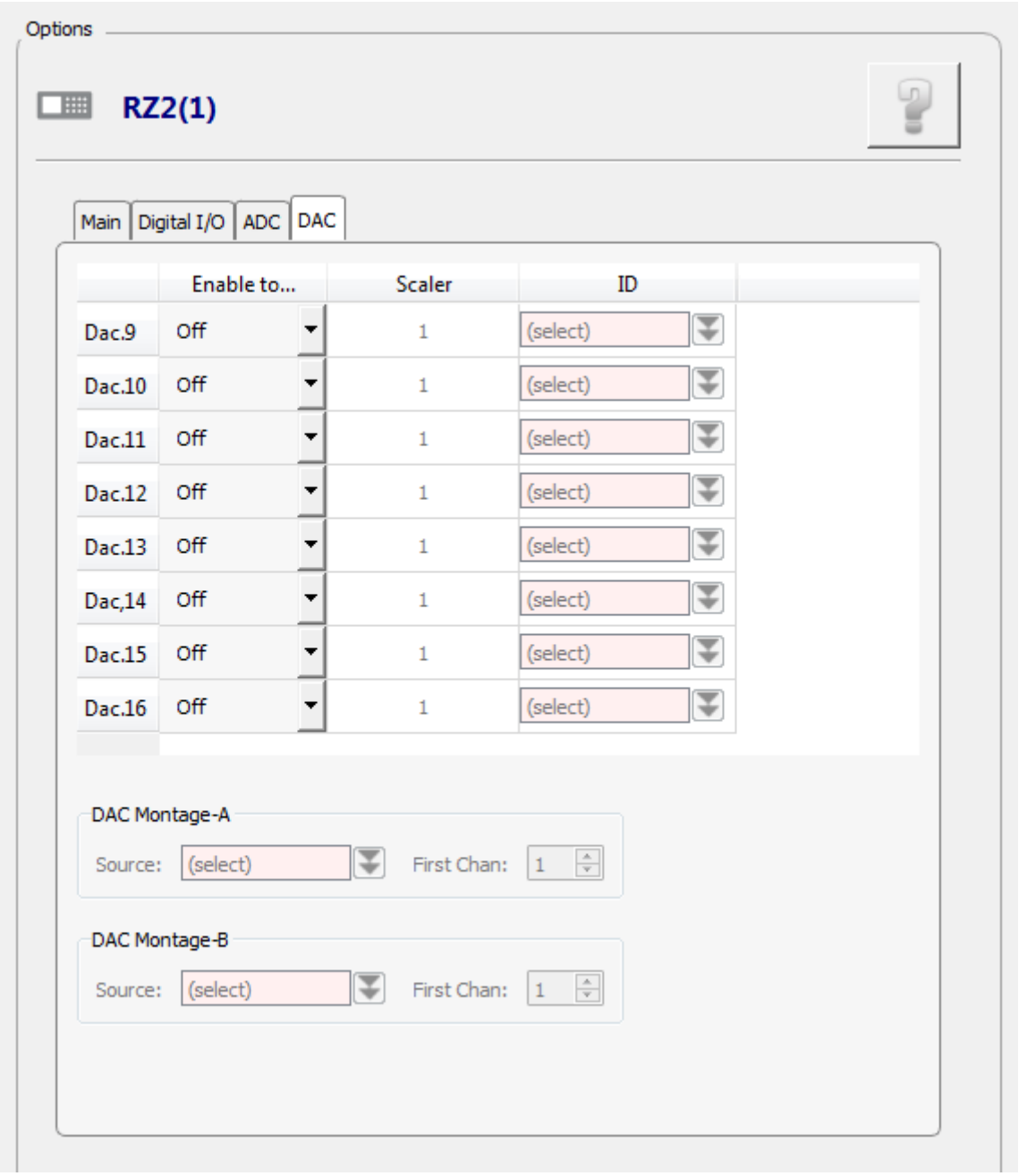
Digital I/O for the processor is configured on the **Digital I/O** tab. Digital inputs add **2 samples** of delay and digital outputs add **3 samples**.



ADC and DAC

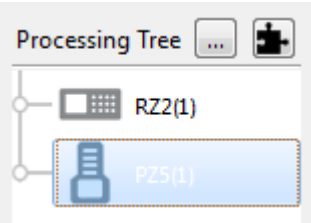
ADC and DAC delays are specific to the type of analog-to-digital and digital-to-analog converters used in the device. See Device Delays for hardware specific delays.



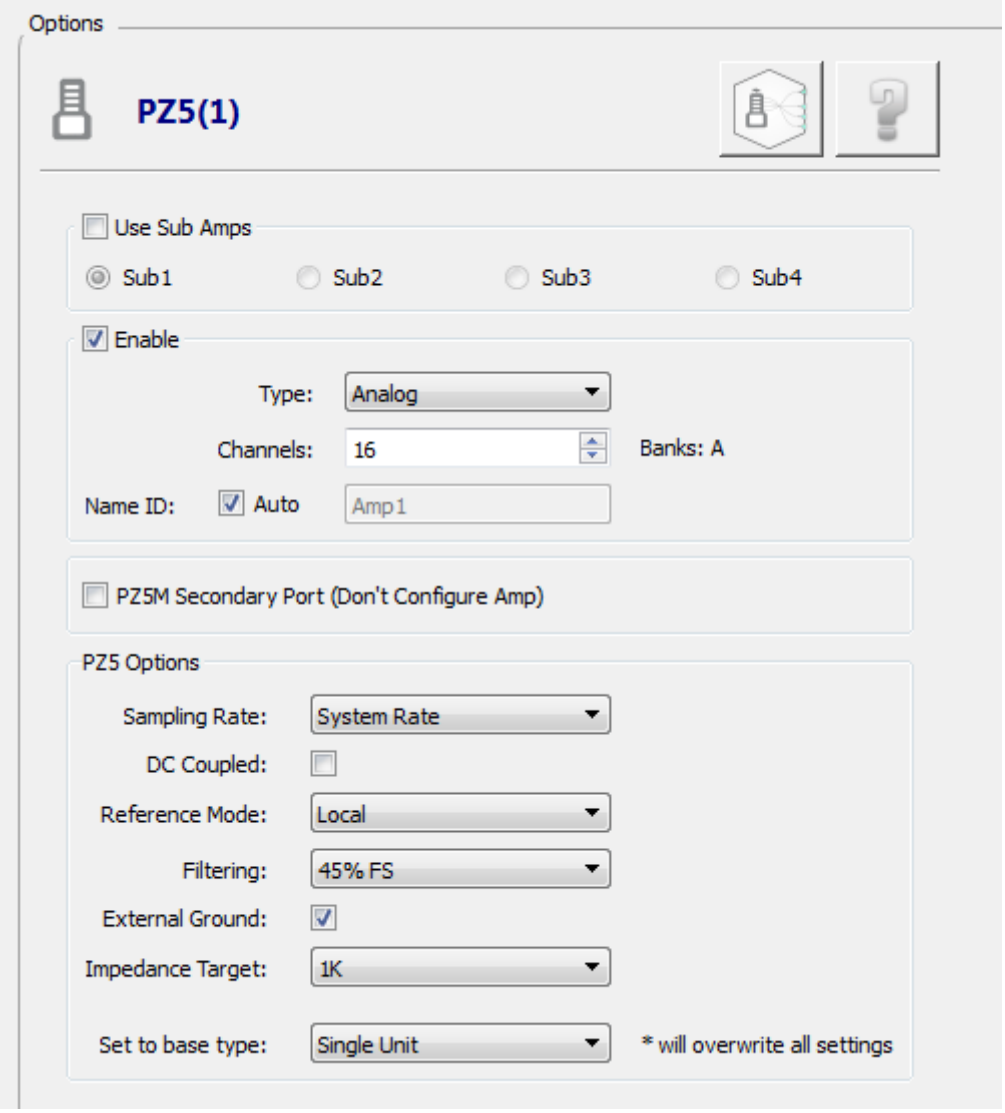


Amplifier Delays

Amplifier delays depend on a variety of factors including: the type of ADC converters, sampling rate, and system architecture. The amplifier's configuration options are displayed when the device is selected in the Processing Tree. The PZ5 HAL (pictured below) can be used to set an amplifier sampling rate or to follow the sampling rate of the RZ processor it is connected to (by selecting **System Rate**).



Amplifier delay varies



See Amplifier Delays for the delays associated with each amplifier.

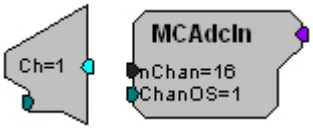
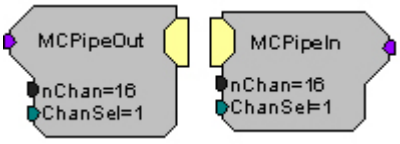
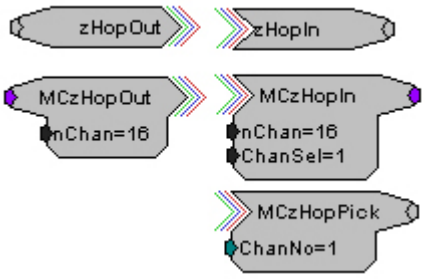
I/O Delays in RPvdsEx and OpenEx

When synchronizing processing circuits users should be aware of delays associated with the I/O of their hardware devices.

Users can synchronize outputs using delay components provided in RPvdsEx. See Delay Functions in the Component Reference section of the RPvdsEx Manual for more information.

I/O Component Delays

The table below provides a comparison of the delays associated with types of I/O and components.

I/O Type	Component	Delay	Component Icons
Digital Input	BitIn WordIn	2 samples	
Digital Output	BitOut WordOut	3 samples	
Analog Input	AdcIn MCAdcIn	device specific*	
Analog Output	DacOut	device specific*	
RZ2 Data Pipe	MCPipeOut/In	2 samples	 *Requires PipeSource Component*
Inter-DSP zHop Pairs	zHopOut/In MCzHopOut/In MCzHopPick	2 samples	

* See Device Delays for hardware specific delays.

For the bitmasks used to address byte and bit addressable digital I/O with the WordIn, WordOut, BitIn and BitOut components, see RZ Processor Digital I/O.

Device Delays

ADC and DAC delays are specific to the type of analog-to-digital and digital-to-analog converters used in the device. These delays are a property of the hardware, so they apply whether the processing chain is built in Synapse or in RPvdsEx and OpenEx.

DAC and ADC Processor Delays

The table below lists devices along with their associated DAC and ADC delays.

Device	SD DAC	SD ADC	PCM DAC	PCM ADC
RZ2, RZ5, RZ5D, RZ5P, IZ2	NA	NA	4 samples	3 samples
RZ6	31 samples	66 samples	NA	NA
RX5, RX7, MS16	NA	NA	4 samples	NA
RX6	43 samples	70 samples	NA	NA
RX8	23 samples	47 samples	4 samples	3 samples
RP2.1	65 samples	30 samples	NA	NA
RA16BA	21 samples	NA	NA	NA

Amplifier Delays

The tables below list amplifiers along with their associated ADC delays.

Amplifier delays depend on a variety of factors including: the type of ADC converters, sampling rate, and system architecture.

PZ5 Hybrid ADC Delays

Dependent on PZ5 and RZ processor sample rates.

PZ5 Rate	RZ at 25 kHz	RZ at 12 kHz
25 kHz	22 samples	x
12 kHz	40 samples	23 samples
6 kHz	76 samples	42 samples
3 kHz	141 samples	79 samples
1.5 kHz	270 samples	152 samples
750 Hz	543 samples	295 samples

Medusa ADC Delays

Device	SD ADC	PCM ADC
RA4PA and RA16PA	NA	3 samples
RA16SD	20 samples	NA

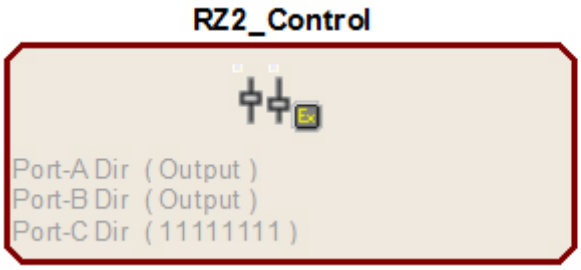
PZ2 and PZ3 Delays

Dependent on RZ processor sample rate.

Rate	Delay
6 kHz	16 samples
12 kHz	17 samples
25 kHz	20 samples
50 kHz	26 samples

RZ Processor Digital I/O

The RZ Processors include 24 bits of programmable digital I/O, two word addressable bytes and eight bit addressible bits. Direction of bytes and bits (in/out) can be set in the corresponding device specific control macro for the device, RZ2_Control, RZ5_Control, RZ5D_Control, RZ6_Control. See below for components/bitmasks to address bytes/bits.

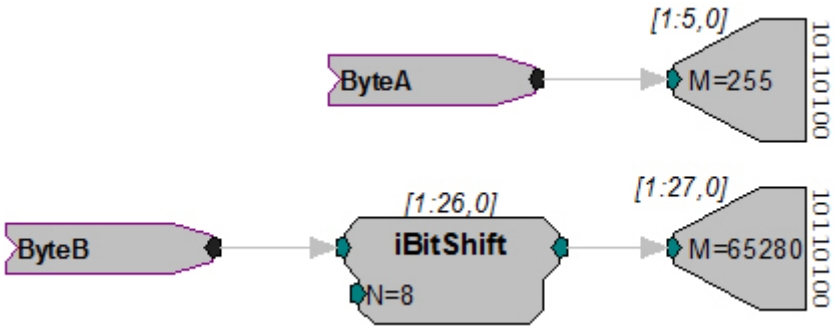


Byte Addressable Digital I/O

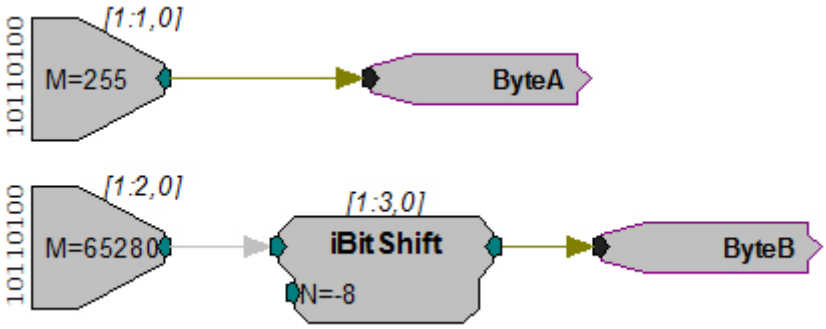
Bitmasks to use for accessing byte addressable digital I/O with the WordIn, WordOut components.

Port	Byte/Bits	Bitmask (Integer)
Port A	Byte A (bits 0 - 7)	M = 255
Port B	Byte B (bits 0 - 7)	M = 65280

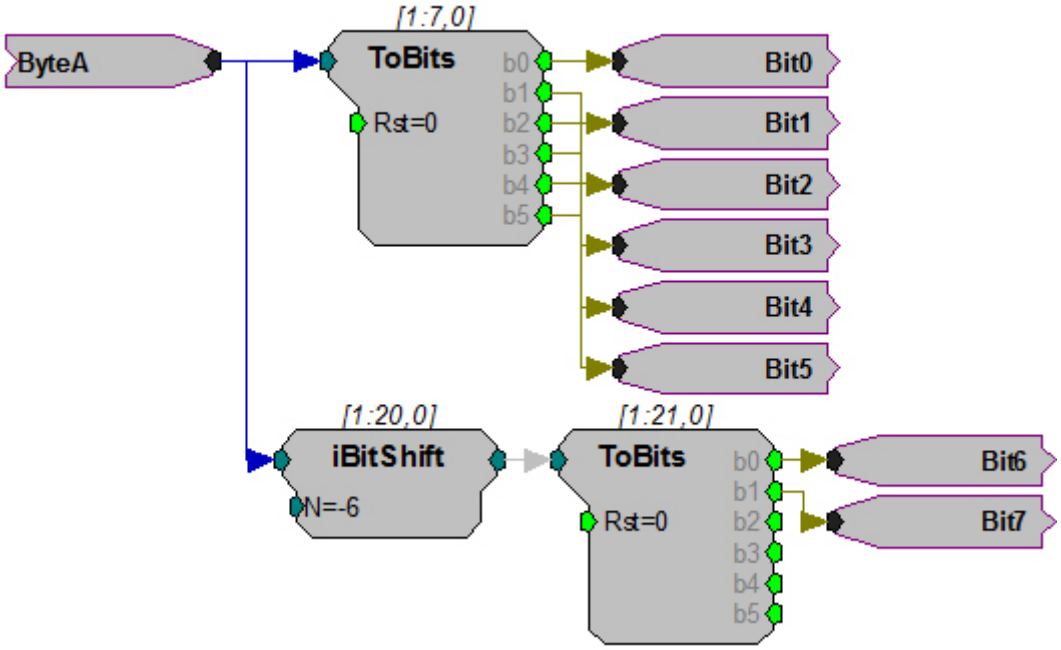
Reading Bytes A and B



Writing to Bytes A and B



Reading Bits from a Byte

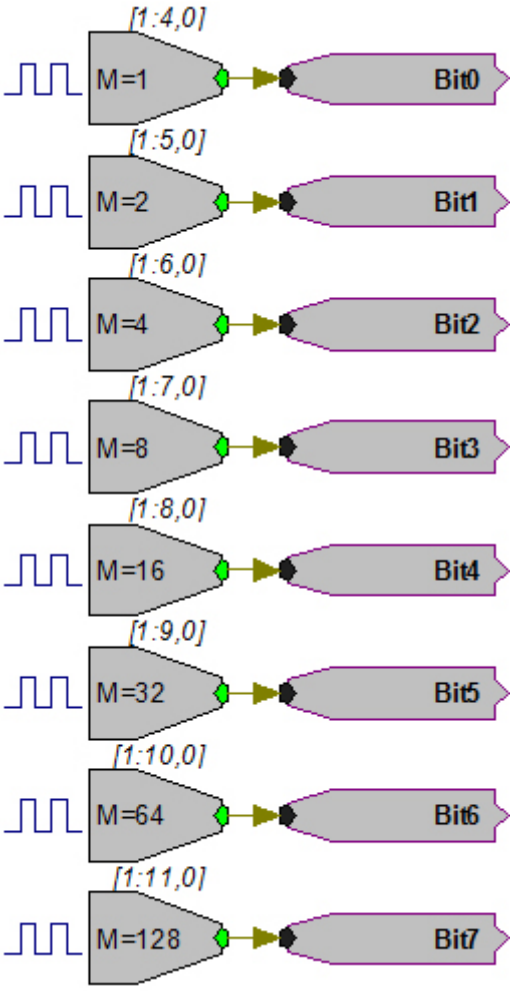
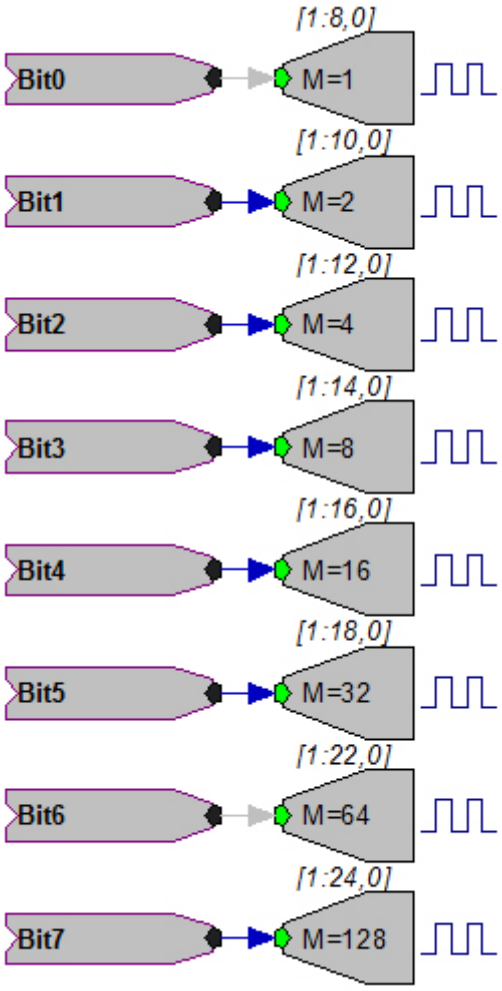


Bit Addressable Digital I/O

Bitmasks to use for accessing bit addressable digital I/O with the BitIn, BitOut components.

Bit	Bitmask (Integer)
0	M = 1
1	M = 2
2	M = 4
3	M = 8
4	M = 16
5	M = 32
6	M = 64
7	M = 128

Port C As Inputs



Port C As Outputs