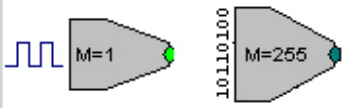
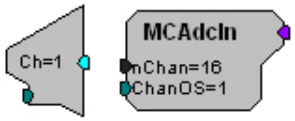
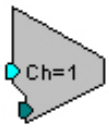
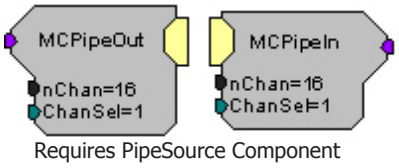
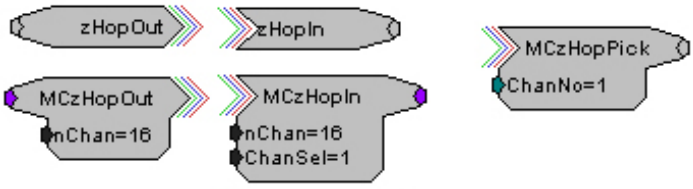
Fast Facts

Input/Output Components

I/O Type	Component	Delay	Component Icons
Digital Input	BitIn WordIn	2 samples	
Digital Output	BitOut WordOut	3 samples	
Analog Input	AdcIn MCAdcIn	device specific*	
Analog Output	DacOut	device specific*	
RZ2 Data Pipe	MCPipeOut/In	2 samples	
Inter-DSP zHop Pairs	zHopOut/In MCzHopOut/In MCzHopPick	2 samples	

DAC and ADC Delays

When synchronizing processing circuits users should be aware of delays associated with the I/O of their hardware devices.

Users can synchronize outputs using delay components provided in RPvdsEx. See Delay Functions in the Component Reference section of the RPvdsEx Manual for more information.

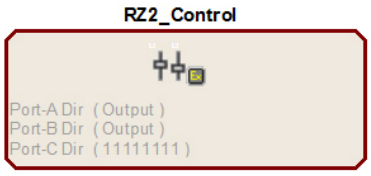
The table to the left provides a comparison of the delays associated with types of I/O and components.

The table below lists devices along with their associated DAC and ADC delays.

Device	SD DAC	SD ADC	PCM DAC	PCM ADC
RZ2, RZ5, RZ5D, IZ2	NA	NA	4 samples	3 samples
RZ6	31 samples	66 samples	NA	NA
RX5, RX7, MS16	NA	NA	4 samples	NA
RX6	43 samples	70 samples	NA	NA
RX8	23 samples	47 samples	4 samples	3 samples
RP2.1	65 samples	30 samples	NA	NA
RA16BA	21 samples	NA	NA	NA
RA16PA	NA	20 samples	NA	3

RZ Processor Digital I/O

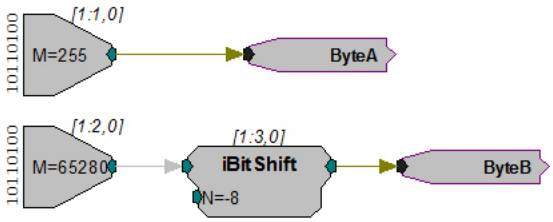
The RZ Processors include 24 bits of programmable digital I/O, two word addressable bytes and eight bit addressible bits. Direction of bytes and bits (in/out) can be set in the corresponding device specific control macro for the device, RZ2_Control, RZ5_Control, RZ5D_Control, RZ6_Control. See below for components/bitmasks to address bytes/bits.



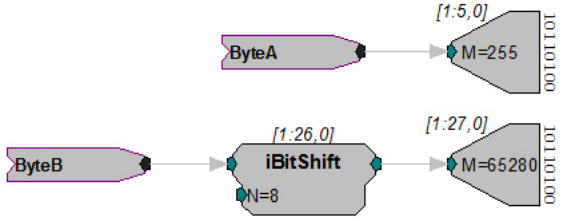
Bitmasks to Use for Accessing Byte Addressable Digital I/O with WordIn, WordOut Components

Port	Byte/Bits	Bitmask (Integer)
Port A	Byte A (bits 0 - 7)	M = 255
Port B	Byte B (bits 0 - 7)	M = 65280

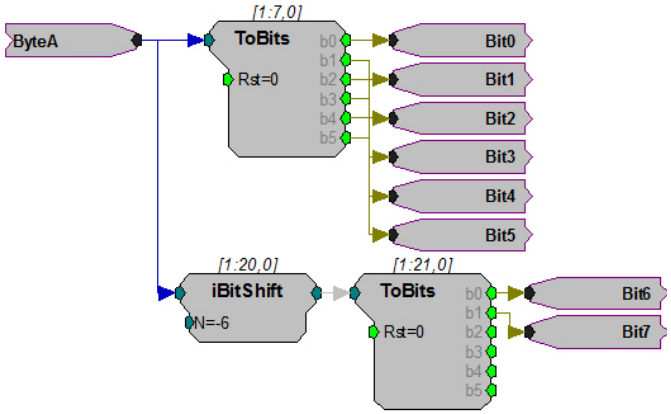
Reading Bytes A and B



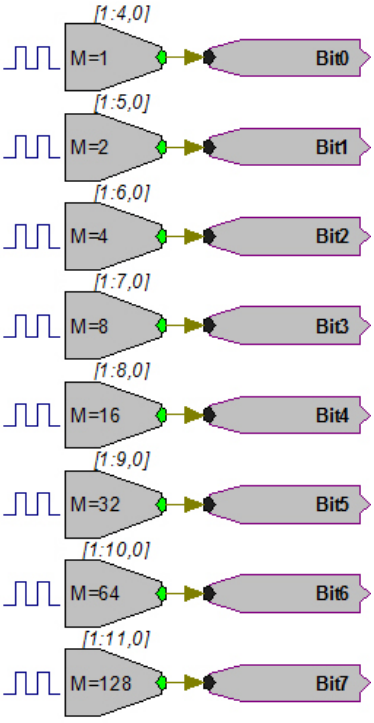
Writing to Bytes A and B

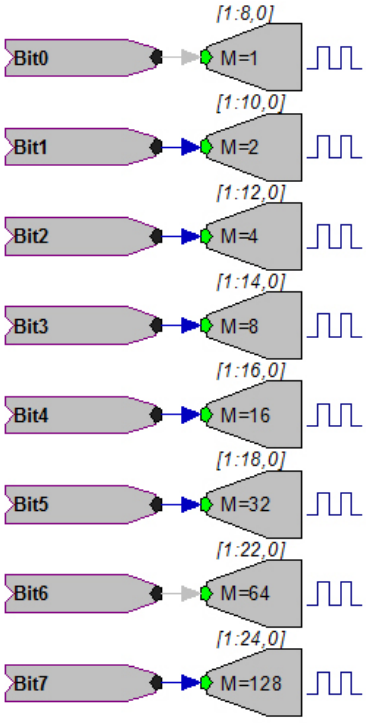


Reading Bits from a Byte



Bitmasks to Use for Accessing Bit Addressable Digital I/O with BitIn, BitOut Components

Port C As Inputs	Bit	Bitmask (Integer)
	0	M = 1
	1	M = 2
	2	M = 4
	3	M = 8
	4	M = 16
	5	M = 32
	6	M = 64
	7	M = 128

Port C As Outputs	Bit	Bitmask (Integer)
	0	M = 1
	1	M = 2
	2	M = 4
	3	M = 8
	4	M = 16
	5	M = 32
	6	M = 64
	7	M = 128

support@tdt.com
www.tdt.com