

Fast Facts

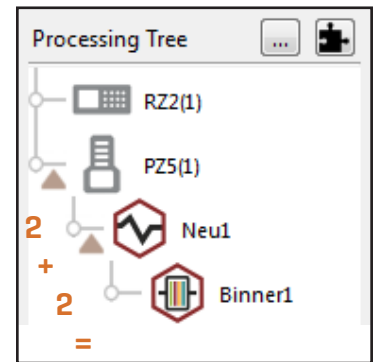
Input/Output Delays

There are two types of delays Synapse users should be aware of: gizmo delays and fixed sample delays associated with the I/O of their hardware devices. When synchronized processing is required, Synapse users can synchronize outputs or inputs using User Gizmos and delay components provided in RPsVsEx. See *User Gizmos in the Synapse Manual and Delay Functions in the Component Reference section of the RPsVsEx Manual for more information.*

Gizmo Delays

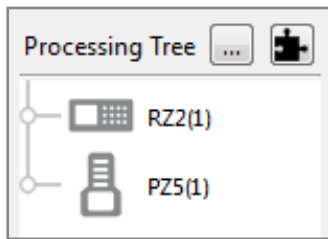
Each branch in the Synapse Processing Tree represents a signal flow or processing path. Each link in a branch adds exactly two samples of delay to that path. The path pictured to the right, from the PZ5 to the Binner, will have a four sample delay. You'll need to be aware of these small delays for experiments with complex processing paths that include many gizmos, custom user gizmos, or where timing is critical.

Gizmo Connections 2 samples



4 sample gizmo delays

Hardware Delays



In Synapse, I/O for your processor is configured in the hardware HAL. These settings are displayed and arranged on Tabs in the Options area when the device is selected in the Processing Tree.

Digital Input 2 samples

Digital Output 3 samples

| Options | | | | | |
|--|--------------------------|--------------------------|--------------------------|-------------------------------------|--------|
| RZ2(1) | | | | | |
| Main Digital I/O ADC DAC | | | | | |
| <input type="checkbox"/> Pair A/B to single port | | | | | |
| | Enable | Output | Invert | AutoID | ID |
| Port-A | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortA |
| Port-B | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortB |
| Port-C.0 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC0 |
| Port-C.1 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC1 |
| Port-C.2 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC2 |
| Port-C.3 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC3 |
| Port-C.4 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC4 |
| Port-C.5 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC5 |
| Port-C.6 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC6 |
| Port-C.7 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input checked="" type="checkbox"/> | PortC7 |

ADC and DAC delays are specific to the type of analog-to-digital and digital-to-analog converters used in the device. *See the table on page two for hardware specific delays.

| Main Digital I/O ADC DAC | | | | |
|--------------------------|--------------|--------|-------------------------------------|------|
| | Enable to... | Scaler | AutoID | ID |
| Adc.1 | Off | 1 | <input checked="" type="checkbox"/> | Adc1 |
| Adc.2 | Off | 1 | <input checked="" type="checkbox"/> | Adc2 |
| Adc.3 | Off | 1 | <input checked="" type="checkbox"/> | Adc3 |
| Adc.4 | Off | 1 | <input checked="" type="checkbox"/> | Adc4 |
| Adc.5 | Off | 1 | <input checked="" type="checkbox"/> | Adc5 |

ADC Delays Device Specific*

| Main Digital I/O ADC DAC | | | | |
|--------------------------|--------------|--------|----------|--|
| | Enable to... | Scaler | ID | |
| Dac.9 | Off | 1 | (select) | |
| Dac.10 | Off | 1 | (select) | |
| Dac.11 | Off | 1 | (select) | |
| Dac.12 | Off | 1 | (select) | |

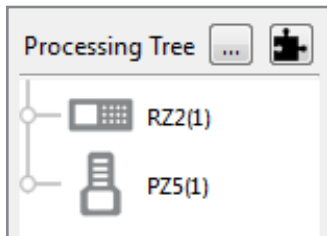
DAC Delays Device Specific*

DAC and ADC Processor Delays

The table below lists devices along with their associated DAC and ADC delays.

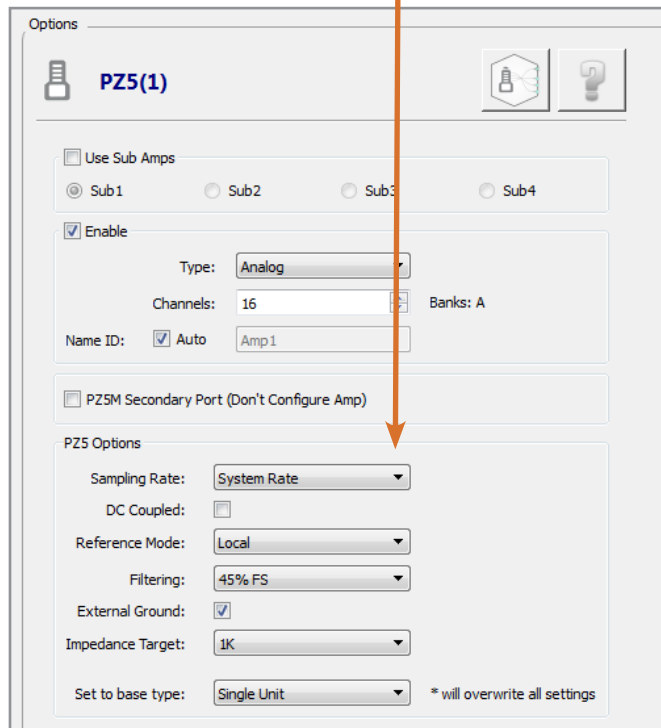
| Device | SD DAC | SD ADC | PCM DAC | PCM ADC |
|---------------------------|-------------------|-------------------|------------------|------------------|
| RZ2, RZ5, RZ5D, RZ5P, IZ2 | NA | NA | 4 samples | 3 samples |
| RZ6 | 31 samples | 66 samples | NA | NA |
| RX5, RX7, MS16 | NA | NA | 4 samples | NA |
| RX6 | 43 samples | 70 samples | NA | NA |
| RX8 | 23 samples | 47 samples | 4 samples | 3 samples |
| RP2.1 | 65 samples | 30 samples | NA | NA |
| RA16BA | 21 samples | NA | NA | NA |

ADC Amplifier Delays



Amplifier delays depend on a variety of factors including: the type on

Amplifier Delay Varies ADC converters, sampling rate, and system architecture. The amplifier's configuration options are displayed when the device is selected in the Processing Tree. The PZ5 HAL (pictured below) can be used to set an amplifier sampling rate or to follow the sampling rate of the RZ processor it is connected to (by selecting System Rate).



The tables below lists amplifiers along with their associated ADC delays.

PZ5 Hybrid ADC Delays

Dependent on PZ5 and RZ processor sample rates.

| PZ5 rate | [RZ at 25 kHz] samples | [RZ at 12 kHz] samples |
|----------|------------------------|------------------------|
| 25 kHz | 22 | x |
| 12 kHz | 40 | 23 |
| 6 kHz | 76 | 42 |
| 3 kHz | 141 | 79 |
| 1.5 kHz | 270 | 152 |
| 750 Hz | 543 | 295 |

Medusa ADC Delays

RA4PA and RA16PA: NA
RA16SD: **20 Samples**

PZ2 and PZ3 Delays

Dependent on RZ processor sample rate.

| Rate | Samples |
|--------|-----------|
| 6 kHz | 16 |
| 12 kHz | 17 |
| 25 kHz | 20 |
| 50 kHz | 26 |



support@tdt.com
www.tdt.com